Electronics for photodetectors

BEAUNE 2005

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Contents

- Overview of readout electronics
- Charge preamplifiers
- Noise
- Analog shaping
- ADCs
- Analog memories
- Digital signal processing
- (R)evolution(s) of analog and digital electronics
- Evolution of technologies
- Evolution of ASICs in particle physics
- Examples of designs

Thanks to: Eric Delagnes, Richard Hermel, Pierre Jarron, Jacques Lecoq, Gisèle Martin, Joel Pouthas, Veljko Radeka, Nathalie Seguin, Jean-Charles Vanel
Overview of readout electronics

- Most front-ends follow a similar architecture

Very small signals (fC) -> need amplification
- Measurement of amplitude and/or time (ADCs, discris, TDCs)
- Thousands to millions of channels
Readout electronics: requirements

- Low noise
- Low power
- High speed
- High reliability
- Radiation hardness
- Low material
- Low cost!
  (and even less)
- Radiation hardness
- High reliability
- Low power
Photodetector(s)

- A large variety, but a similar modelization
Detector modelization

- **Detector** = capacitance $C_d$
  - Pixels: 0.1-10 pF
  - PMs: 3-30 pF
  - Ionization chambers: 10-1000 pF
  - **Capa or transmission line?**

- **Signal**: current source
  - Pixels: $\sim 100e-/\mu m$
  - PMs: 1 photoelectron $\rightarrow 10^5-10^7$ e-
  - Modelized as an impulse (Dirac): $i(t)=Q_0\delta(t)$

- **Missing**:
  - High Voltage bias
  - Connections, grounding
  - Neighbours
  - Calibration...

[Diagram of detector modelization]
**Reading the signal**

- **Signal**
  - Signal = current source
  - Detector = capacitance $C_d$
  - Quantity to measure
    - Charge => integrator needed
    - Time => discriminator + TDC

- **Integrating on $C_d$**
  - Simple : $V = \frac{Q}{C_d}$
  - «Gain» : $1/C_d$ : 1 pF -> 10 mV/fC
  - Need a follower to buffer the voltage...
  - Input follower capacitance : $C_a // C_d$
  - Gain loss, possible non-linearities
  - crosstalk
  - Need to empty $C_d$...

---

**Impulse response**
Monolithic active pixels

Epitaxial layer forms sensitive volume (2-20 µm)

Charge collection by diffusion

Charge collected by N-well

Vreset Vdd

Out

Select Reset

MAPS readout

Column-parallel ADCs

Data processing / Output stage

Readout control

I2C control

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### Ideal charge preamplifier

- **ideal opamp in transimpedance**
  - Shunt-shunt feedback
  - Transimpedance: $v_{out}/i_{in}$
  - $V_{in}=0 \Rightarrow V_{out}(\omega)/i_{in}(\omega) = -Z_f = -1/j\omega C_f$
  - Integrator: $v_{out}(t) = -1/C_f \int i_{in}(t)dt$

\[ v_{out}(t) = -Q/C_f \]

- «Gain»: $1/C_f$: 0.1 pF $\rightarrow$ 10 mV/fC
- $C_f$ determined by maximum signal

- **Integration on $C_f$**
  - Simple: $V = -Q/C_f$
  - Unsensitive to preamp capacitance $C_{PA}$
  - Turns a short signal into a long one
  - The front-end of 90% of particle physics detectors...
  - But always built with custom circuits...

---

![Charge sensitive preamp](attachment:image.png)

![Impulse response with ideal preamp](attachment:image2.png)
Non-ideal charge preamplifier

- **Finite opamp gain**
  - \[ \frac{V_{out}(\omega)}{i_{in}(\omega)} = -\frac{Z_f}{(1 + C_d / G_0 C_f)} \]
  - Small signal loss in \( C_d / G_0 C_f \ll 1 \) (ballistic deficit)

- **Finite opamp bandwidth**
  - First order open-loop gain
  - \( G(\omega) = \frac{G_0}{(1 + j \omega/\omega_0)} \)
    - \( G_0 \) : low frequency gain
    - \( G_0 \omega_0 \) : gain bandwidth product

- **Preamp risetime**
  - Due to gain variation with \( \omega \)
  - Time constant : \( \tau = C_d / G_0 \omega_0 C_f \)
  - Rise-time : \( t_{10-90\%} = 2.2 \tau \)
  - Rise-time optimised with \( \omega_C \) or \( C_f \)

![Open-loop frequency response diagram](image)

![Impulse response with non-ideal preamp diagram](image)
Charge preamp seen from the input

- **Input impedance with ideal opamp**
  - \( Z_{in} = \frac{Z_f}{G+1} \)
  - \( Z_{in} \rightarrow 0 \) for ideal opamp
  - "Virtual ground" : \( V_{in} = 0 \)
  - Minimizes sensitivity to detector impedance
  - Minimizes crosstalk

- **Input impedance with real opamp**
  - \( Z_{in} = \frac{1}{j\omega G_0 C_f} + \frac{1}{G_0 \omega_0 C_f} \)
  - Resistive term : \( R_{in} = \frac{1}{G_0 \omega_0 C_f} \)
    - Exemple : \( \omega_C = 10^9 \) rad/s \( C_f = 0.1 \) pF => \( R_{in} = 10 \) k
  - Determines the input time constant : \( t = R_{eq} C_d \)
  - Good stability= (\ldots!)
Crosstalk

- **Capacitive coupling between neighbours**
  - Crosstalk signal is differentiated and with same polarity
  - Small contribution at signal peak
  - Proportionnal to $C_x/C_d$ and preamp input impedance
  - Slowed derivative if $R_i C_d \sim t_p$ => non-zero at peak

- **Inductive coupling**
  - Inductive common ground return
  - "Ground apertures" = inductance
  - Connectors : mutual inductance
Noise in charge pre-amplifiers

- 2 noise generators at the input
  - Parallel noise: \( (i_n^2) \) (leakage currents)
  - Series noise: \( (e_n^2) \) (preamp)

- Output noise spectral density:
  \[
  S_v(\omega) = \frac{i_n^2 + e_n^2/|Z_d|^2}{\omega^2 C_f^2}
  = \frac{i_n^2}{\omega^2 C_f^2} + \frac{e_n^2 C_d^2}{C_f^2}
  \]
  - Parallel noise in \( 1/\omega^2 \)
  - Series noise is flat, with a « noise gain » of \( C_d/C_f \)

- \textit{rms} noise \( V_n \)
  \[
  V_n^2 = \int S_v(\omega) \, d\omega / 2\pi \rightarrow \infty
  \]
  - Benefit of shaping...
Equivalent Noise Charge (ENC) after CRRC\(^n\)

- Noise reduction by optimising useful bandwidth
  - Low-pass filters (RC\(^n\)) to cut-off high frequency noise
  - High-pass filter (CR) to cut-off parallel noise
  - \(\rightarrow\) pass-band filter CRRC\(^n\)

- Equivalent Noise Charge : ENC
  - Noise referred to the input in electrons
  - \(\text{ENC} = \text{I}_a(n) e_n C_t / \sqrt{T} \oplus \text{I}_b(n) i_n^* \sqrt{T}\)
  - Series noise in \(1/\sqrt{T}\)
  - Parallel noise in \(\sqrt{T}\)
  - 1/f noise independant of \(T\)
  - Optimum shaping time \(\tau_{\text{opt}} = \tau_c / \sqrt{2n-1}\)

- Peaking time \(t_p\) (5-100%)
  - \(\text{ENC}(t_p)\) independent of \(n\)

- Complex shapers are obsolete :
  - Power of digital filtering
  - Analog filter = CRRC ou CRRC\(^2\)
**Equivalent Noise Charge (ENC) after CRRC$^n$**

- **A useful formula:** ENC (e- rms) after a CRRC$^2$ shaper:

\[
ENC = 174 \, e_n C_{tot} / \sqrt{t_p (\delta)} + 166 \, i_n \sqrt{t_p (\delta)}
\]

- $e_n$ in nV/√Hz, $i_n$ in pA/√Hz are the preamp noise spectral densities.
- $C_{tot}$ (in pF) is dominated by the detector ($C_d$) + input preamp capacitance ($C_{PA}$).
- $t_p$ (in ns) is the shaper peaking time (5-100%).

**Noise minimization**

- Minimize source capacitance.
- Operate at optimum shaping time.
- Preamp series noise ($e_n$) best with high transconductance ($g_m$) in input transistor.
- $\Rightarrow$ large current, optimal size.
ENC for various technologies

- ENC for $C_d=1$, 10 and 100 pF at $I_B=500$ uA
- MOS transistors best between 20 ns - 2 $\mu$s

### Parameters

- **Bipolar**:
  - $g_m = 20$ mA/V
  - $R_{BB'}=25$ $\Omega$
  - $e_n = 1$ nV/$\sqrt{\text{Hz}}$
  - $I_B=5$ uA
  - $i_n = 1$ pA/$\sqrt{\text{Hz}}$
  - $C_{PA}=100$ fF

- **PMOS 2000/0.35**:
  - $g_m = 10$ mA/V
  - $e_n = 1.4$ nV/$\sqrt{\text{Hz}}$
  - $C_{PA}=5$ pF
  - $1/f$:
MOS input transistor sizing

- **Capacitive matching: strong inversion**
  - $g_m$ proportional to $W/L \sqrt{I_D}$
  - $C_{GS}$ proportional to $W*L$
  - ENC proportional to $(C_{det} + C_{GS})/ \sqrt{g_m}$
  - Optimum $W/L : C_{GS} = 1/3 \ C_{det}$
  - Large transistors are easily in moderate or weak inversion at small current

- **Optimum size in weak inversion**
  - $g_m$ proportional to $I_D$ (indep of $W,L$)
  - ENC minimal for $C_{GS}$ minimal, provided the transistor remains in weak inversion
Example of charge preamps

- **FLC_PHY3 for CALICE Si diodes**
  - 18 channels variable gain low noise preamp
  - Optimized for $C_d=20-100$ pF
  - Bi-gain shaper
  - Linearity 0.1%
  - Multiplexed output
  - 3 000 chips produced in 2003 in 0.8µm

- **FLC_PHY4**
  - Variable gain preamp variable shaper
  - Pulsed power
  - Includes 12bit ADC
FLC_TECH1 : noise performance

- **FLC_TECH1 : 0.35µm**
  - Series : $e_n = 1.4 \text{nV/√Hz}$, $C_{PA} = 7 \text{ pF}$
  - $1/f$ noise : 12 e-/pF
  - Parallel : $i_n = 40 \text{ fA/√Hz}$

![Graph: ENC vs Peaking time and ENC vs Capacitance $t_p=100\text{ns}$]
16 channels readout for CdTe detector
- Low noise charge preamps
- Optimized for $C_d = 2\text{-}5 \text{ pF}$
- Variable SallenKey shapers
- Peak detection
- Discriminator
- Multiplexed output
Current preamplifiers:

- Transimpedance configuration
  - \( \frac{V_{\text{out}}(\omega)}{i_{\text{in}}(\omega)} = -\frac{R_f}{1+Z_f/GZ_d} \)
  - Gain = \( R_f \)
  - High counting rate
  - Typically optical link receivers

- Easily oscillatory
  - Unstable with capacitive detector
  - Inductive input impedance
    \[ L_{\text{eq}} = \frac{R_f}{\omega C} \]
  - Resonance at: \( f_{\text{res}} = \frac{1}{2\pi} \sqrt{L_{\text{eq}}C_d} \)
  - Quality factor: \( Q = \frac{R}{\sqrt{L_{\text{eq}}C_d}} \)
    - \( Q > 1/2 \rightarrow \text{ringing} \)
  - Damping with capacitance \( C_f \)
    - \( C_f = 2 \sqrt{C_d/R_f G_0 \omega_0} \)
    - Easier with fast amplifiers

Diagram: Current sensitive preamp
High speed transimpedance amplifier

- **Fast transimpedance amplifiers**
  - $R_f = 25k \, C_f = 10fF$
  - SiGe process
  - 15 GHz gain-bandwidth product
  - See talk on OPERA_ROC

- **40 Gb/s transimpedance for optical receiver**
  - Simple architecture (CE + CC)
  - SiGe bipolar transistors
  - CC outside feedback loop

Open loop frequency response of SiGe amplifier
ADCs : G.D.A.S.A.P.

- The era of G.D.A.S.A.P. : « go digital as soon as possible »
  - Spectacular evolution of ADCs : more bits, faster, less watts
  - Propelled by evolution of technologies and telecom
  - Has revolutionized signal processing

Resolution vs speed of ADCs in 2002
© L. Dugoujon STm
Integrating the ADCs:

- Possible use of IPs (expensive)
- Huge effort started in in2p3/CEA
  - Several designs in institutes
  - 10 bit pipeline ADC (LPCC) 10MHz
  - 10 Bit C/2C SAR (LAL) 1 mW 1 MHz
  - 10 bit FADC (LAL) 100 MHz
    
      See poster by B. Genolini
  - 12 bit Wilkinson (CEA,LAL,LPCC)
    
      See talk by R. Gaglione 22/6

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**FEATURES**

- Small Area < 0.83mm²
- Size x= 842µm y= 960µm
- Supply Voltage 2.7-3.6 V
- Junction Temp. Range -40 - 125°C
- Resolution 12-Bit
- Maximum Sampling Rate 1.5MS/s
- Track and Hold Input Stage
- Rail-to-Rail Dynamic Range
- Single Ended and Fully Differential Input Stage
- Low Power of 8mW at 3.3V Supply Voltage
- Self Power Down Mode

**DESCRIPTION**

The SCADC12F is a complete analog to digital converter cell which operates from a single supply. It performs sampling, analog-to-digital conversion, generating a true 12 bit value in parallel form. The output word rate can be up to 1.5MS/s. The output data format is compatible with most µP and digital signal processors and can be unipolar or bipolar.
Analog memories

- **Switched Capacitor Arrays (SCAs)**
  - Store signal on capacitors (~pF)
  - Fast write (~GHz)
  - Slower read (~10MHz)
  - Dynamic range: 10-13 bits
  - Depth: 100-2000 caps
  - Unsensitive to cap absolute value (voltage write, voltage read)
  - Low power
  - Possible loss in signal integrity (droop, leakage current)

- **The base of 90% of digital oscilloscopes!**
Example: SAM for HESS2

- Swift Analog Memory
  - 3 Gsamples/s >10 bits

See talk by E. Delagnes 20/6

Swift Analog Memory

3 Gsample/s >10 bits

16 columns

16 delays / column

wck

In

unsigned

buffers

Phase comparator
+ Charge Pump

2 ns pulse in SAM0

Chip layout in 0.35µ CMOS
**Pipeline 12b 2GHz**

- **MATACQVME**
  - VME board with 4-8 channels
  - 2 GHz - 12 bits
  - Auto-trigger mode
  - Sold by CAEN

![Diagram of Pipeline 12b 2GHz](image-url)
Digital filtering

- Linear sums of sampled signal
  - Finite Impulse Response (FIR)
  - made possible by fast ADCs (or analog memories)...

- Signal: \( s(t) = A g(t) + b \)
  - \( A \): amplitude
  - \( G(t) \): normalised signal shape
  - \( B \): noise
  - Sampled signal: \( s_i = A g_i + b_i \)

- Filter: weighted sum \( \sum a_i s_i \)
  - \( a_i = \sum R^{-1}_{ij} g_i \)
  - \( R \): autocorrelation function
  - \( g_i \): signal shape
    - \((0, 0.63, 1, 0.8, 0.47)\)
  - \( S = \sum_{i=1}^{n} a_i s_i \)
Exemple : ATLAS “multiple sampling”

- Slowing down the signal
  - Reduction of series noise
  - Similar to a simple integration

- Accelerating the signal
  - Reduction of pileup noise
  - Similar to a differentiation

- Measuring the timing

Signal before and after digital filtering

\[
\begin{align*}
A &= (0.17, 0.34, 0.4, 0.31, 0.28) \\
A &= (-0.75, 0.47, 0.75, 0.07, -0.19)
\end{align*}
\]
(R)evolution of analog electronics (1)

- Access to microelectronics

Charge preamp in SMC hybrid techno

Charge preamp in 0.8\(\mu\)m BiCMOS

FET

\(6\text{ cm}\)

\(100\,\mu\text{m}\)

\(Z_0\)

\(Z_f\)
(R)evolution of analog electronics (2)

- **ASICs**: Application Specific Integrated Circuits
  - Access to foundries through *multiproject runs (MPW)*
  - Reduced development costs: 600-1000 €/mm² compared to dedicated runs (50-200 k€)
  - Full custom layout, at transistor level
  - Mostly *CMOS & BiCMOS*

- **Very widespread in high Energy Physics**
  - High level of integration, limited essentially by power dissipation and parasitic couplings (EMC)
  - Better *performance*: reduction of parasitics
  - Better *reliability* (less connections)
  - But longer developpement time
Processing of ASICs

- From Sand to ICs...

RETICLE
(Pattern with 0.7 micron apertures ie 4 X 0.18)

Light Sensitive Coating.

Silicon Wafer

Lithography.

UV Light

CREATING > 125 million TRANSISTORS ON EACH MICROPROCESSOR;

WITH FEATURES 1/2000th THE WIDTH OF A HUMAN HAIR.
Evolution of technologies

First transistor (1949) (Brattain-Bardeen Nobel 56)

SiGe Bipolar in 0.35μm monolithic process

First planar IC (1961)

5 μm MOSFET (1985)

15 nm MOSFET (2005)

20 June 2005

C. de La Taille Tutorial Electronics for photodetectors Beaune 2005
Evolution of CMOS technologies

Moore's law: doubling every 2 years
Goal: Over 1 billion transistors by 2005

<table>
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<th>i386</th>
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<td>5</td>
<td>5</td>
<td>5/3.3</td>
<td>1.3 internal</td>
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</table>
« CMOS scaling »

- **Reduction of dimensions**
  - Gate length : $L$
  - Oxide thickness : $t_{ox}$

- **Reduction of power supplies**
  - Reduction of power dissipation

- **Improvement of speed in $1/L^2$**
  - Transconductance : $g_m \propto W/L$
  - Capacitance : $C \propto WL$
  - Speed : $F_T = g_m/C \propto 1/L^2$

- **Reduction of costs (?)**
  - Increase of integration density

- **Radiation hardness in bonus !**
  - Less trapping in gaye oxide

Principle of Nchannel MOSFET
Evolution of CMOS technologies (2)

- Differences between analog/mixed signal and digital technologies
  - Very fast evolution of digital technologies (faster design migration)
  - More « perene » analog technologies (SiGe, BiCMOS...) (driven by mobile telecom and automotive)
  - A visible split occurring

- More difficult analog design in low voltage
  - « no more headroom for signals »

![Diagram showing the evolution of gate length and voltage over time.](Image)
SiGe technology

- Faster bipolar transistors for RF telecom
  - Better mobility and FT
  - Better current gain (beta)
  - Better Early voltage
  - Interesting improvement at low T
  - Compact CMOS (0.25 or 0.35µm) for mixed-signal design

© R. Hermel

d’a après [1]
Cost of ASICs

- **MPW (multi-project wafers)**
  - CMOS 0.35µm (AMS) : 650 €/mm²
  - BiCMOS SiGe 0.35 µm (AMS) : 900 €/mm²
  - CMOS 0.13µ (STm) : 2500 €/mm²
  - CMOS 90 nm (STm) : 5000 €/mm²
  - Usually a few 10 to 100 pieces in a MPW run

- **Production runs**
  - Masks : 91 k€ (CMOS 0.35µm)
  - 8" wafers : 4 k€, useful area : 25 000 mm² = several thousands of chips

- **Packaging**
  - Ceramic : 20-30€/chip
  - Plastic : 2k€ + 1-2 €/chip

- **Example : chip 10mm² 16 channels**
  - 100 chips (MPW) : 120€/chip, 7€/channel
  - 10 000 chips (4wafers) : 12€/chip < 1€/channel
(R)evolution of digital electronics (1)

- From stacks of circuits to FPGAs: programmable gate arrays
(R)evolution of digital electronics (2)

- Schematic -> High level languages (Verilog, VHDL)
  - Example 8 bit comparator
  - 74LS866

- VHDL comparator:
  
  ```vhdl
  entity comparator_8 is
  port ( raz : in std_logic;
         val1, val2 : in std_logic_vector(7 downto 0)
       result : out std_logic
     );
  end entity comparator_8;
  architecture archi_& of comparator_8 is
  begin
    result <= '0' when raz = '0' else '1' when val1 > val2 else '0'
  end architecture archi_1;
  ```
(R)evolution of digital electronics (3)

- **Reduction of digital logic levels**
  - 1980: **TTL**: 0-5 V
  - 2000: **LVDS**: Low Voltage (±400 mV) Differential Swing
  - Better signal integrity (EMC)
  - Reduction of power supplies 5V → 3.3V → 2.5V → 1.2V

- **Components: the revolution of FPGAs**:
  - = Field Programmable Arrays (Altera©, Xilinx©)
  - 4-40 millions gates (55M in a Pentium4)
  - RISC 32bits processors
  - 10 Mbits resident memory
  - 2000 pins 1300 I/O (inputs/outputs)
  - 300 MHz operation
FPGAs as blackhole of digital electronics?

- RISC processors
- Memories & FIFOs
- Clocks & PLLs
- IP standard interfaces (Ethernet, USB, PCI...)
- Matching networks
- DSP blocks, arithmetics
- Bus interfaces (GTL, LVDS...)

©JP Cachemiche
Electromagnetic compatibility (EMC-EMI)

- **Coexistence analog-digital**
  - Capacitive, inductive and common-impedance couplings
  - A full lecture!
  - A good summary: there is no such thing as «ground», pay attention to current return
Effect of radiations on components

- **TID**: total ionising dose effects
  - Charge trapping in gate oxide
  - Alleviated in thin oxides (Deep SubMicron DSM)
  - Radiation tolerant layout techniques designed by CERN RD49 in 0.25µm

- **NIEL**: non ionising energy loss
  - Cristal damage with neutrons
  - Beta drop in bipolar transistors

- **SEU**: Single Event Effect
  - Effect of large ionising impact: local charge deposition on critical nodes
  - SEU: single event Upset = bit flip
  - SEL: single Event Latchup: thyristor setting -> destructive!

![Radiation levels in ATLAS (rads/an)](image)

1 krad/an $10^{11}$ N/cm²
1 Mrad/an $10^{14}$ N/cm²

Galactic Cosmic Rays

Solar Protons & Heavier Ions

Trapped Particles
# Radiation hardness: space vs LHC

<table>
<thead>
<tr>
<th></th>
<th>Space missions</th>
<th>LHC experiments</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Mission Time</strong></td>
<td>10-15 years</td>
<td>10 years</td>
</tr>
<tr>
<td><strong>Service</strong></td>
<td>Not Possible</td>
<td>Impractical</td>
</tr>
<tr>
<td><strong>Electronics Reliability</strong></td>
<td>High</td>
<td>High</td>
</tr>
<tr>
<td><strong>Total Dose Requirements</strong></td>
<td>10 -100 krad</td>
<td>1 krad - 10 Mrad</td>
</tr>
<tr>
<td><strong>Non Ionizing Energy Loss (N)</strong></td>
<td>~0</td>
<td>$10^{13}-10^{15}$ N/cm²</td>
</tr>
<tr>
<td><strong>Single Event Upsets</strong></td>
<td>IC's SEU characterised</td>
<td>No Critical SEU Accepted</td>
</tr>
</tbody>
</table>

=> Similar requirements
Summary of radiation effects on components

**IONISING**
(TID)
Gy, rad

- NMOS: $V_t \uparrow$ or $\downarrow$
- PMOS: $V_t \uparrow$
- $g_m \downarrow$
- $I_{\text{leak}} \uparrow$

**NON IONISING**
(NIEL)
Fluence or particles/cm²

- Atomic displacement

**Bipolar:**
$\beta \downarrow$

**Optoelect.**

---

**Single Event Effects**
(SEE)
Occurrence rate

- SEU (transient)
- SEE permanent
- SEL, SEGR, SEB

**MOS**

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46
Examples: tracker circuits APV25

- **High level of intégration**
  - 128 preamps/shapers, 128*160 analog pipelines
  - Mode peak & déconvolution, multiplexed output, internal calibration...

- **Performance**
  - Dynamic range ±13 MIP, low dissipation (2µW/ch), Low noise: ~200e-

[Diagram of APV25 readout chip]
Example 2: variable everything

- SiPM readout chip for CALICE AHCAL
- 0-5V 8 bit DAC for gain adjustment
- Variable gain preamp
- Variable gain shaper
- 18 channels, multiplexed output

SiPM readout chip for CALICE AHCAL

- Gain adjustment
- Preamp
- Shaper
- 18 channels

SiPM +HV

100 kΩ

100 MΩ

0.1p

0.2p

0.4p

0.8p

DAC

0-5V

10p

Rin =

10k

Ω

8-bit

12k

Ω

2.4p

1.2p

0.6p

0.3p

100 MΩ

4kΩ

24p

12p

6p

3p

2.4p

1.2p

0.6p

0.3p

0-5V 8 bit DAC for gain adjustment

Variable gain preamp

Variable gain shaper

18 channels, multiplexed output
Example 3: Towards SoCs...

- **System on Chip (SoC):** multi-fonctionnalité
- **Ex:** ARS chip for Antarès: pipelines 1GHz, TDC, ADCs...
Evolution 1: integrating the detector (MAPS)

RAL Camera-on-a-chip

- 0.5 µm CMOS technology
- Design 1\textsuperscript{st} time right
- Noise ≤ 50 electrons
- Power consumption: ≤ 300mW
- 3.3V Operation
- Readout control
- Readout speed: 10 Frames/Second
- Adjustable Gain Column Amplifiers
- 10 Bit ADC/Column
- Alternative analogue output
- Parallel digital output
- I\textsuperscript{2}C control system
- Rad Tolerant Design, Triple

525 by 525 array of 25µm pixels
Evolution 1: integrating the detector (TFA)

TFA or above ASIC technology

- Emerging sensor technology for APS
  - Adapted for a-Si:H thick films
    - Bottom thin n-doped layer ~ 20 nm
    - Middle thick i-layer layer ~ 5-30 μm
    - Top thin p-doped layer ~ 40 nm
    - Indium Tin Oxide ITO ~ 100nm
  - Pixel segmentation of the n-i-p film
    - High resistivity n-layer

![TFA Concept](image)

![Thick TFA cross section](image)
Evolution 2: integrating the backend

- ALICE TPC readout: ALTRO chip (CERN) 8 ch/chip
  - Internal ADC: 10 bits 20MHz
  - Digital tail cancelation and baseline correction

Power consumption: < 40 mW/channel

- L1: 5 µs
  - 200 Hz
- L2: < 100 µs
  - 200 Hz

- 8 CHIPS x 16 CH/CHIP

- CUSTOM IC (CMOS 0.35 µm)

- CUSTOM IC (CMOS 0.25 µm)

- 570132 PADS

- PASA

- ADC

- Digital Circuit

- RAM

- MULTI-EVENT MEMORY

- Power consumption: < 40 mW/channel

- 1 MIP = 4.8 fC
  - S/N = 30 : 1
  - DYNAMIC = 30 MIP

- CSA
  - SEMI-GAUS. SHAPER
  - GAIN = 12 mV/fC
  - FWHM = 190 ns

- 10 BIT
  - < 10 MHz

- • BASELINE CORR.
  - • TAIL CANCELL.
  - • ZERO SUPPR.
Integrating the backend (2)

- ALTRO chip (CERN)
  - Detail du digital processing
Conclusion

- A real move towards “smart sensors”

- micro-electronics getting closer to detector
  - Unavoidable with increase of channels number
  - Cost reduction

- Backend more and more integrated
  - Integration of ADC
  - Signal processing
  - Loading of parameters

USB