



SiPMs with bulk integrated resistors – Future perspectives –

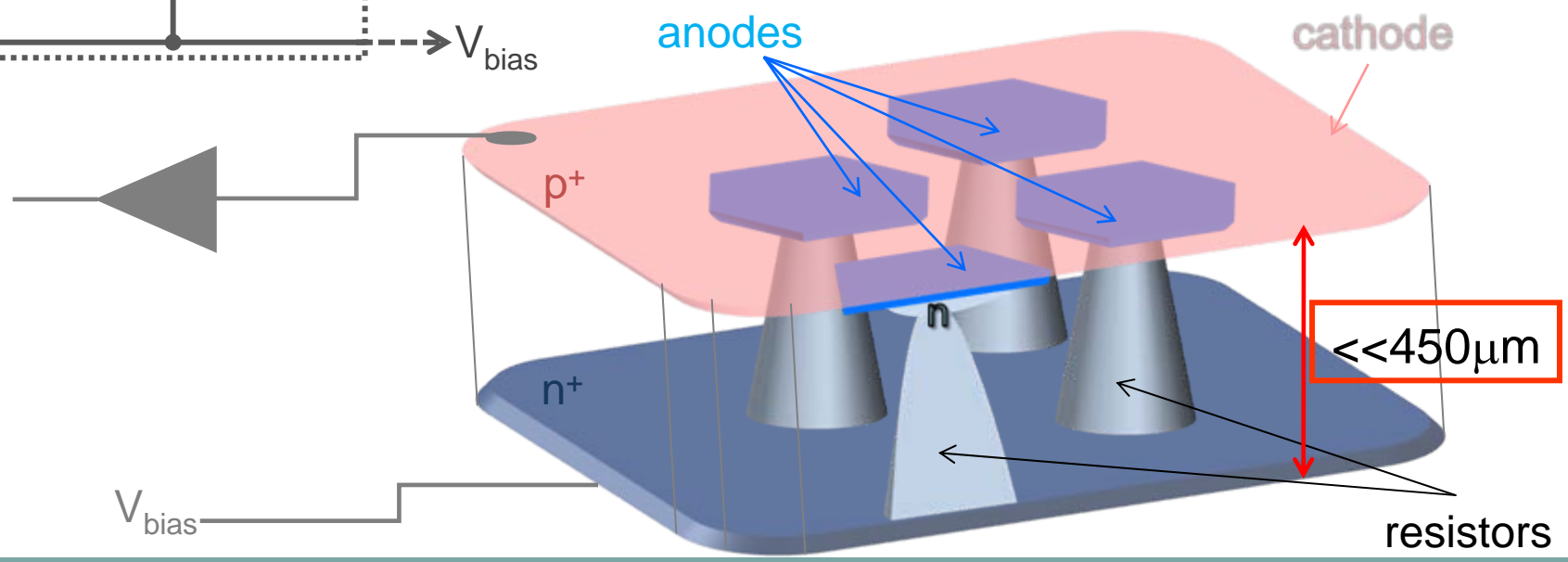
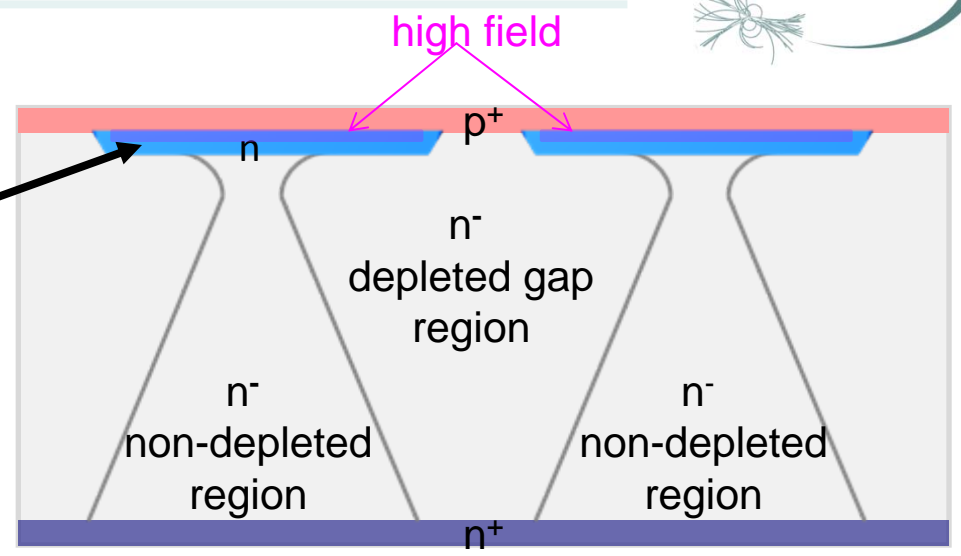
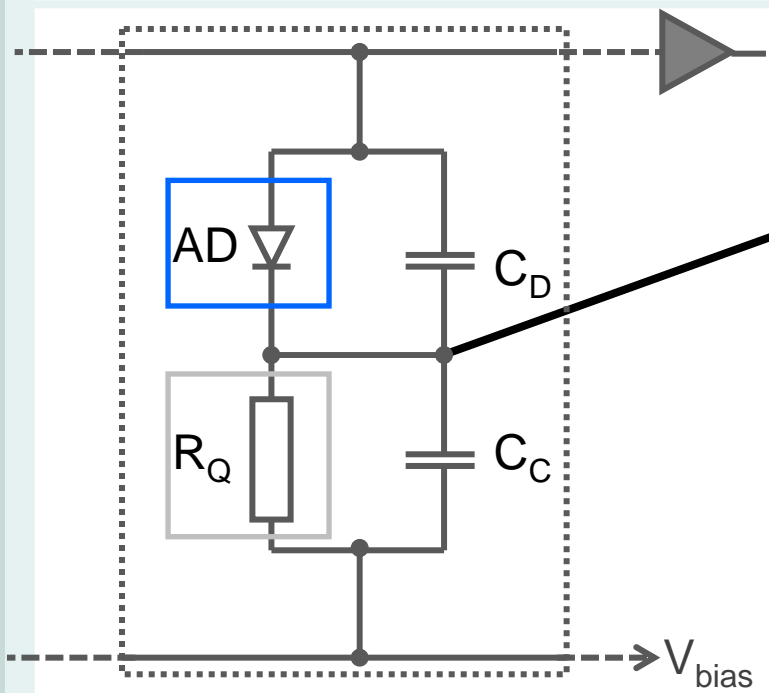
- Concept of SiPMs with Bulk Integrated Quench Resistors – SiPMI concept
- First results from the prototype production
- Future perspectives

J. Ninkovic¹, L. Andricek¹, C. Jendrysik¹, G. Liemann¹, G. Lutz², H. G. Moser¹, R. H. Richter¹

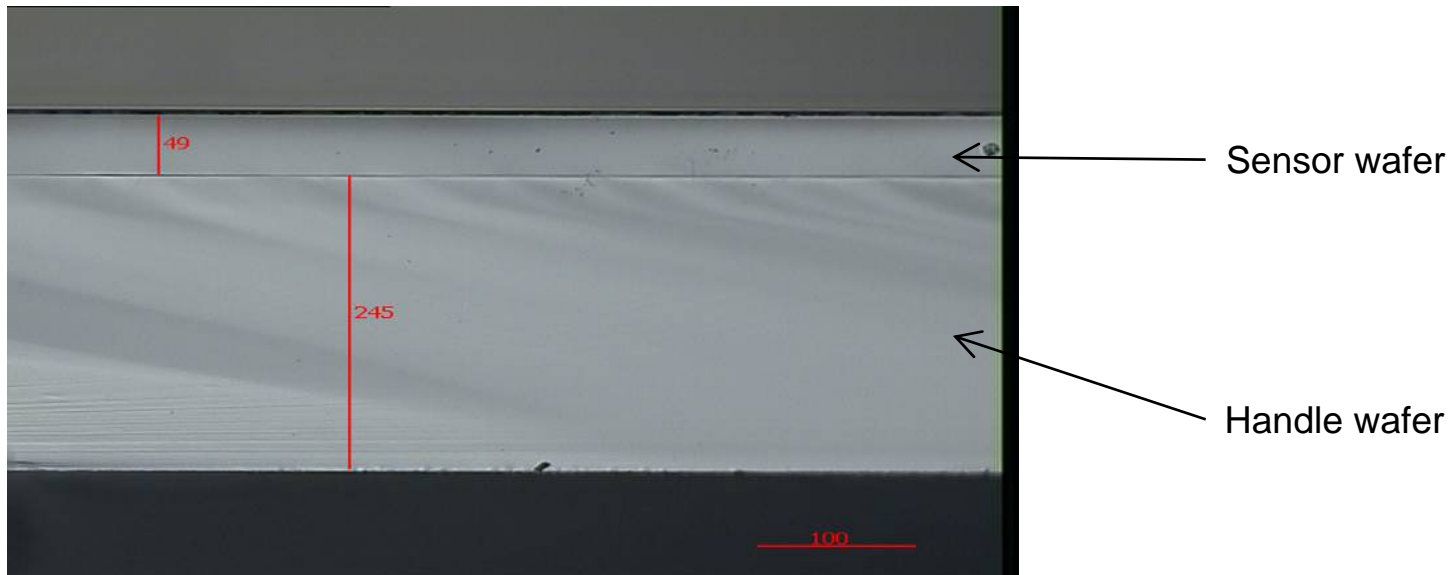
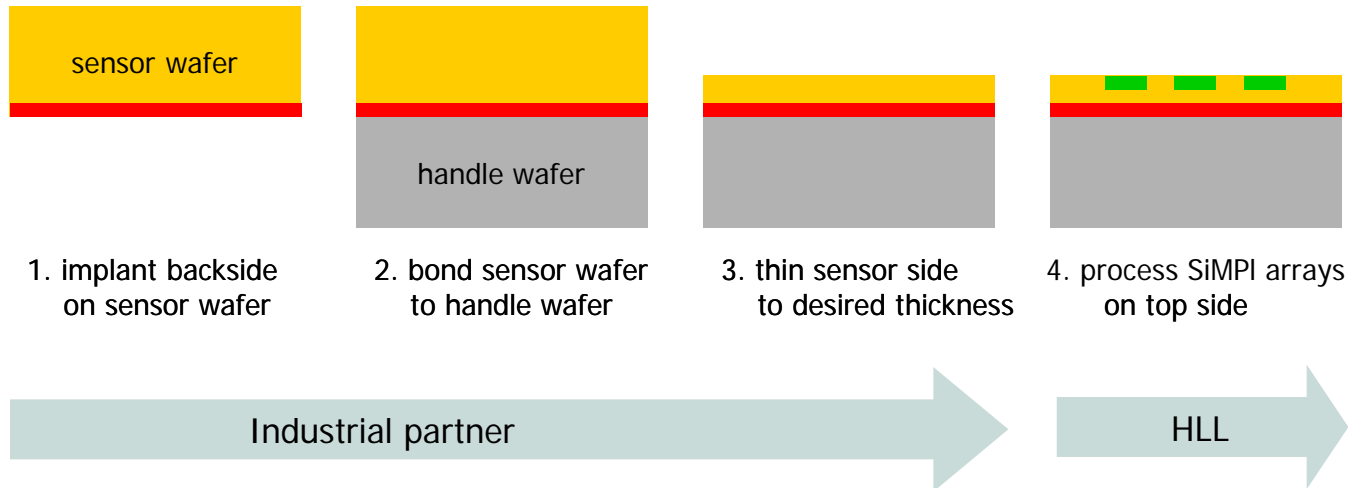
¹Max Planck Institute for Physics, Semiconductor Laboratory, Munich, Germany

²PN Sensor GmbH, Munich, Germany

● SiPM cell components → SiMPI approach



SOI wafers



● Advantages and Disadvantages



Advantages:

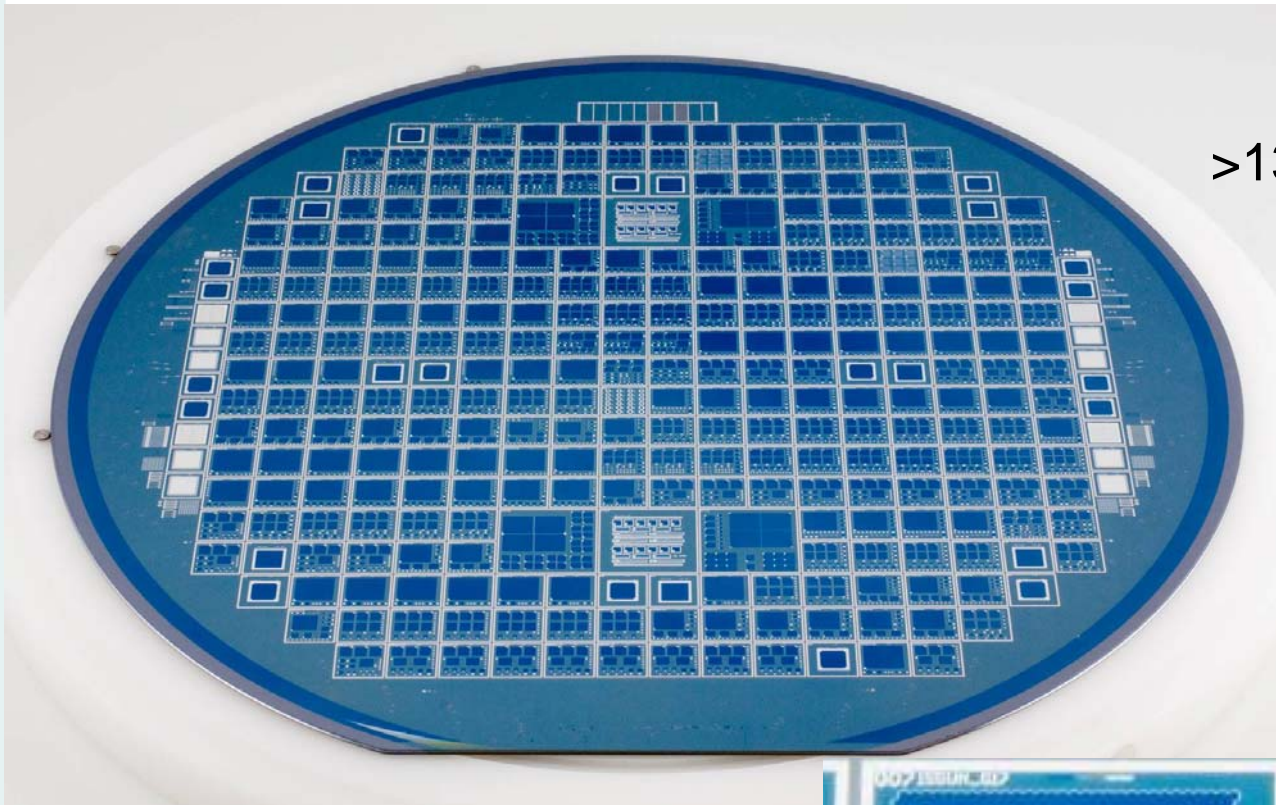
- no need of polysilicon
- free entrance window for light, no metal necessary within the array
- coarse lithographic level
- simple technology
- inherent diffusion barrier against minorities in the bulk -> less optical cross talk

Drawbacks:

- required depth for vertical resistors does not match wafer thickness
- wafer bonding is necessary for big pixel sizes, epi can be used for small pixel sizes
- significant changes of cell size requires change of the material
- vertical 'resistor' is a JFET -> parabolic IV -> longer recovery times

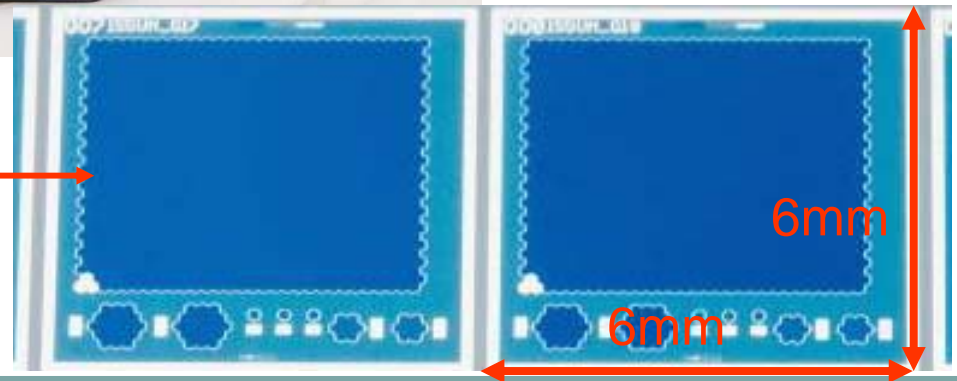
- Prototype production

Idea presented Light 2007, NDIP 2008



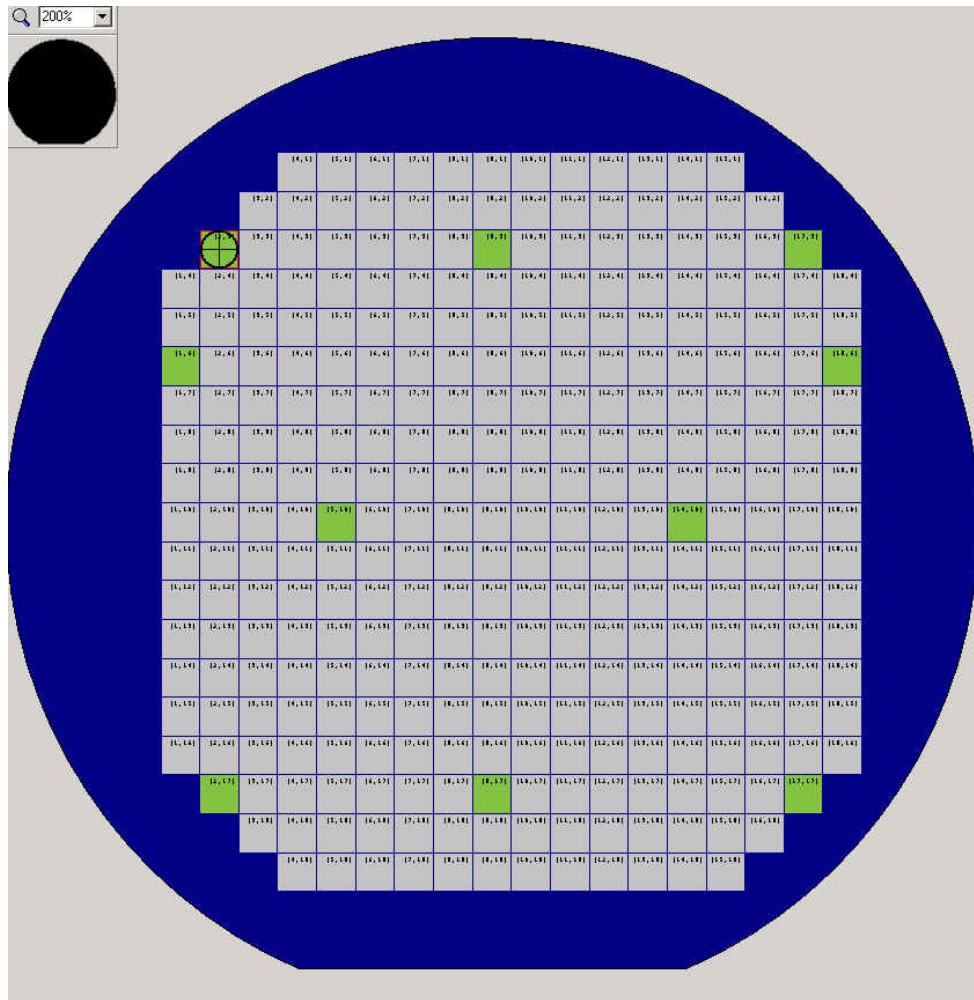
>130 different chips

30x30 array
sensitive area free



Bulk doping variation of the top wafers measured on 10 diodes*/wafer (CV)

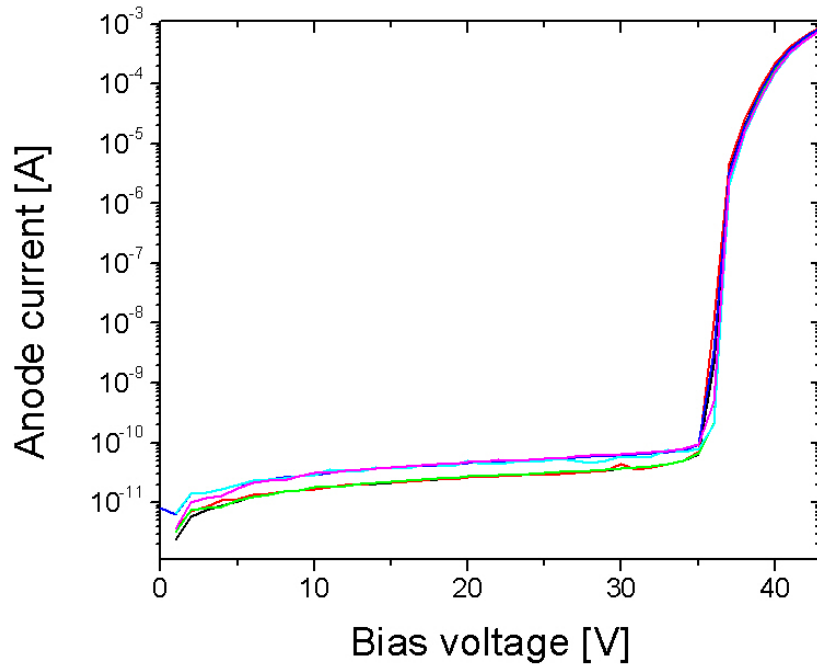
(*test diodes without high energy implantation)



Standard deviation
1—2% of the mean value
over the wafer

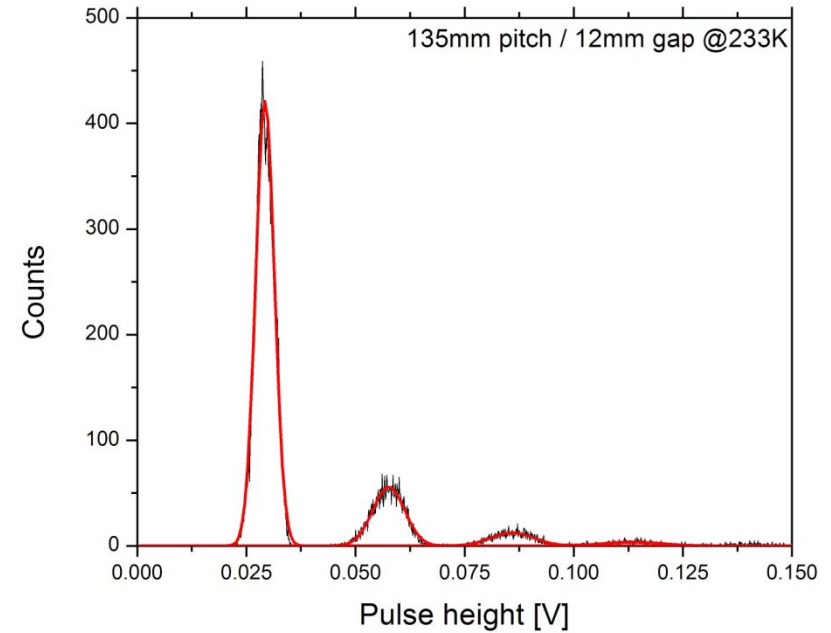
● Results

Static measurements



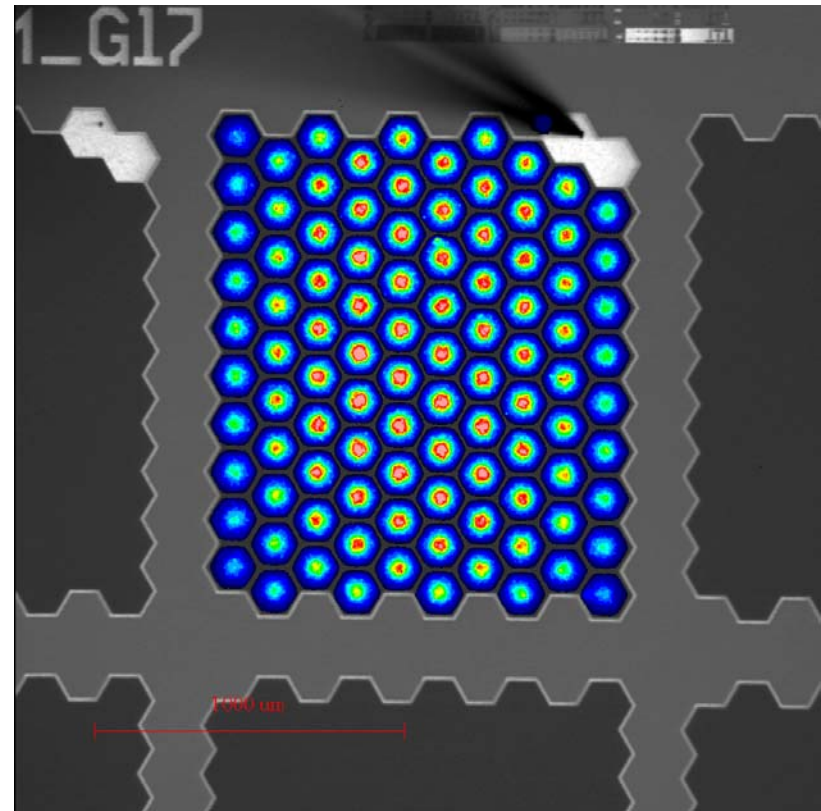
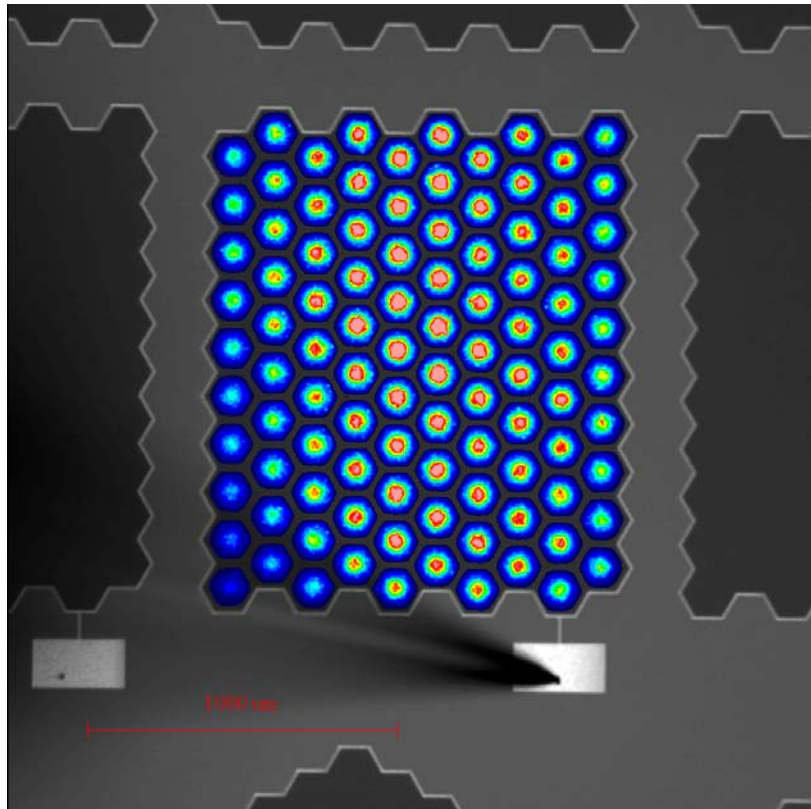
High homogeneity over big distances!
6 (10x10) arrays placed over
6mm distance

Dynamic measurements



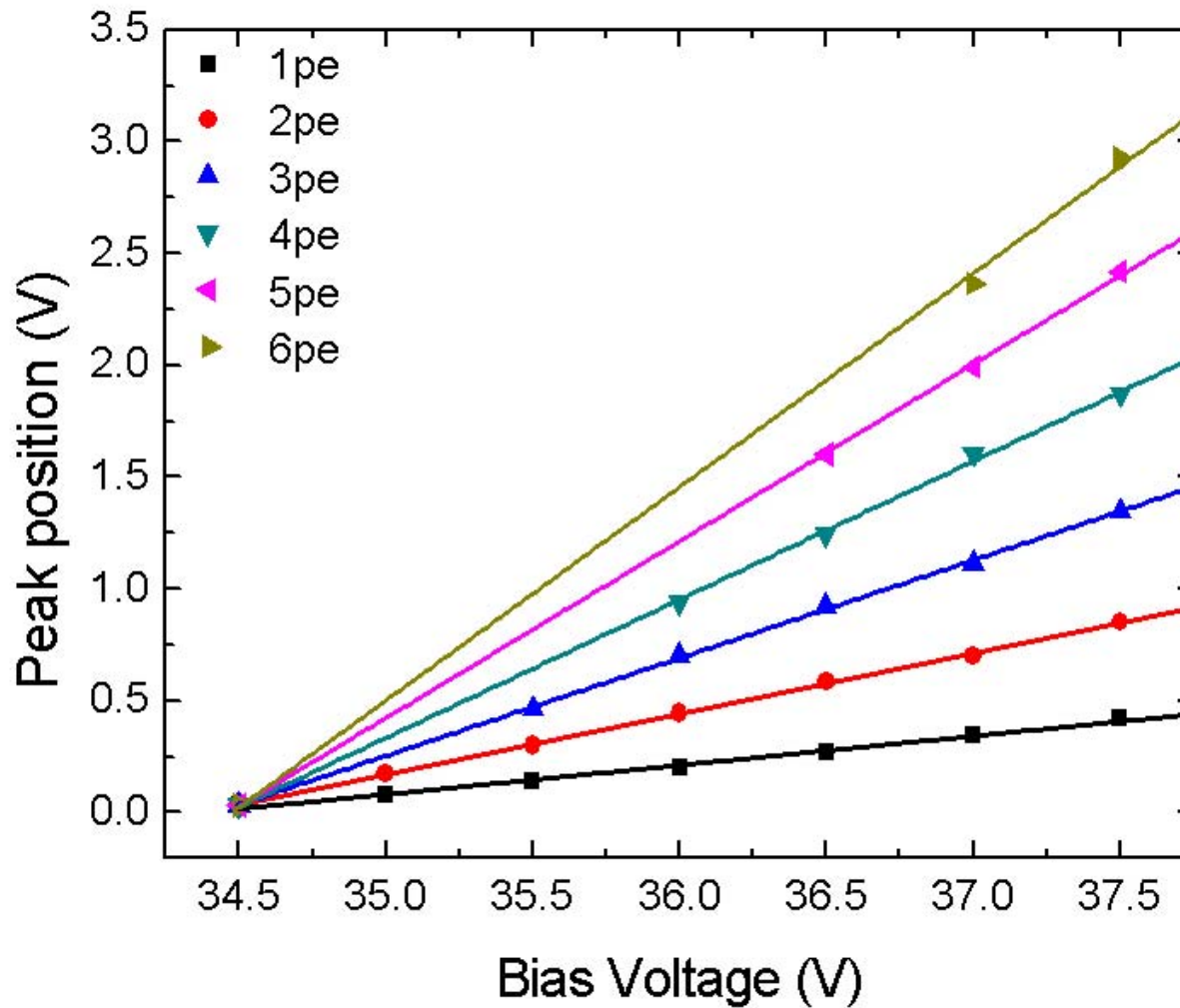
High homogeneity within the array!

- Photoemission images



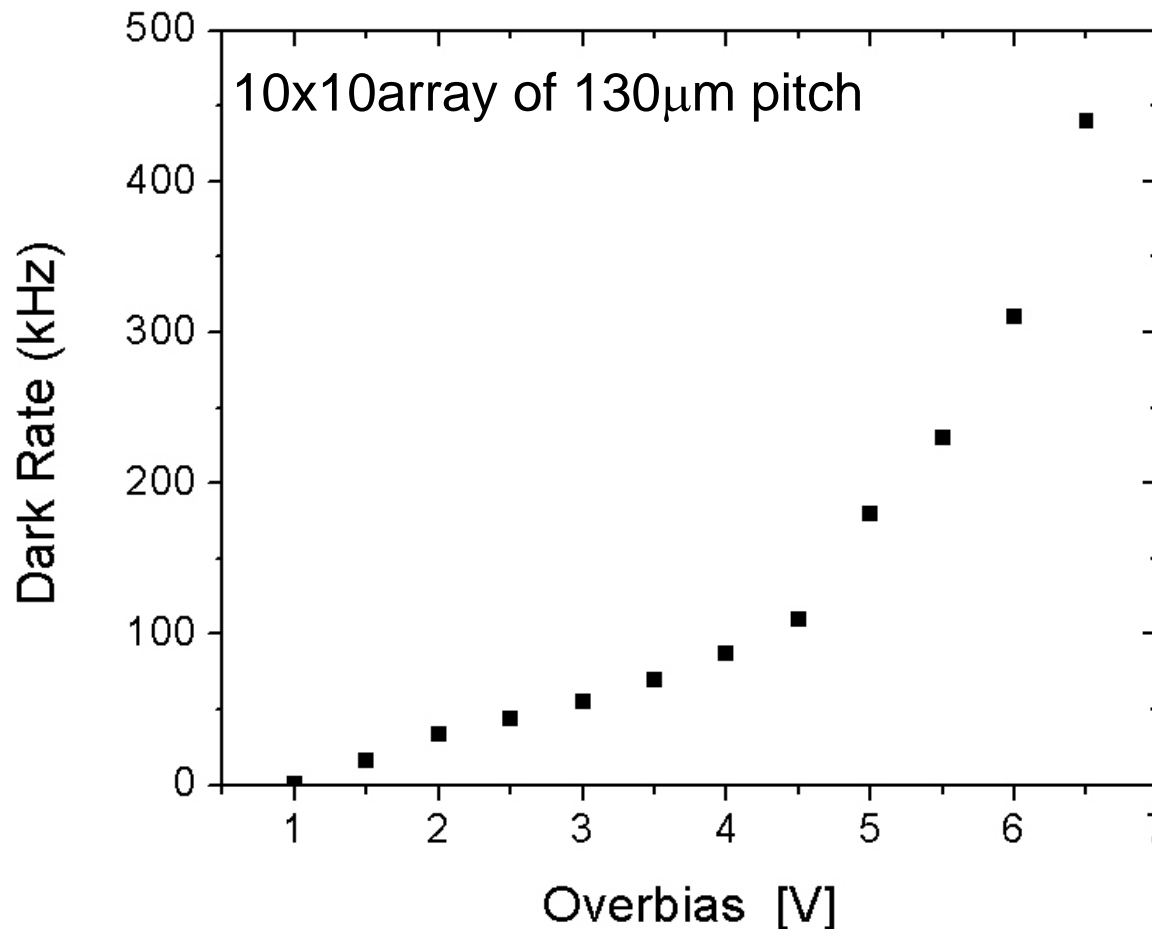
● Gain linearity

10x10 array of 130 μ m pitch @ -30 $^{\circ}$ C



● Dark rate

Due to the non optimal process sequence of the high field processing ~10MHz @300K for 4V overbias



Normal operation up to 4.5V overbias @227K

● Fill factor & Cross Talk & Photon Detection Efficiency



Produced SiMPI devices have the world record in the fill factors!

Pitch / Gap	Fill factor	Cross talk meas. ($\Delta V=2V$)	PDE calc. ($\Delta V=2V$)	PDE calc. ($\Delta V=5V$)
130 μm / 10 μm	85.2%	29%	39%	61%
130 μm / 11 μm	83.8%	27%	38%	60%
130 μm / 12 μm	82.4%	25%	37%	59%
130 μm / 20 μm	71.6%	15%	32%	52%

PDE estimate:

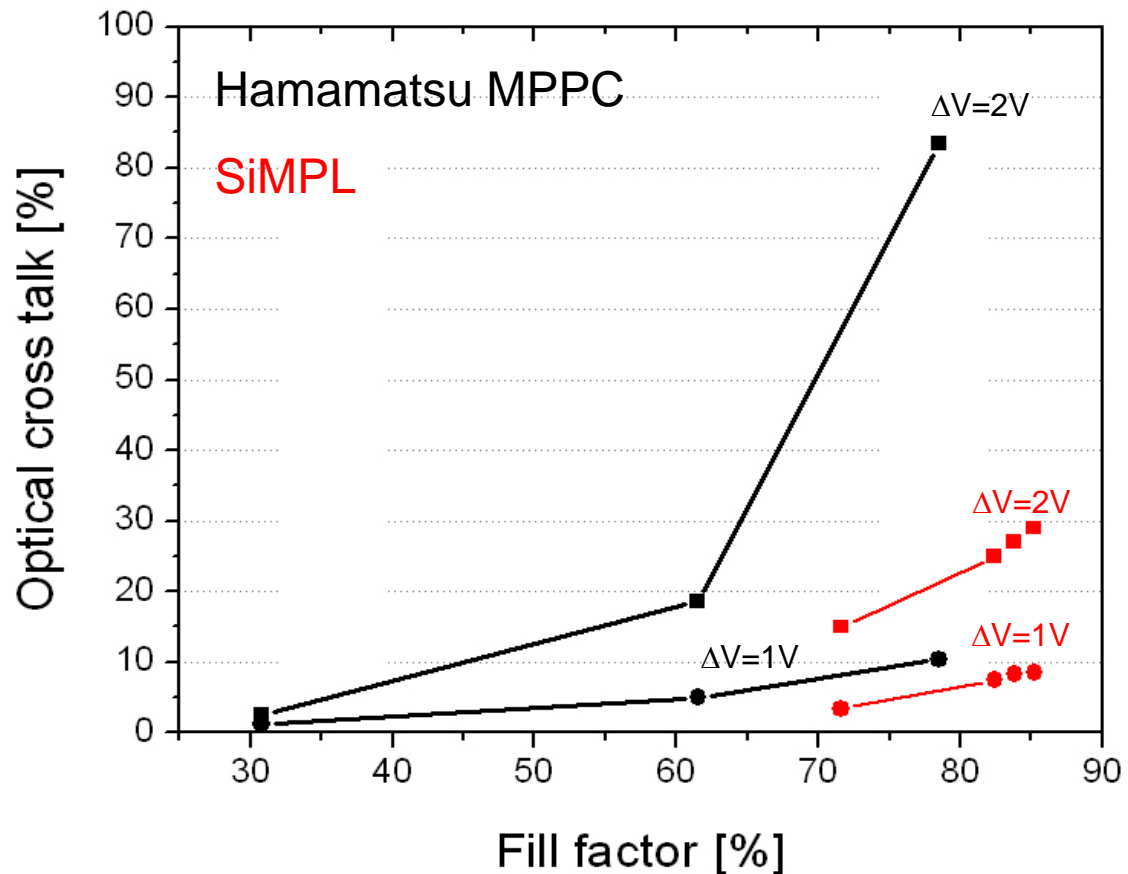
- Optical entrance window: 90% @400nm
- Geiger efficiency : 50% @ 2V overbias

80% @5V overbias

● Fill factor & Cross Talk

Produced SiMPI devices have the world record in the fill factors and still lower cross talk!

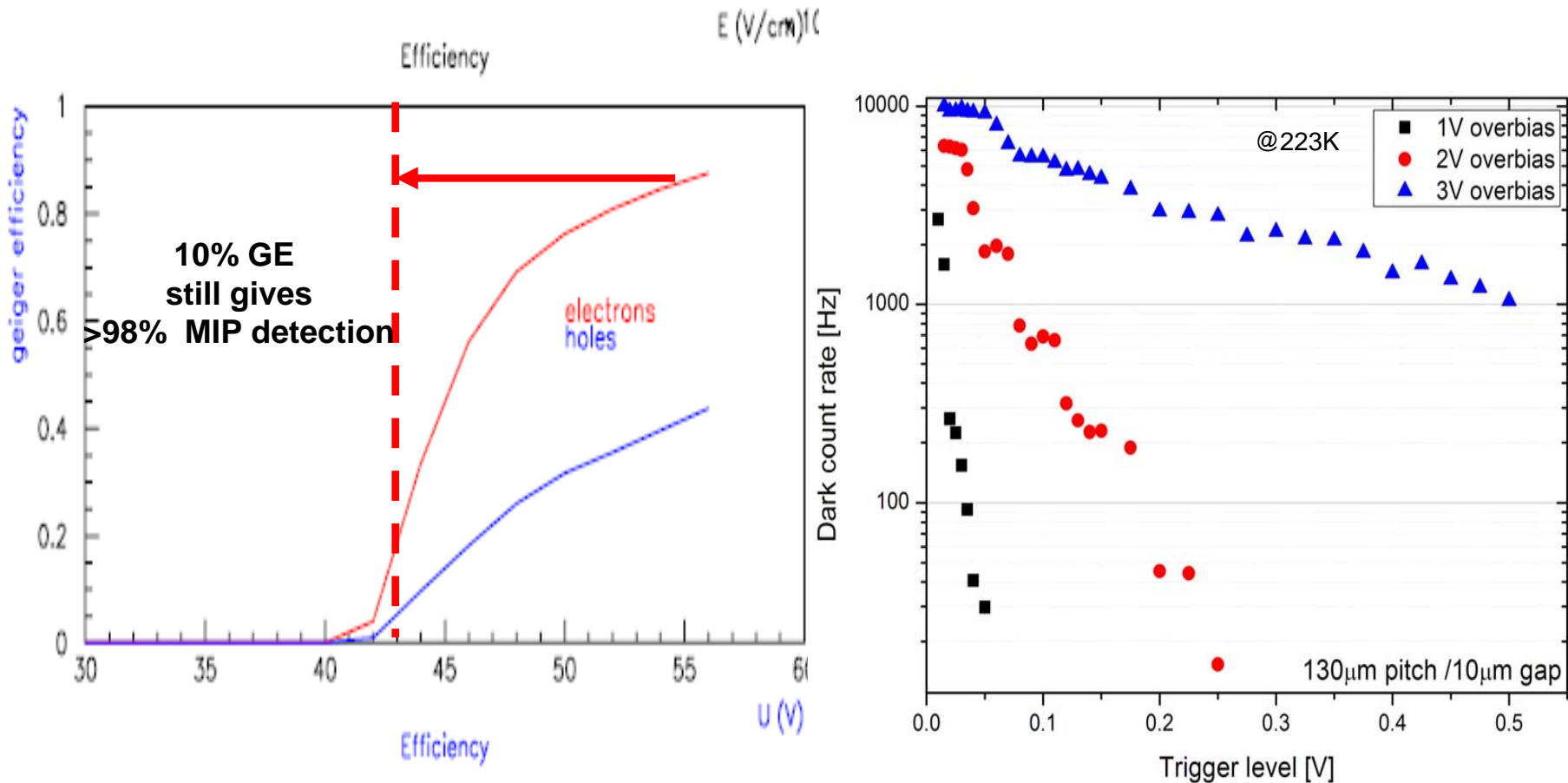
No special cross talk suppression technology applied
just intrinsic property of SiMPI devices



● Detection of particles

Excellent time stamping due to the fast avalanche process (<1ns)

MIP gives about 80pairs/ μm \rightarrow huge signal in SiPM \rightarrow allows operation at small ΔV



Reduction of dark rate and cross talk by order of magnitude

● Detection of particles



Dark rate: $1 \text{ MHz/mm}^2 = 1 \text{ hit}/\mu\text{m}^2/\text{s} = O(\text{Belle II})$

With $20 \mu\text{m}$ pitch and 12 ns time stamp: occupancy: 2.5×10^{-6}

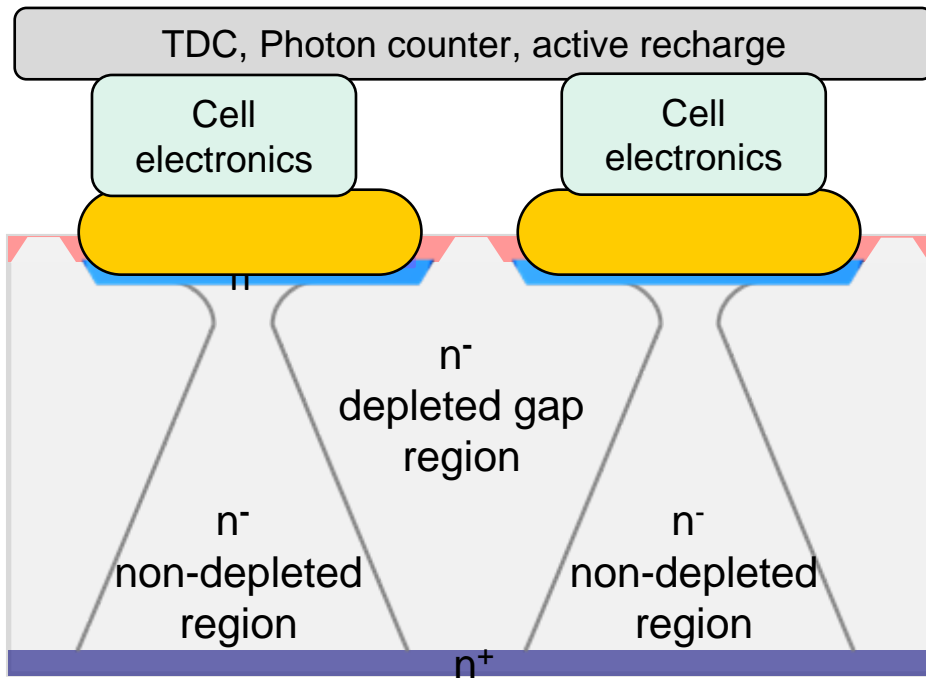
Power (analogue): $\sim 5 \mu\text{W/cm}^2$

Dominated by dark rate

Possible problems:

- Radiation hardness (dark rate increases due to bulk damage)
- Cross talk
- Efficiency (fill factor)
- Digital power

● Next generation SiMPI devices



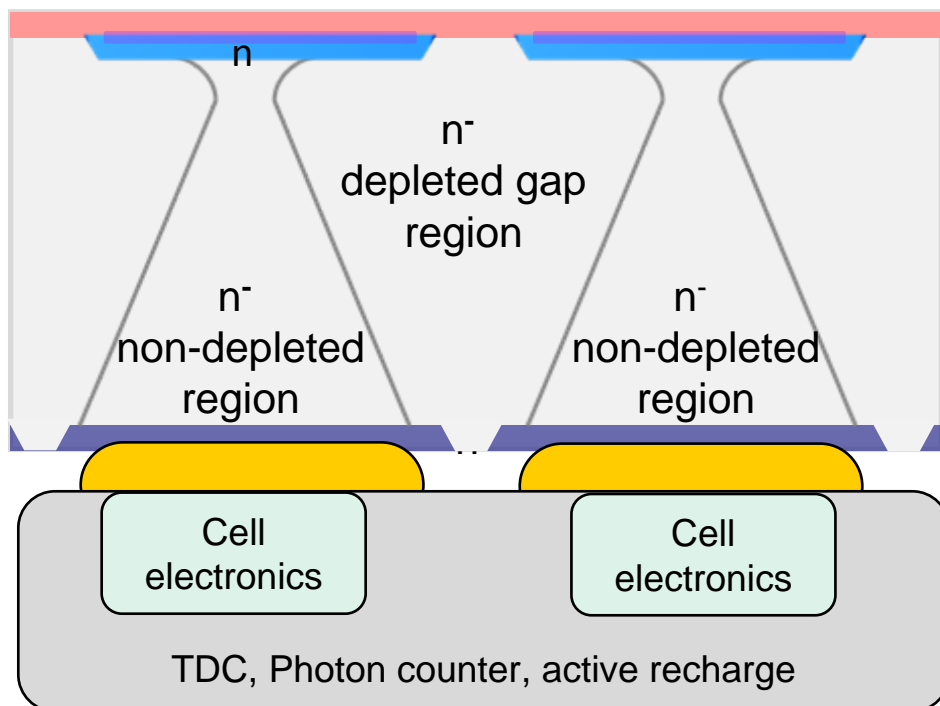
Topologically flat surface

High fill factor

Adjustable resistor value

Pitch limited by the bump bonding

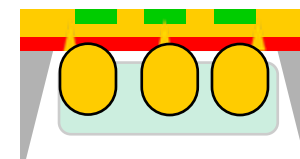
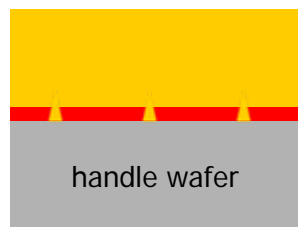
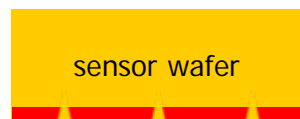
● Next generation SiMPI devices



Topologically flat and free surface

High fill factor

Sensitive to light



1. Structured implant on backside on sensor wafer

2. bond sensor wafer to handle wafer

3. thin sensor side to desired thickness

4. process SiMPI arrays on top side

● Summary



Silicon photomultiplier array with individual quench resistors, integrated into the silicon bulk - SiMPI detector

- Required flexibility for quench resistor adjustment comes with wafer bonding technique (for small pixels an epitaxial layer is also suitable)
- No polysilicon resistors, contacts and metal necessary at the entrance window
- Geometrical fill factor is given by the need of cross talk suppression only
- Very simple process, relaxed lithography requirements
- Very attractive → idea already used by other groups ☺

Prototype production finished – quenching works , first measurements very promising, functional devices with very high fill factor and low cross talk

Next generation SiMPI devices with electronics interconnected

- on front side can be used for trackers at future colliders
- on back side → high sensitivity, high fill factor digital SiPM

Thank you for your attention!