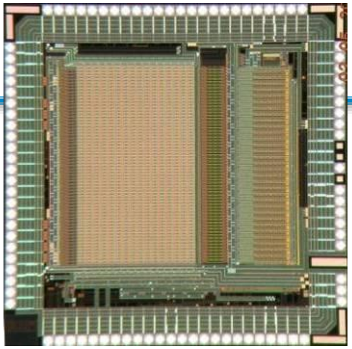
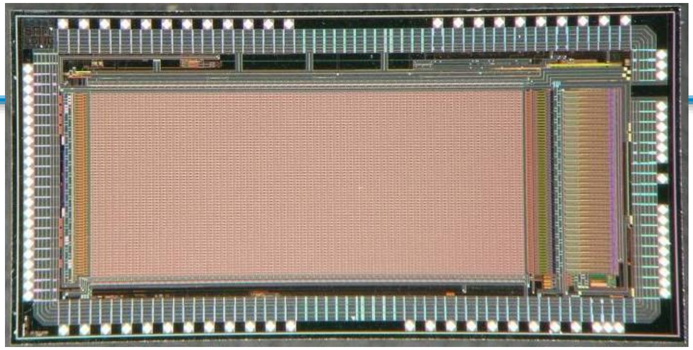
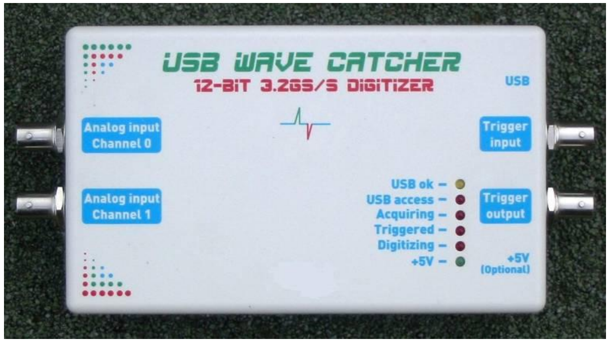




USING ULTRA FAST ANALOG MEMORIES FOR FAST PHOTO-DETECTOR READOUT

D.Breton & J.Maalmi (LAL Orsay), E.Delagnes (CEA/IRFU)



NDIP 2011

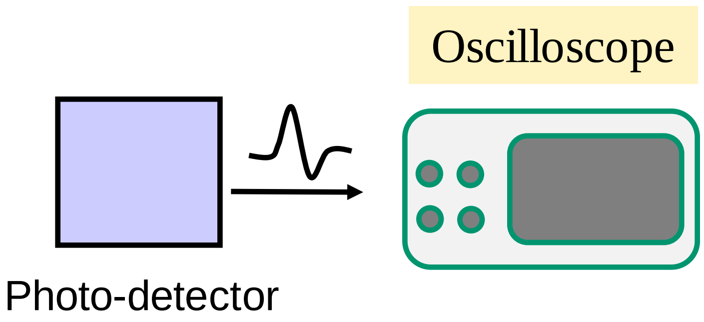
Introduction

- **Photo-detectors** are implied in all kinds of applications. Associated electronics can be used either for their **characterization** (test benches) or for their **readout** (experiments).
- For **test benches**:
  - Ultimate performance of the electronics is requested
  - If the number of channels is small (≤4), then high-end oscilloscopes can be used, but they are expensive.
  - If the **number of channels increases**, and if one wants to study all of them in parallel, difficulties occur.
- For **physics experiments:**
  - Usually, **dedicated ASICs** are used
  - They shape the signal and then permit Amplitude, Charge and/or Time measurement
- But, what happens if:
  - **Time measurement** precision has to **better than 30ps rms** ?
  - One wants to **measure A, Q and/or T**, but also see the **waveforms** on demand ?

The measurement chain

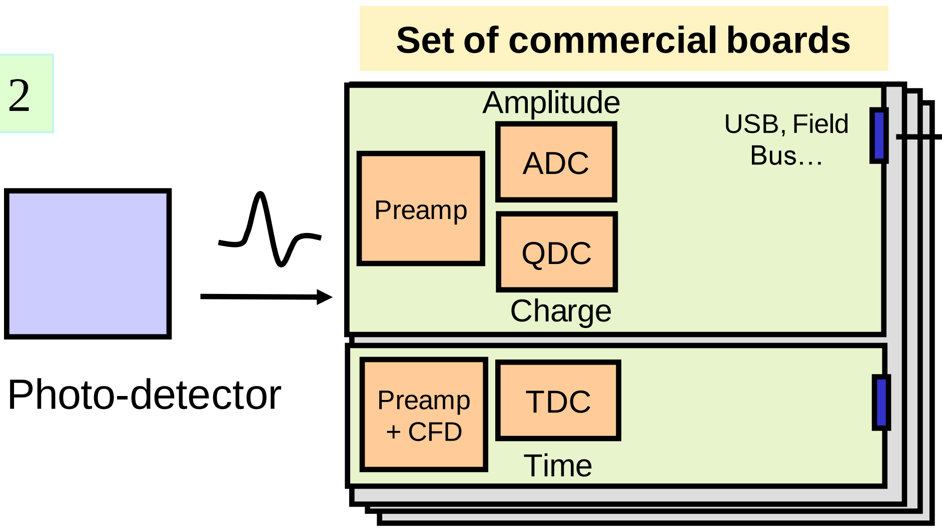
Choice of measurement chain is driven by the ratio performances/cost per channel

Option 1

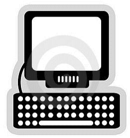


- Simplest solution
- All measurements possible
- But limited to 4 channels
- Cost per channel: ≥ 5 k€

Option 2



Control & readout

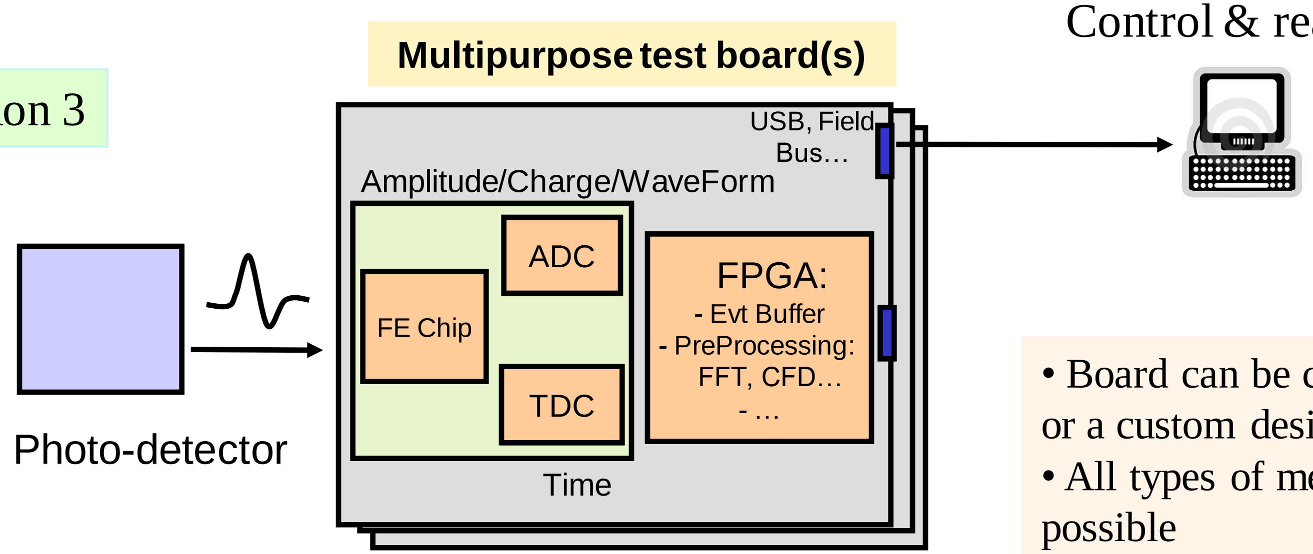


- Best performances
- May require many different boards
- Cost per channel: few k€ up to > 10 k€ (GS/s ADCs)

Using multipurpose boards

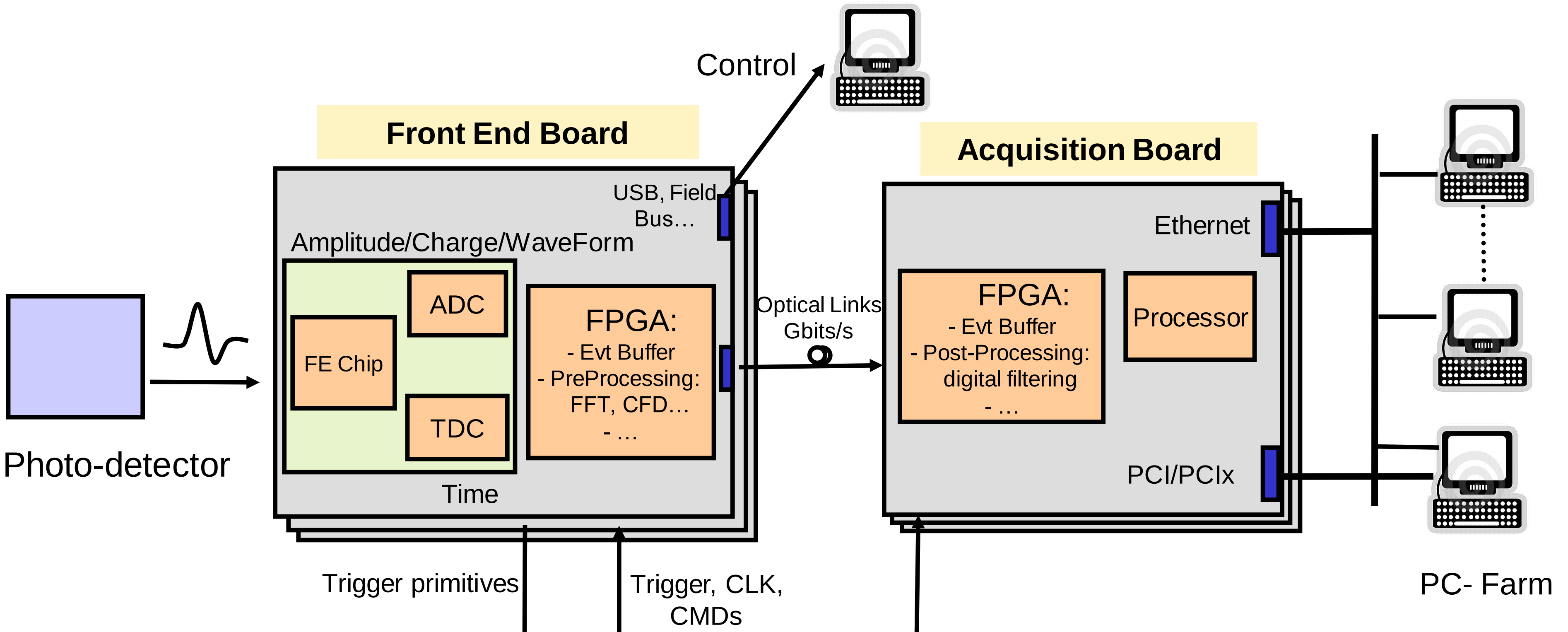
Control & readout

Option 3



- Board can be commercial or a custom design
- All types of measurements possible
- But limited by the performances of the different ASICs
- Cost per channel: few 100 € to few k€

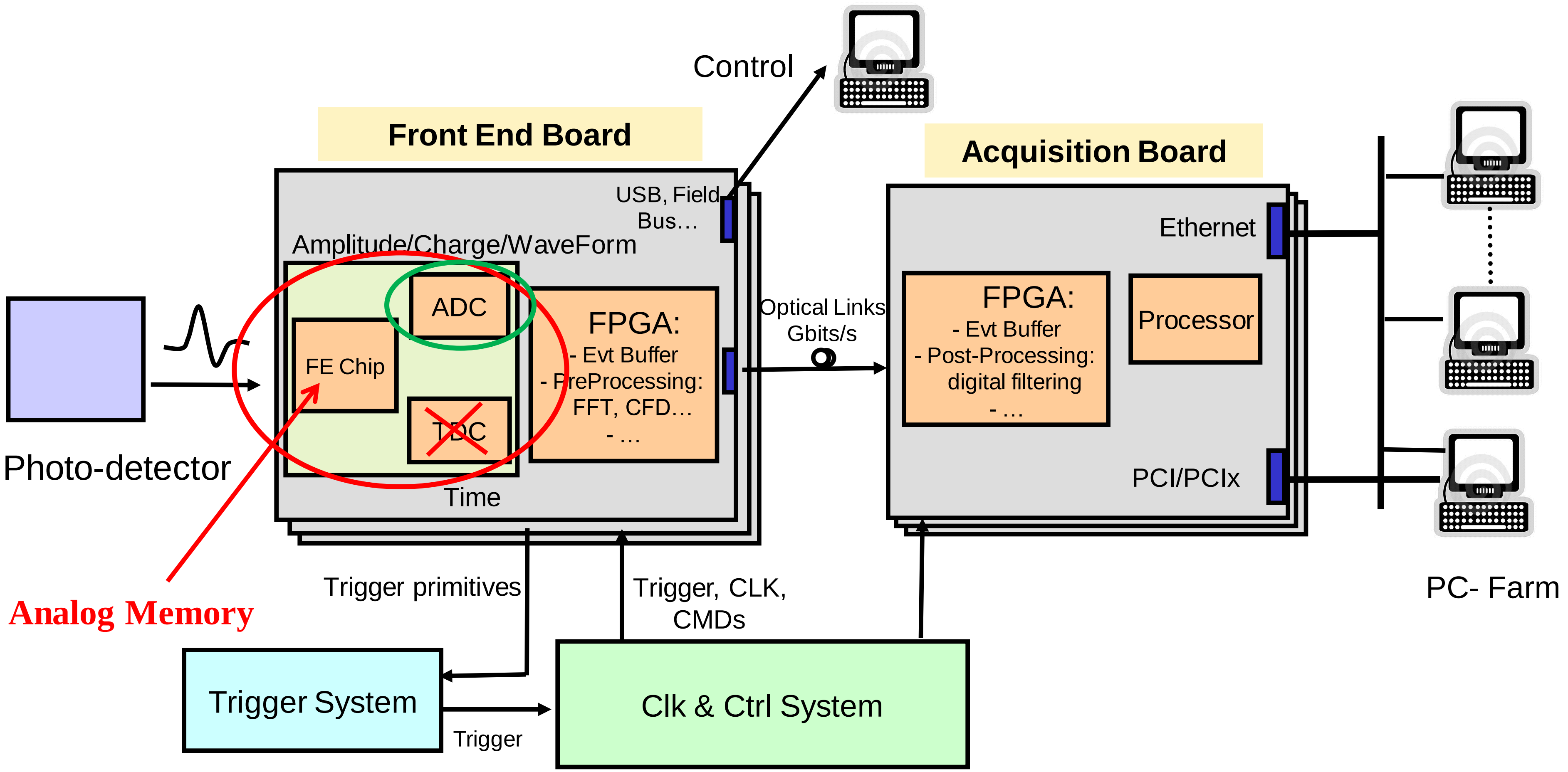
Case of a big physics experiment



- Cost per channel is dominant: has to be a few 100 € max
- Measurements and performances are adapted to physics requirements

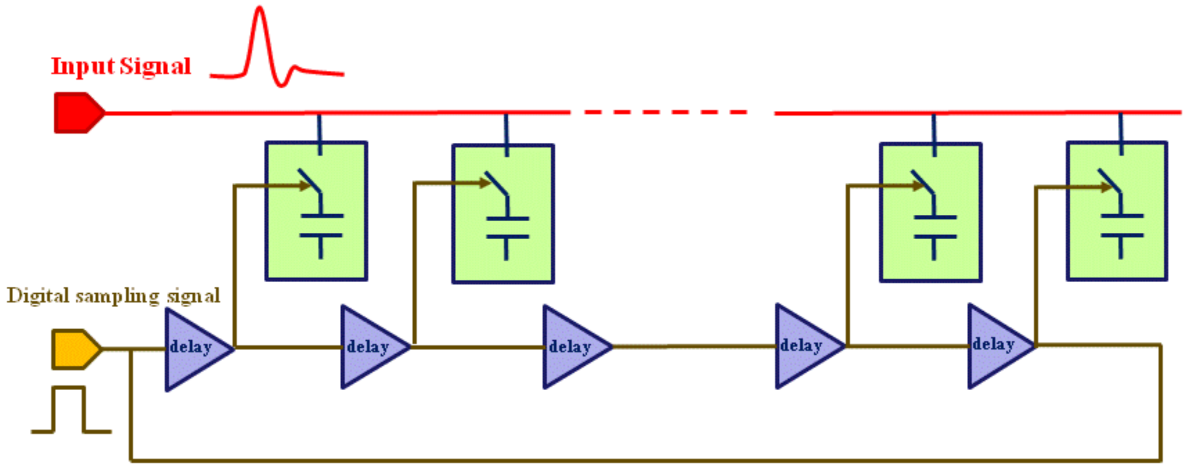
Introducing analog memories

Using analog memories permits measuring the time (no more need fot TDC) and relaxes the requirements on the ADC

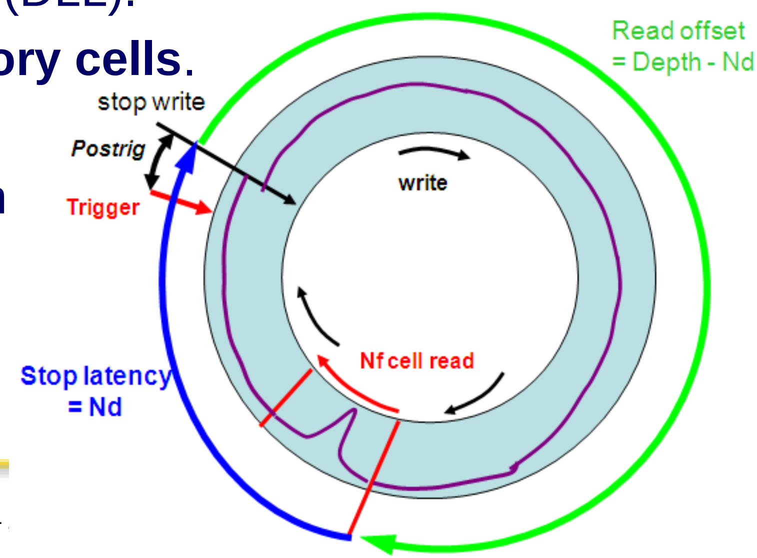


Circular analog memories: basic principles

An analog memory can record waveforms at very high sampling rate (>>GS/s)
After trigger, they are digitized at a much lower rate with an ADC (~20 MHz)



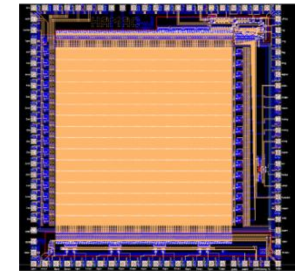
- A write pulse is running along a folded **delay line** (DLL).
- It drives the recording of signal into **analog memory cells**.
- Sampling stops upon **trigger**.
- **Readout** can target an area of interest, which can be only a **subset** of the whole channel
- **Dead time** due to readout has to remain as small as possible **(<100ns / sample)**.



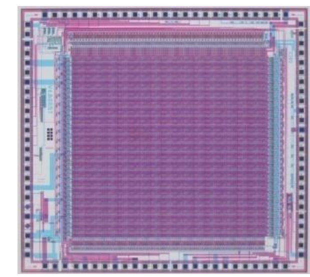
Our favourite solution: a Sampling Matrix

- We started designing analog memories in 1992 with the first prototype of the Switched Capacitor Array (SCA) for the ATLAS LARG calorimeter. 80000 chips produced in 2002, now on duty on the LHC.
- Since 2002, 3 new generations of fast samplers have been designed (ARS, MATACQ, SAM): total of more than 30000 chips in use.

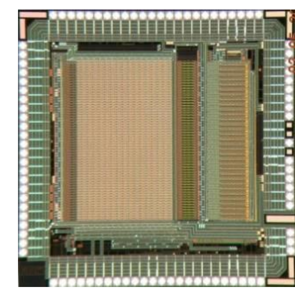
HAMAC



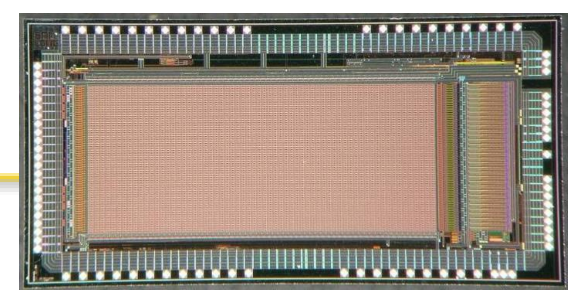
MATACQ



SAM

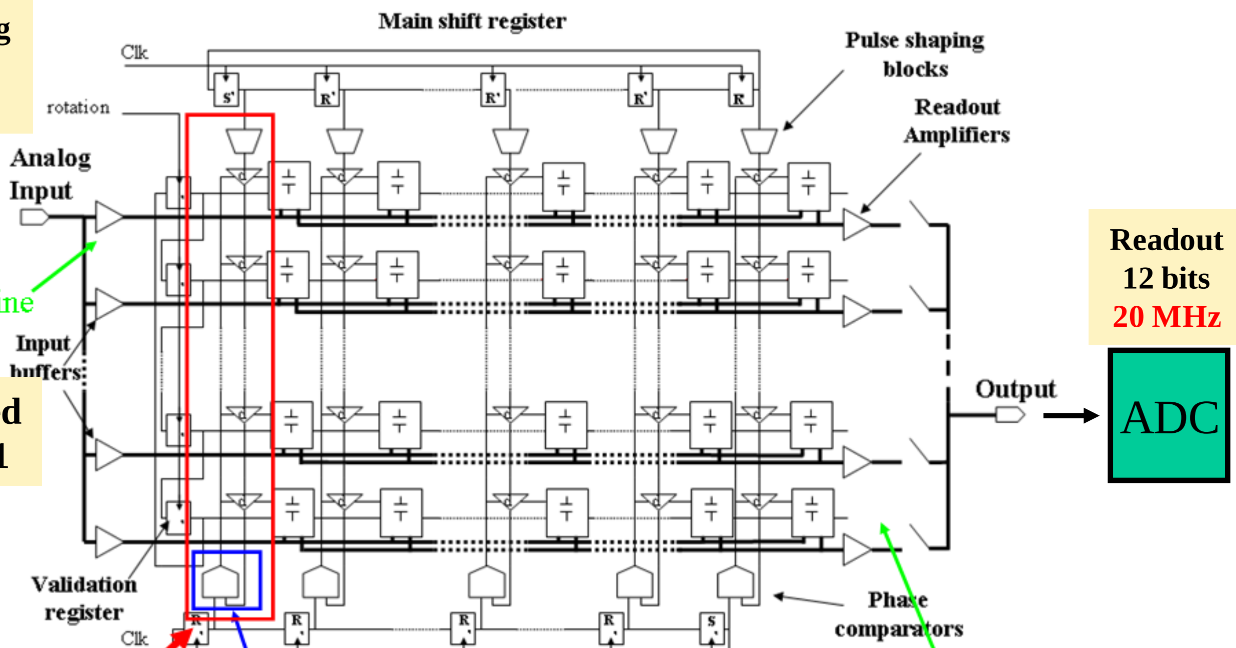


SAMLONG



Sampling at 3.2GS/s

Patented in 2001



Readout 12 bits 20 MHz

short DLL: less jitter

1 delay servo-control /col: stability

Parallelized Readout

See Eric Delagnes's poster on Friday

Analog memories vs ADCs

- **Analog memories** actually look like perfect candidates for **high precision measurements** at **high scale**:
  - Like ADCs they catch the signal waveform (this can also be very useful for debug)
  - TDC is built-in (position in the memory gives the time)
  - Only the useful information is digitized (vs ADCs) => **low power**
  - Any type of digital processing can be used
  - Main difficulty is less sampling frequency than signal **bandwidth**
- Their drawbacks:
  - The limited recording **depth**
  - The readout **dead-time**
- But:
  - Only a few samples/hit can be read => this may limit the dead time
  - **Simultaneous write/read** operation is feasible, which may further reduces the dead time if necessary

The USB_WaveCatcher board (V6)

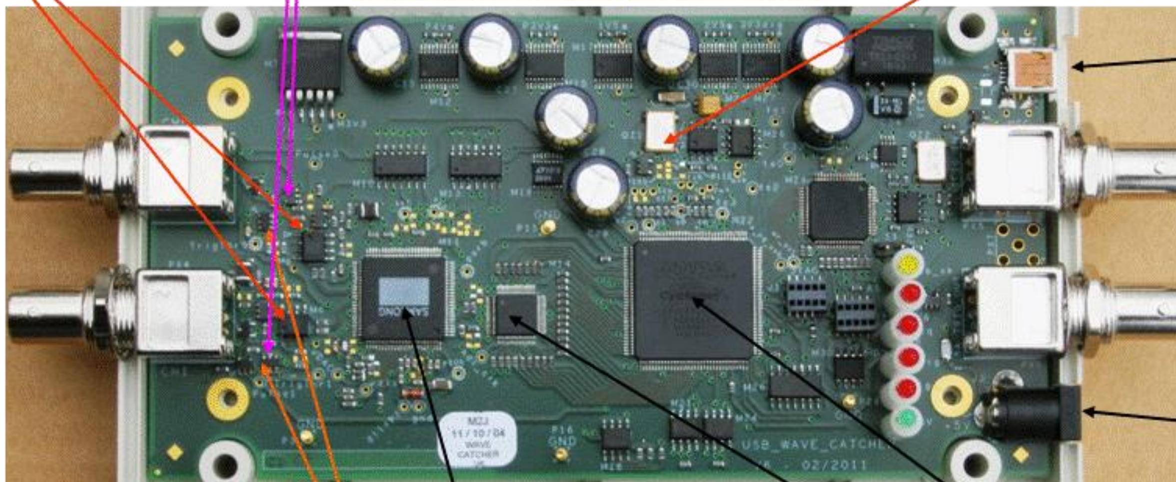
Pulsers for reflectometry applications

1.5 GHz BW amplifier.

Board has to be powered by USB
=> power consumption ≤ 2.5W

Reference clock:
200MHz => **3.2GS/s**

2 analog inputs. DC Coupled.



µ USB

Trigger input

Trigger output

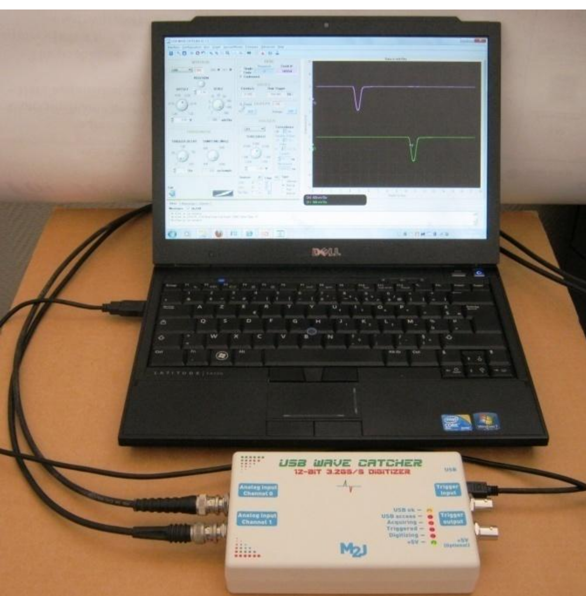
+5V Jack plug

SAM Chip

Cyclone FPGA

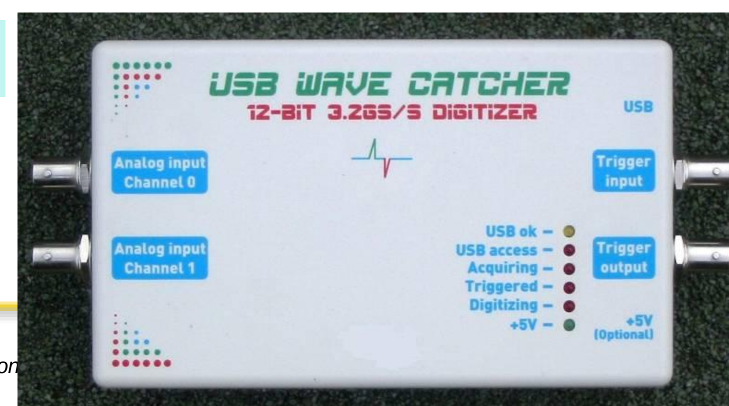
Trigger discriminators

Dual 12-bit ADC



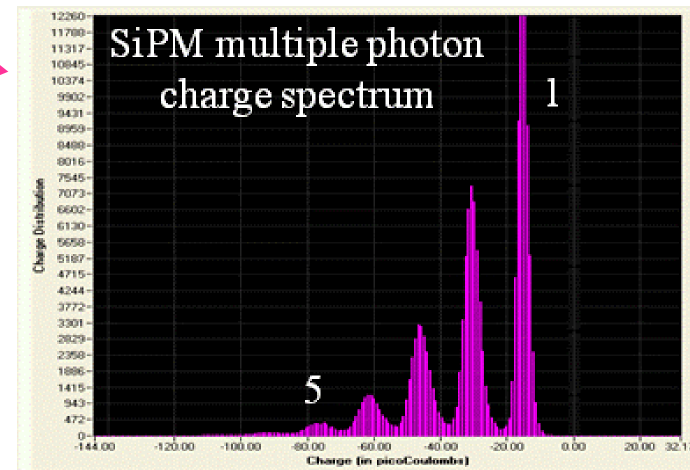
The autonomous test bench

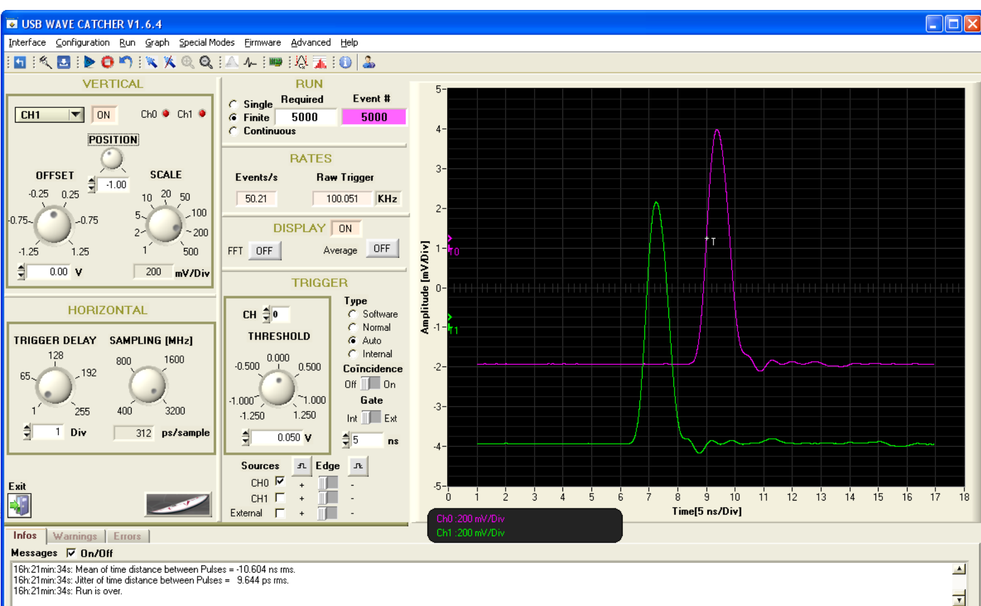
The module



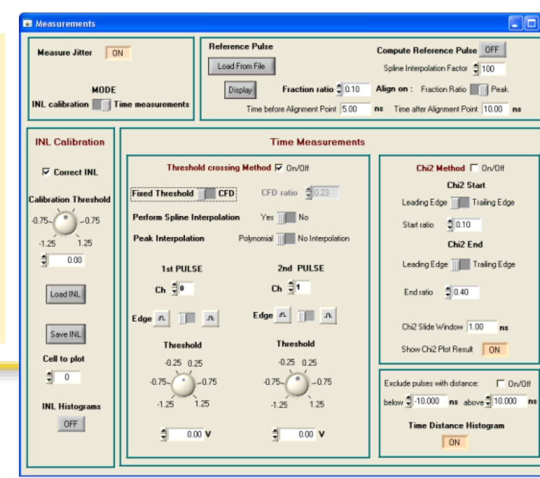
Board Specific Features

- Possibility to add **an individual DC offset** on each signal
- Individual **trigger discriminator** on each channel
- External and internal trigger + numerous modes of **triggering on coïncidence** (11 possibilities including two pulses on the same channel) => useful for afterpulse studies
- **Real time trigger counting** independent of acquisition rate
- **Embedded charge mode** (integration starts on threshold or at a fixed location) => high rates (~ a few 10 kEvents/s)
- **Embedded pulse generators** for reflectometry applications

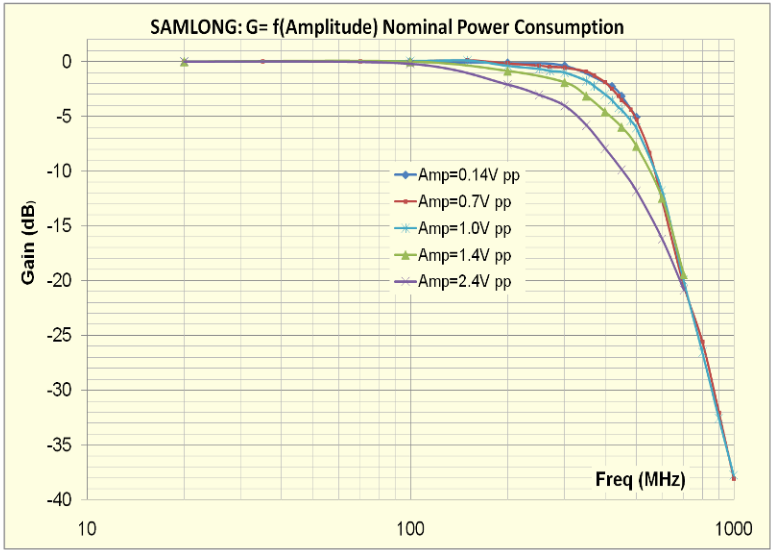


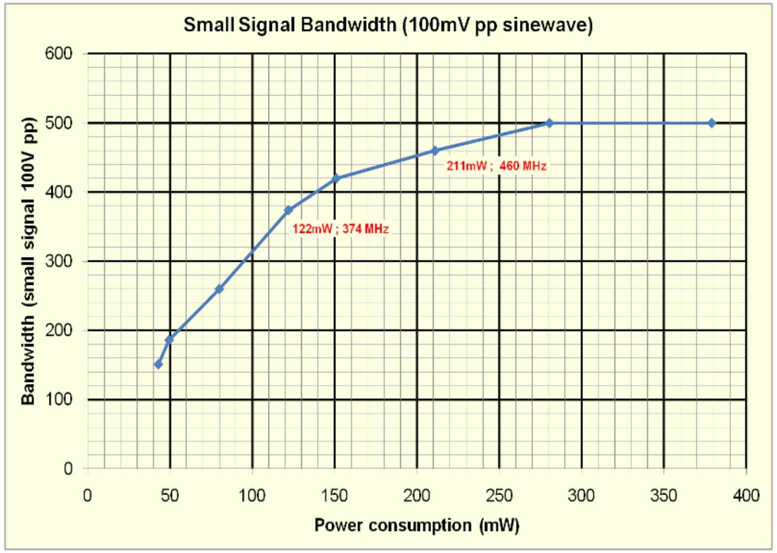


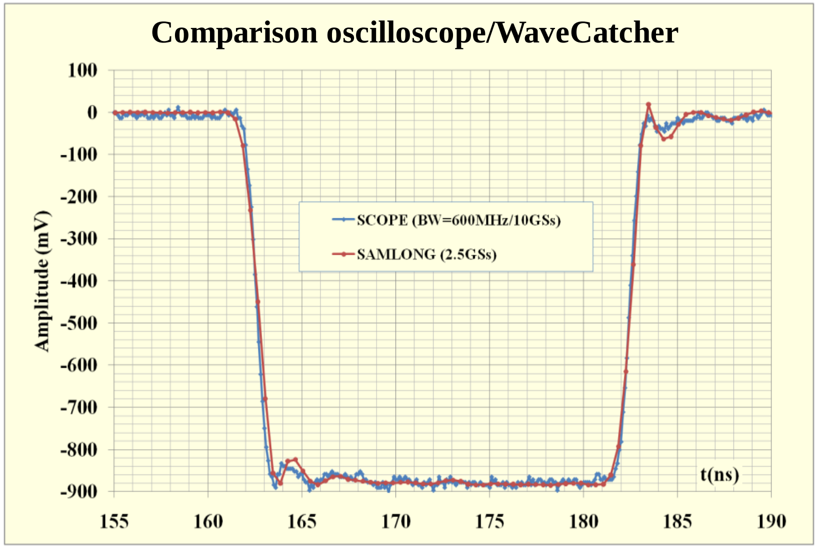
This oscilloscope-like software was developed by the team.

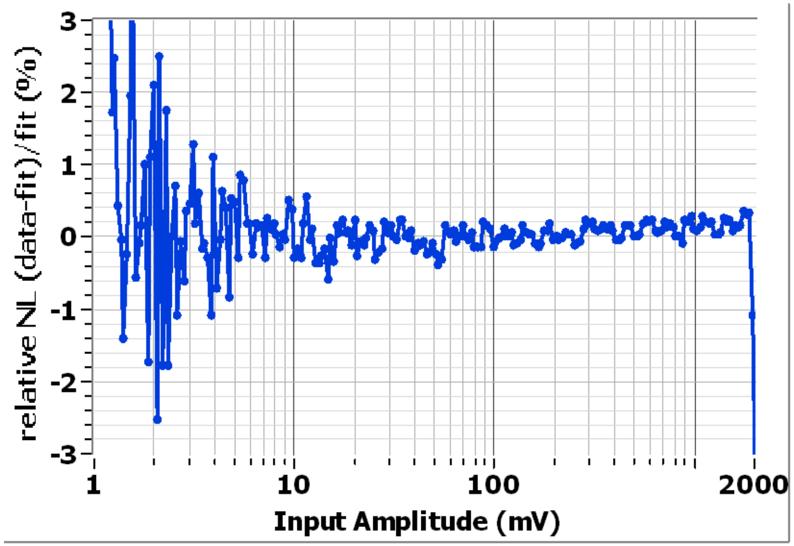


Board performances: examples





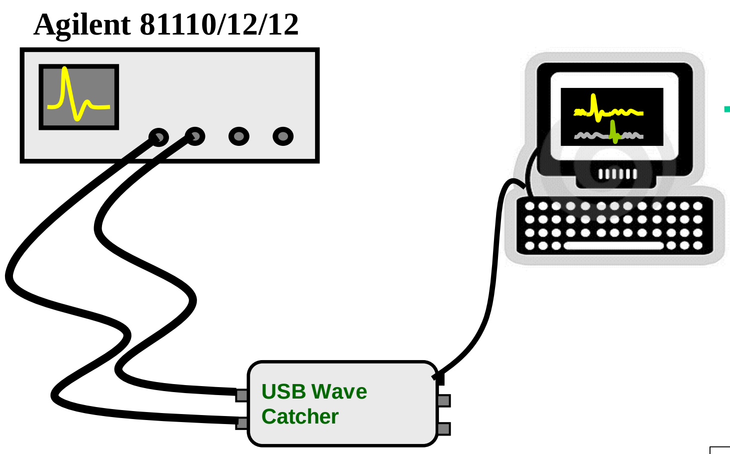


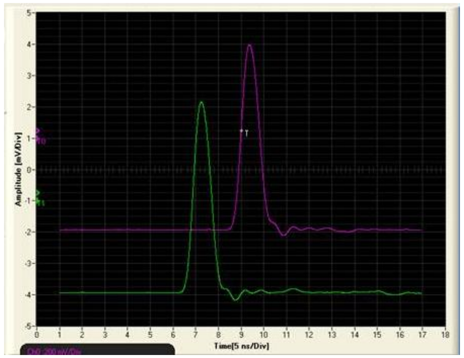


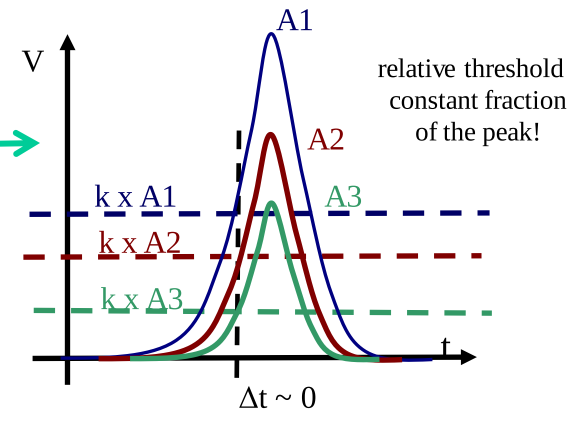
Time characterization with digital CFD method

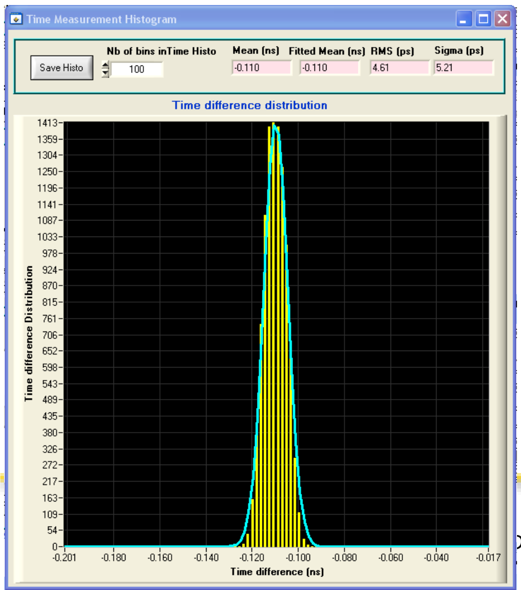
- Source: randomly distributed set of two positive pulses
- Results are the same with negative pulses or distance between arches of a sine wave

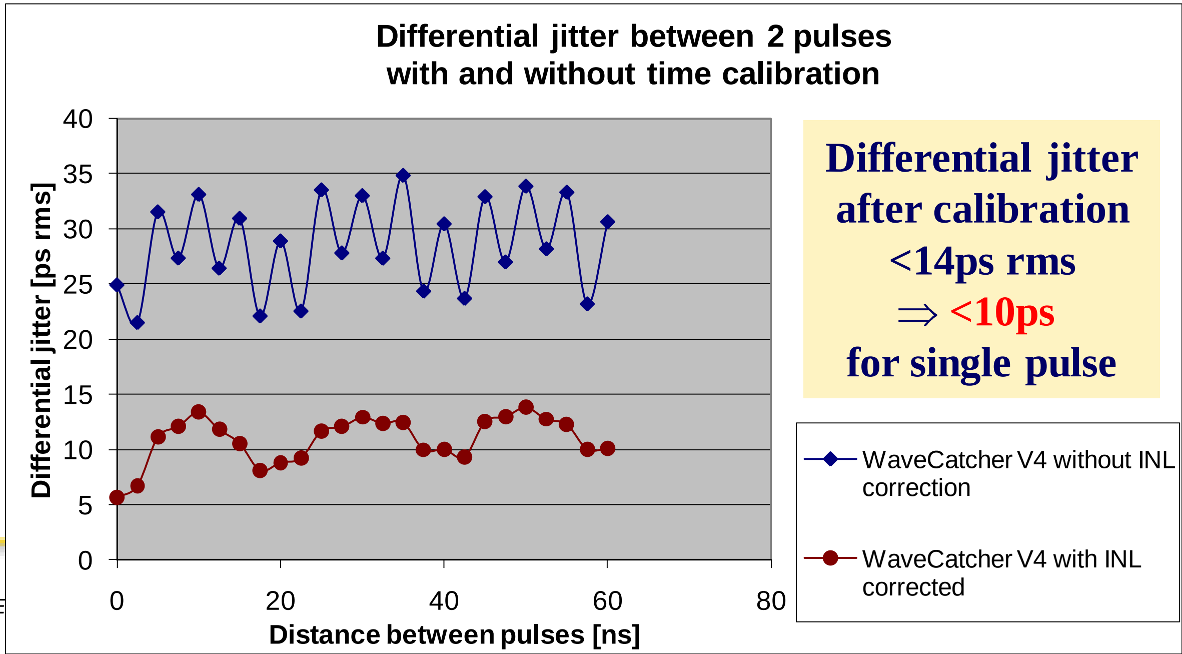
Constant Fraction Discriminator







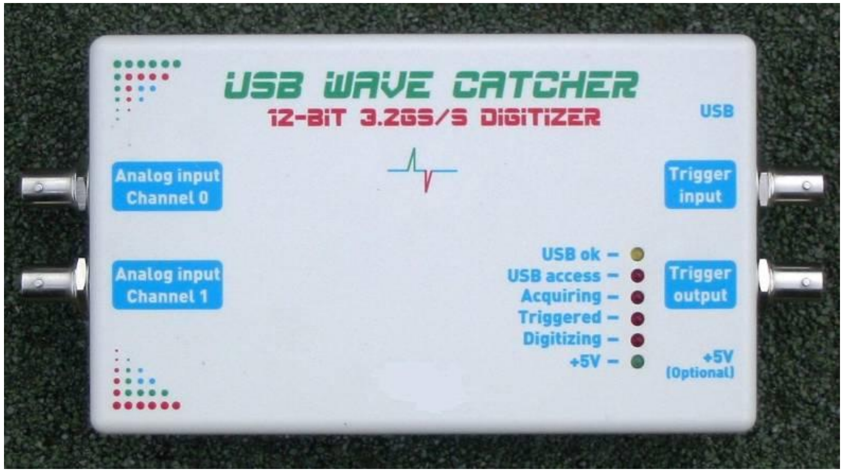




Differential jitter after calibration <14ps rms
⇒ <10ps
for single pulse

Summary of the WaveCatcher performances.

- **2** DC-coupled **256/1024-deep channels** with 50-Ohm active input impedance
- **1.25V** dynamic Range, with full range 16-bit individual tunable offsets
- 2 individual **pulse generators** for test and reflectometry applications.
- On-board **charge integration** calculation.
- Integrated **raw trigger rate** counters
- **Bandwidth ~ 500MHz**
- **Signal/noise ratio**: **11.8 bits rms**
  (noise = **650 µV RMS**)
- **Sampling Frequency**: **400MS/s to 3.2GS/s**
- Max consumption on +5V: **0.5A**



- **Absolute time precision** in a channel (typical):
  - without time calibration: ~20ps rms (3.2GS/s)
  - **after time calibration** **~10ps rms** (3.2GS/s)
- **Relative time precision** between channels: **<5ps rms**.
- **Trigger sources**: software, external, internal, threshold on signals,
- **11 modes of trigger** coincidence
- Acquisition rate (**full events**) Up to **~1 kHz** over 2 full channels
- Acquisition rate (**charge mode**) Up to **~10 kHz** over 2 channels

Applications to photo-detectors:

(the WaveCatcher around the world)

MCP-PMT characterization: NIM paper published

Nuclear Instruments and Methods in Physics Research A 629 (2011) 123–132

Contents lists available at ScienceDirect

Nuclear Instruments and Methods in Physics Research A

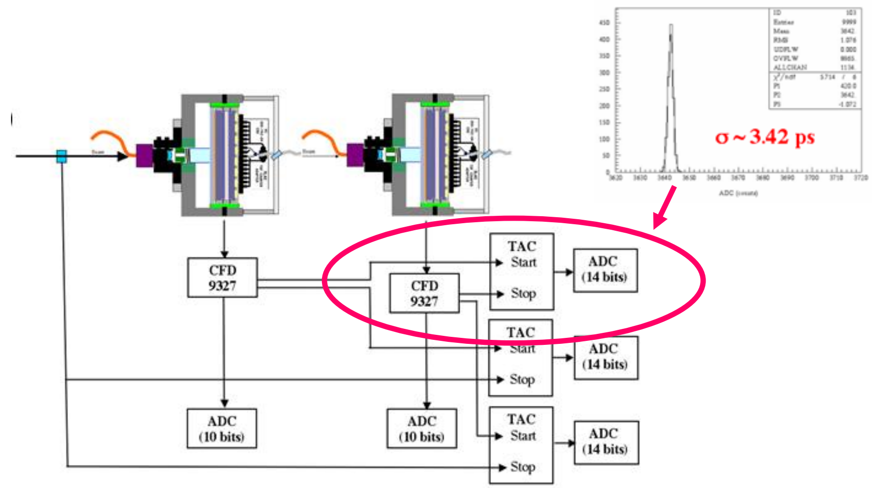
journal homepage: www.elsevier.com/locate/nima

Fermilab test beam setup
Burle/Photonis MCP-PMTs with 10 µm pores
~40pe and low gain (2-3 10^4)

High resolution photon timing with MCP-PMTs: A comparison of a commercial constant fraction discriminator (CFD) with the ASIC-based waveform digitizers TARGET and WaveCatcher ☆

D. Breton [d], E. Delagnes [c], J. Maalmi [d], K. Nishimura [b], L.L. Ruckman [b], G. Varner [b], J. Va'vra [a,*]

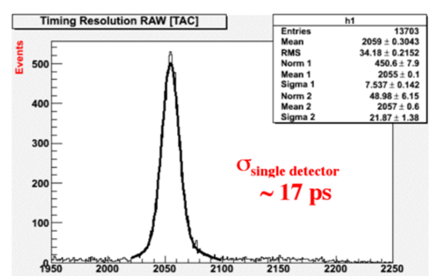
[a] SLAC National Accelerator Laboratory, CA, USA
[b] University of Hawaii, USA
[c] CEA/Irfu Saclay, France
[d] Laboratoire de l'Accélérateur Linéaire, Orsay, CNRS/IN2P3, France



Abstract: … The question we pose in this paper is **if new waveform digitizer ASICs, such as the WaveCatcher** and TARGET, operating with a sampling rate of 2-3 GSa/s **can compete with 1GHz BW CFD/TDC/ADC electronics** …

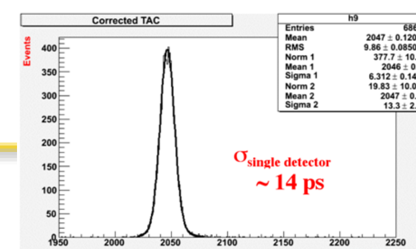
…

Conclusion: … The fact that **we found waveform digitizing electronics capable of measuring timing resolutions similar to that of the best commercially-available Ortec CFD/TAC/ADC electronics** is, we believe, a very significant result. It will help to advance the TOF technique in future.



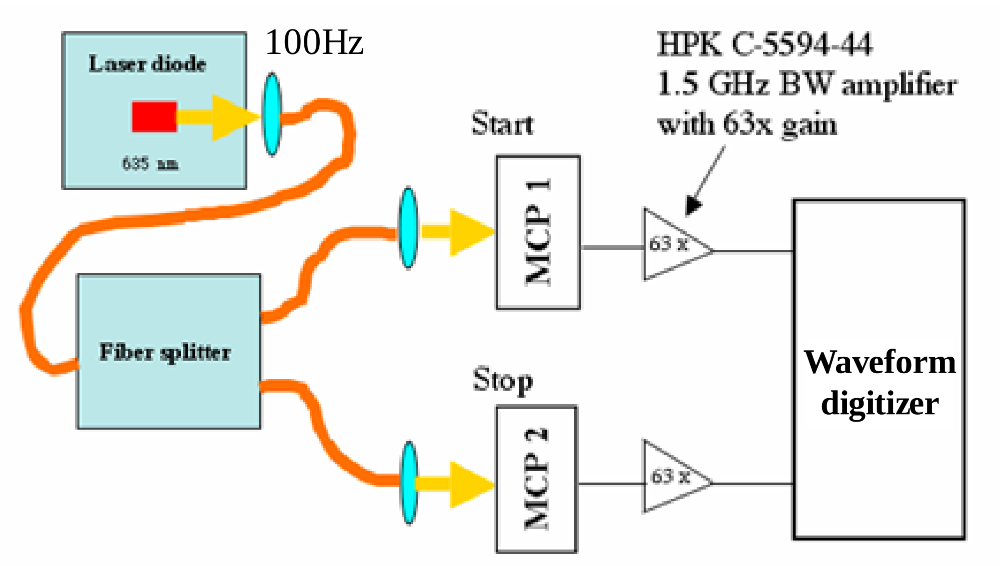
Raw CFD measurement

CFD with walk correction

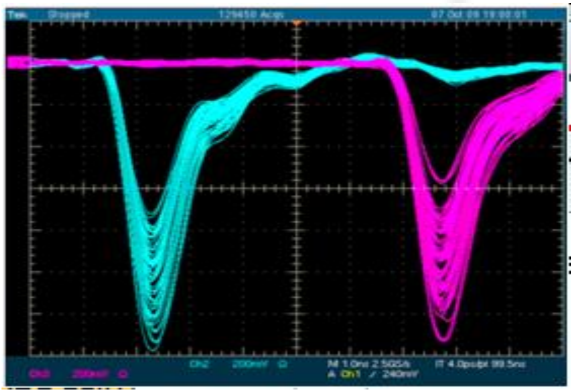


NIM paper: SLAC laser test

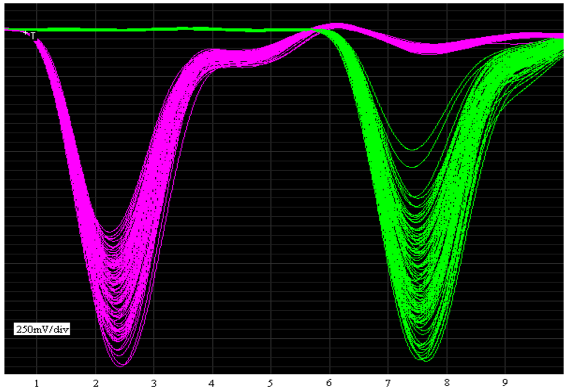
Same conditions as for Fermilab test:
40pe and low gain (2-3 10^4)



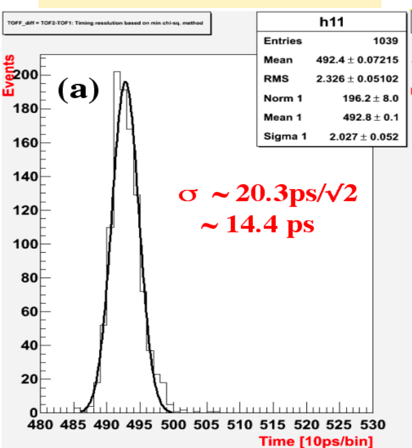
Tektronix oscilloscope



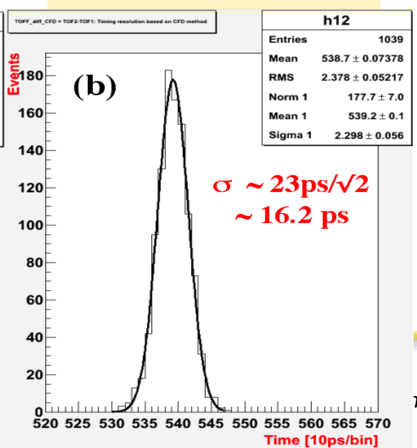
WaveCatcher Board

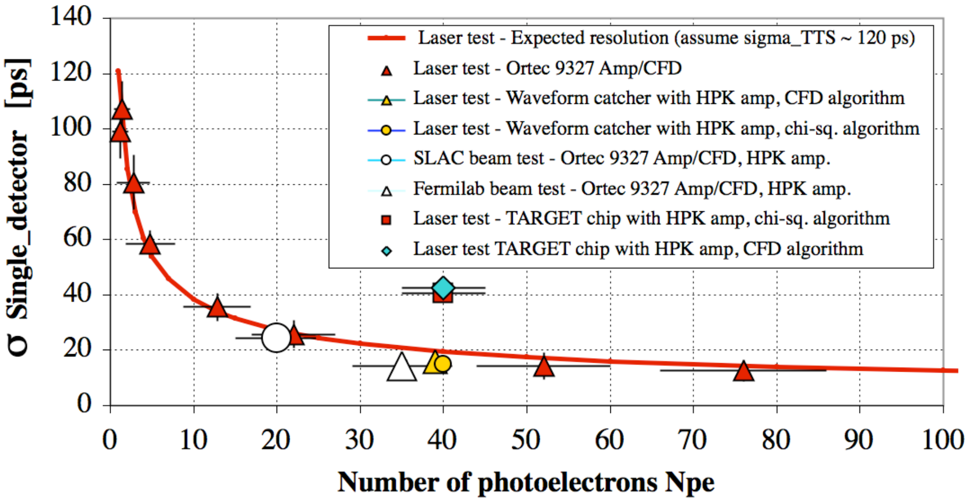


X² method:



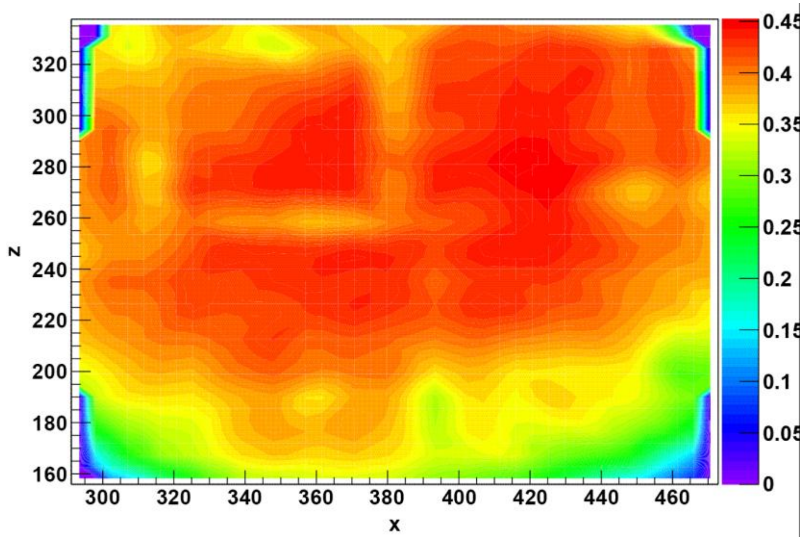
CFD method:

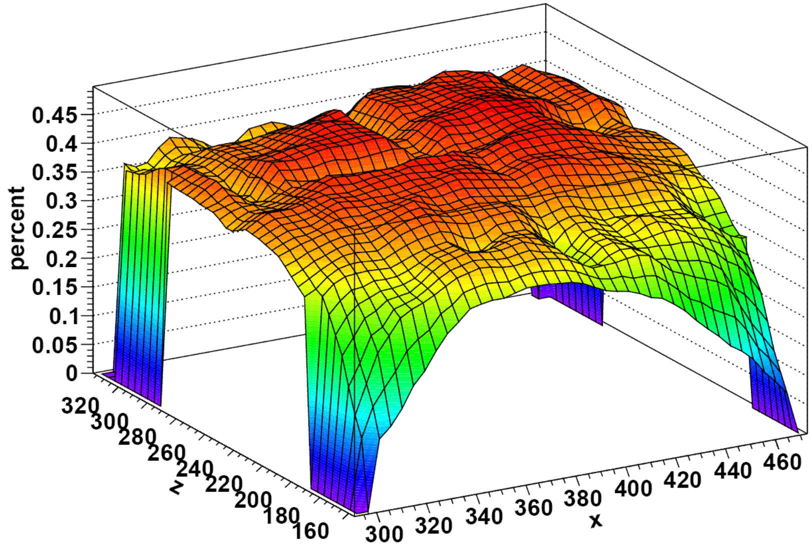




PM characterization at APC

- Goal is to precisely characterize the Antares opto-modules in single photoelectron mode
- **1,000,000 triggers** per measurement step
- 0.45% of triggers give a photoelectron (=> ~1.5% of statistical error)
- There are 289 measurement steps spaced by 1cm (3 degrees of aperture on the optical module) starting from its center
- Using the **integrated charge mode**, reading out the 289,000,000 events takes only 2h30.

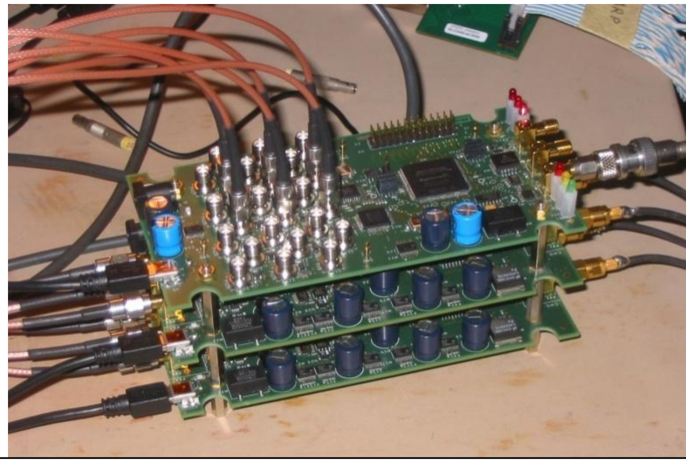




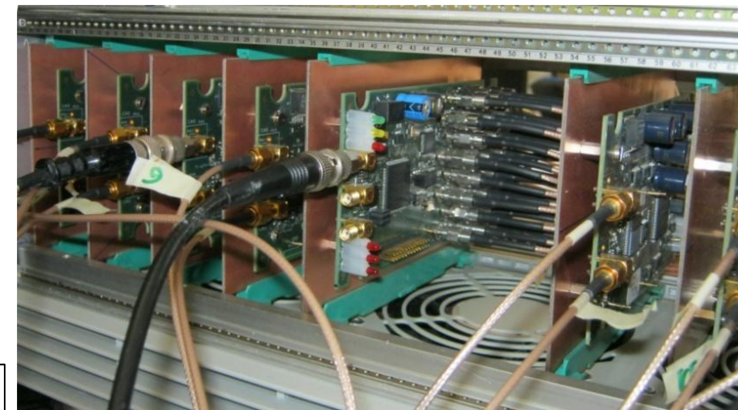
Increasing the number of channels …

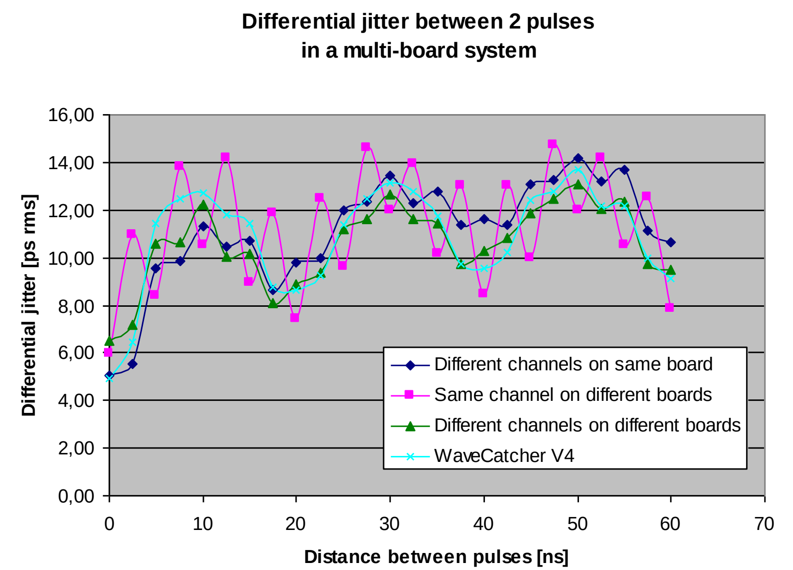
- We decided to build a synchronous **16-channel** acquisition system based on **8 two-channel WaveCatcher** V5 boards
- Technical challenge: to **keep the 10ps time precision** at the crate level

4-channel prototype



16-channel crate

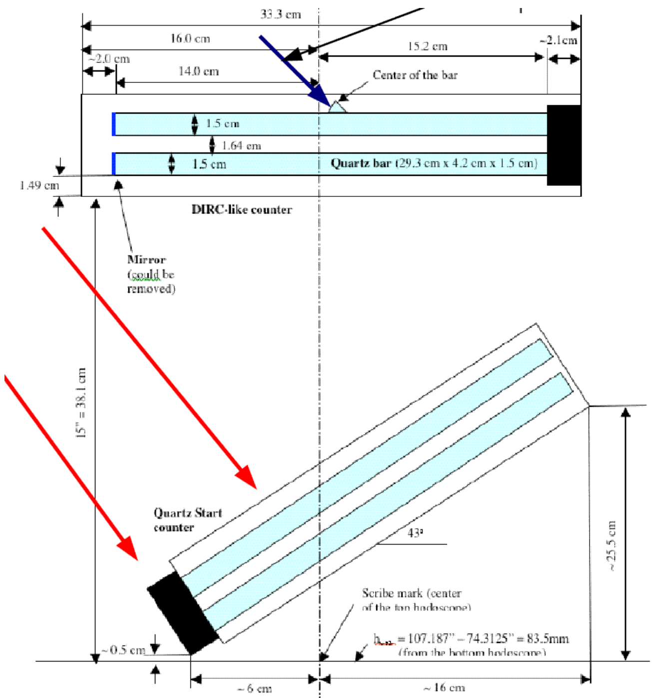


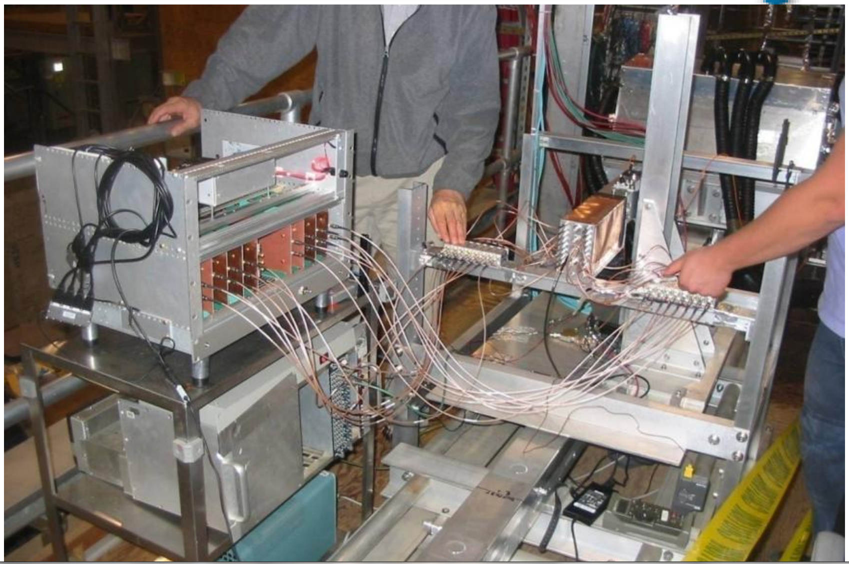


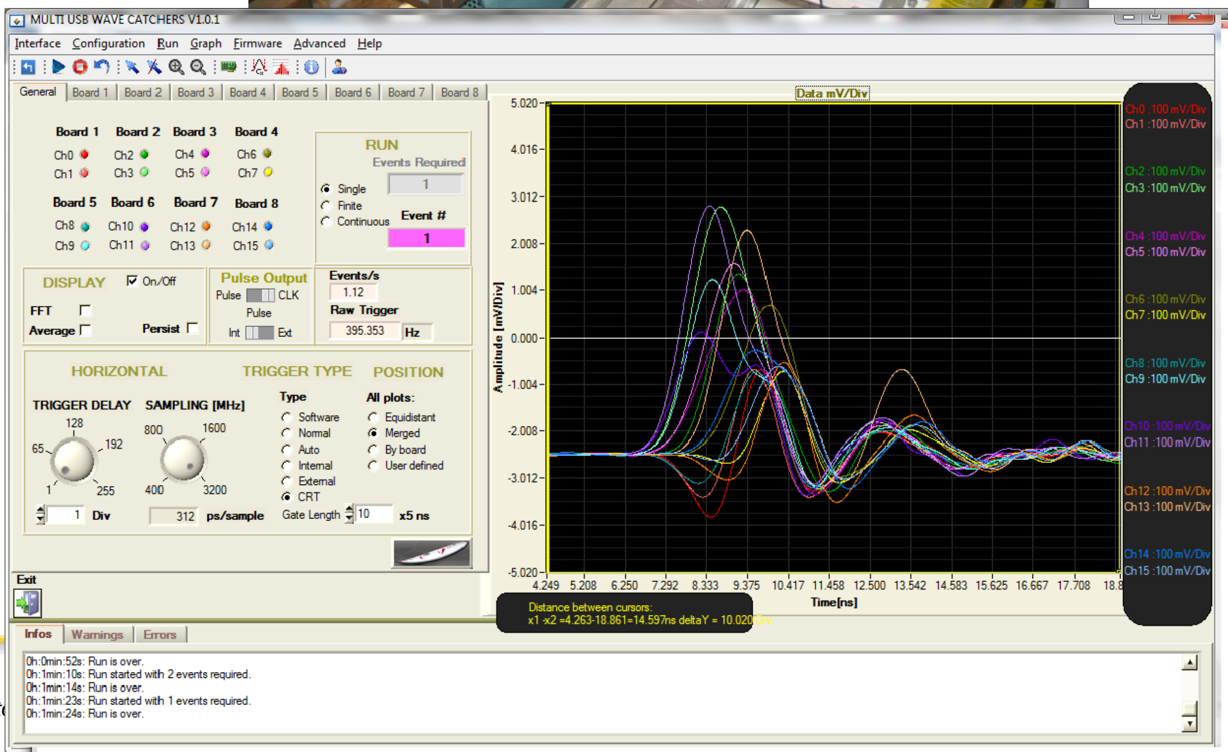
Mean differential jitter is of about 12ps rms which corresponds to **8.5 ps rms** of time precision per pulse

TOF at the SLAC cosmic ray telescope

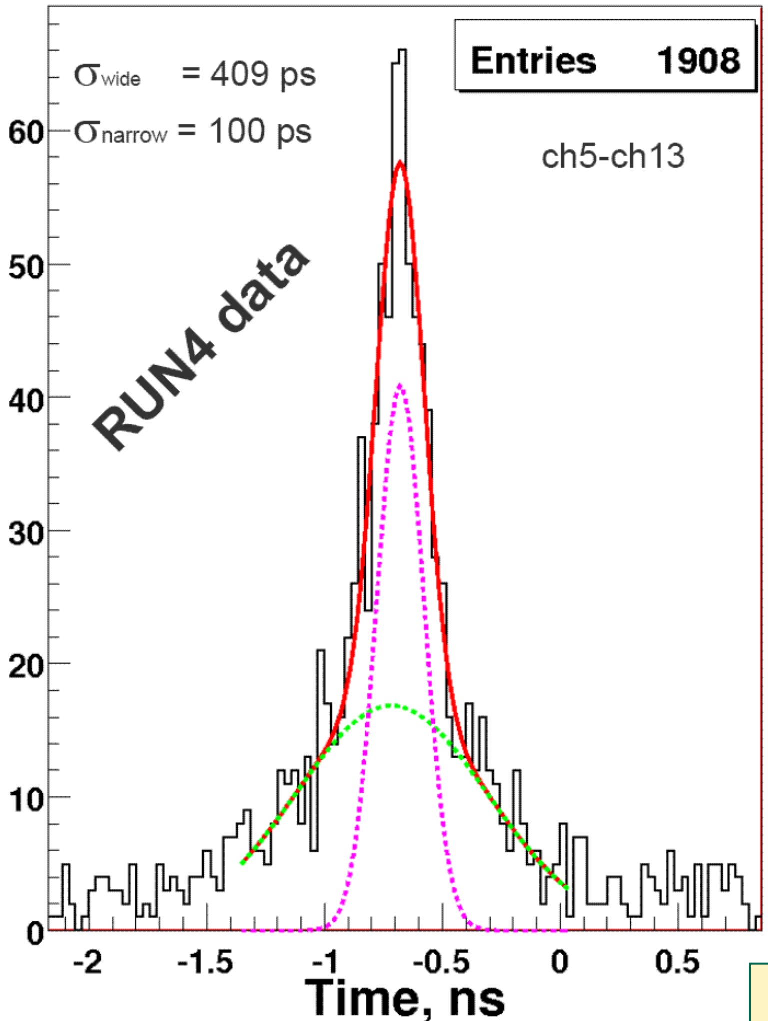
- TOF experimental setup on the CRT
- This innovative experiment will be described by Leonid Burmistrov in his talk this afternoon

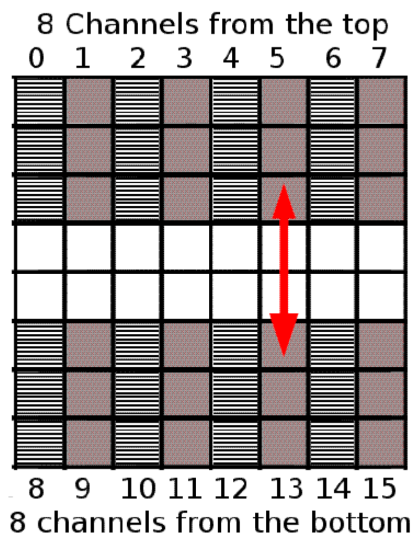






Single photoelectron time resolution between bars





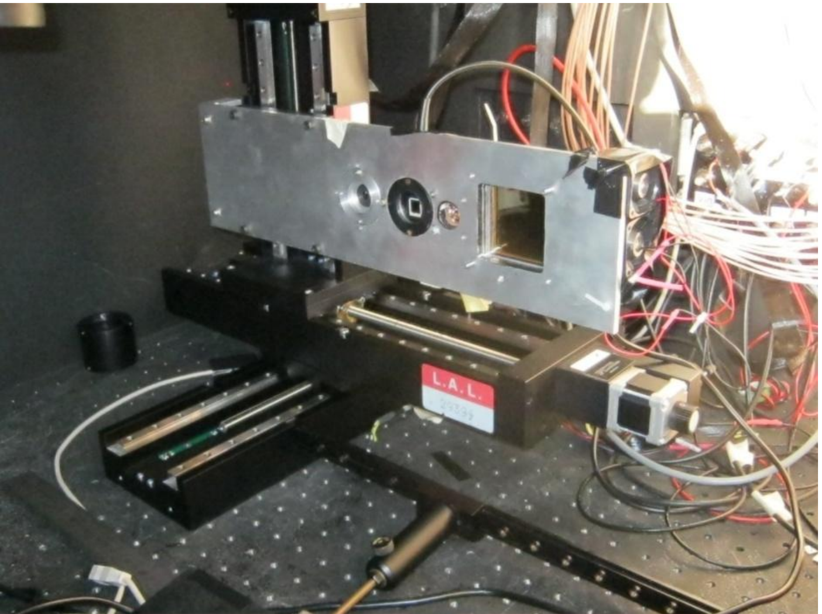
One example of time difference

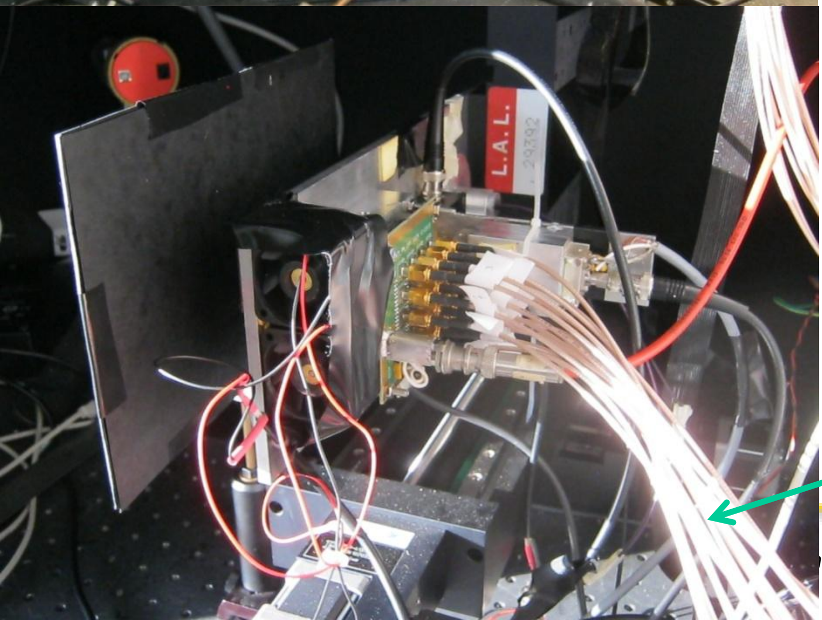
σ_{narrow}/sqrt(2) ~ 70 ps

More than adequate for final physics goal of 50 ps with 5 to 10 photoelectrons

MCPPMT test bench at LAL

- We performed a test scan of a Burle 85012 25-µm MCPPMT (16 groups of 4 ch)
  - Steps of 2 mm in X and Y => 900 steps
  - 20 s per step to get ~500 events
  - Example of an extracted 2-D efficiency plot for channel 6
  - Charge sharing at the limit between pixels can be studied



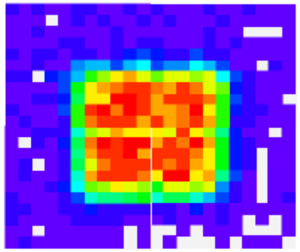


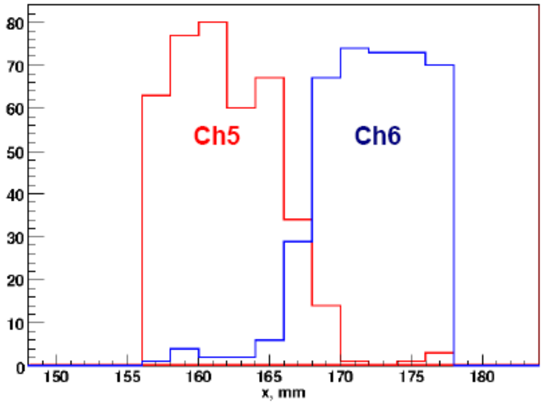
The MCPPMT on its scanning setup

Towards the 16 electronics channels

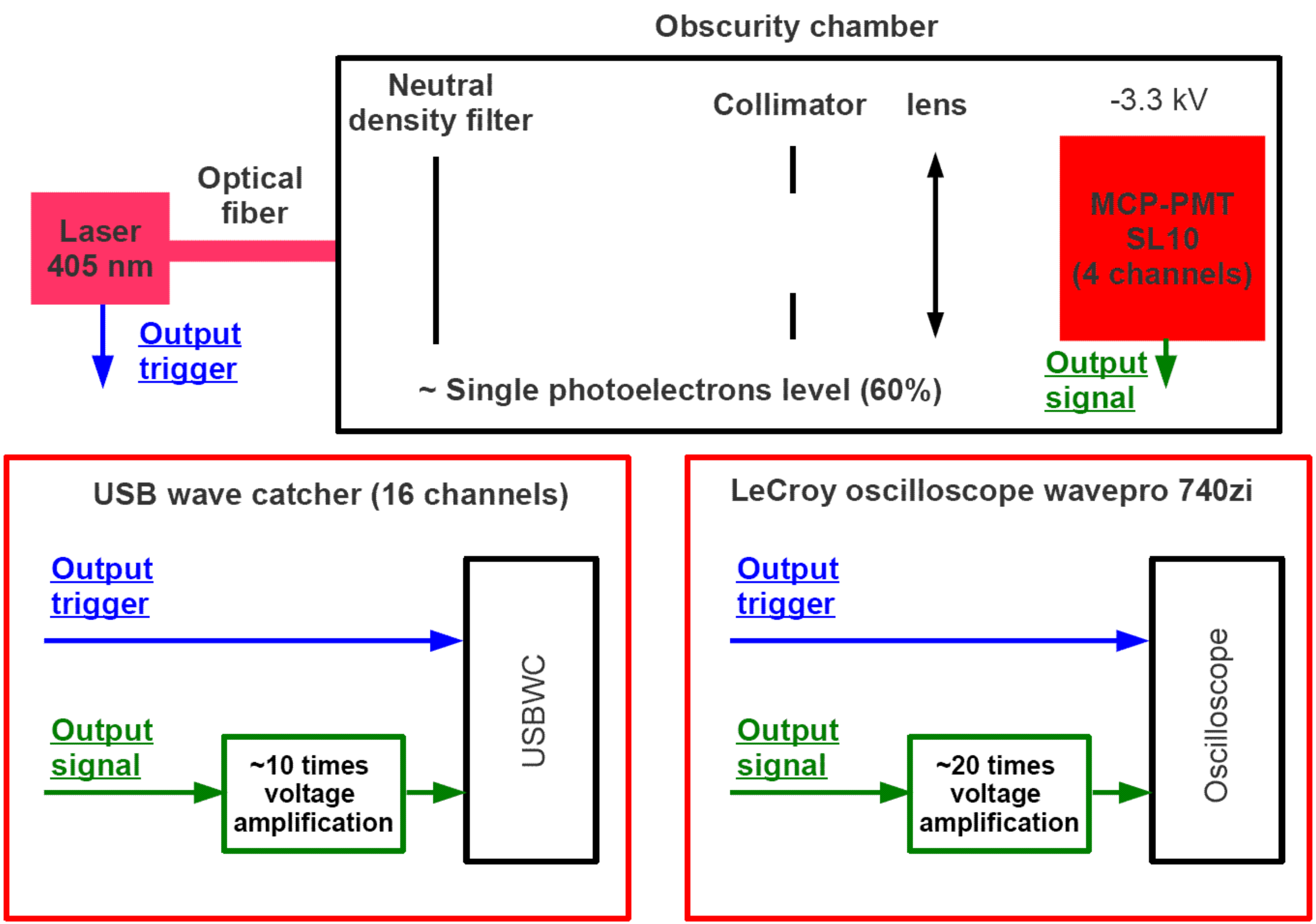
Mapping

X vs Y ch 6



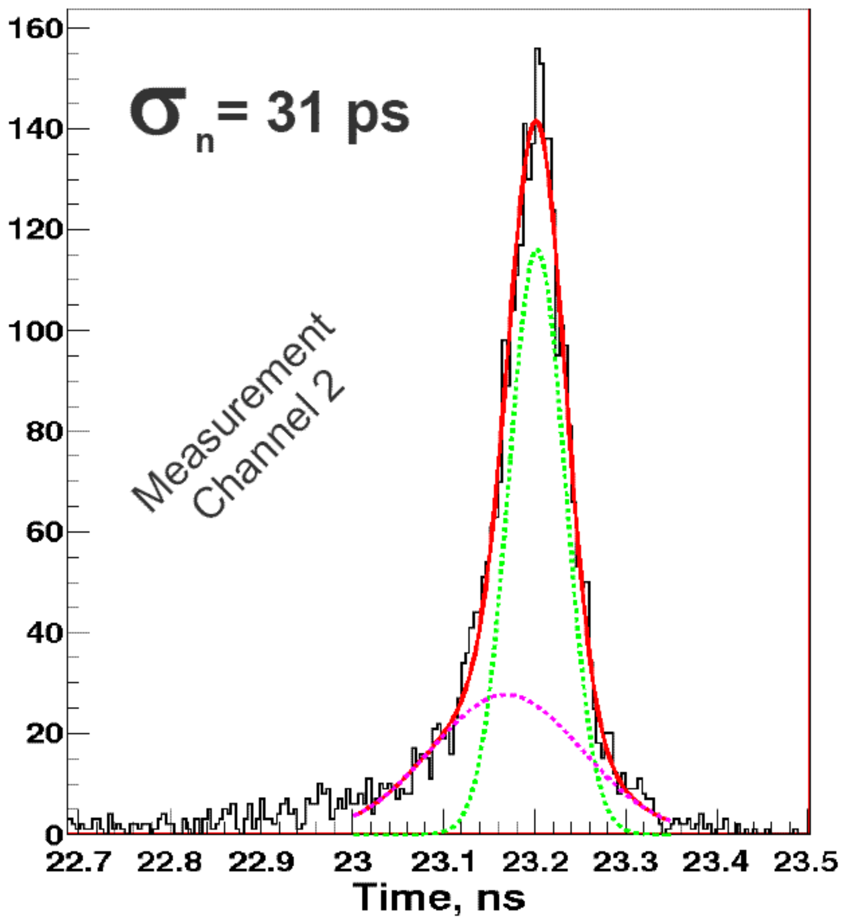


Time resolution of SL10 MCP-PMT (Experimental setup)

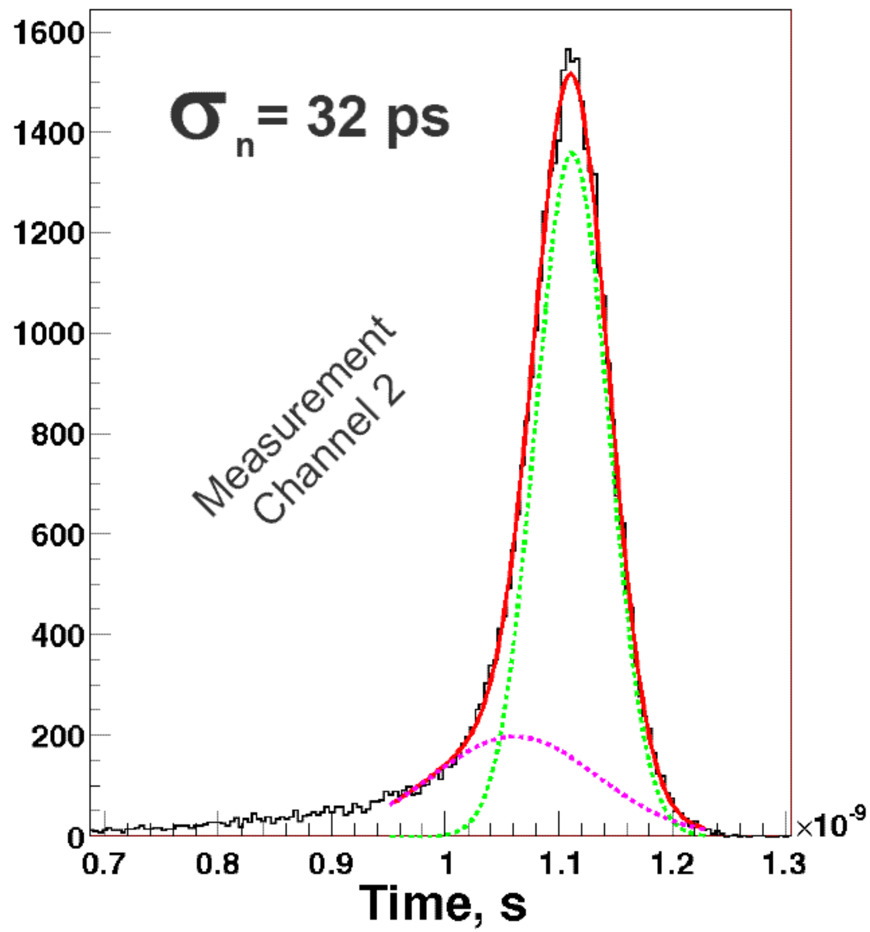


Time resolution of SL10 MCP-PMT (Measurements)

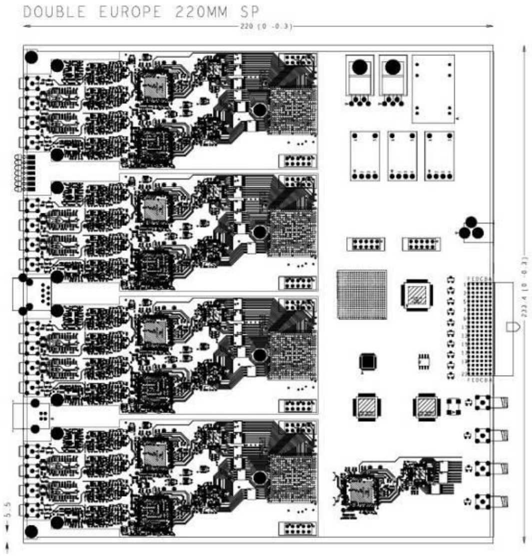
USB wave catcher (16 channels)



LeCroy oscilloscope wavepro 740zi

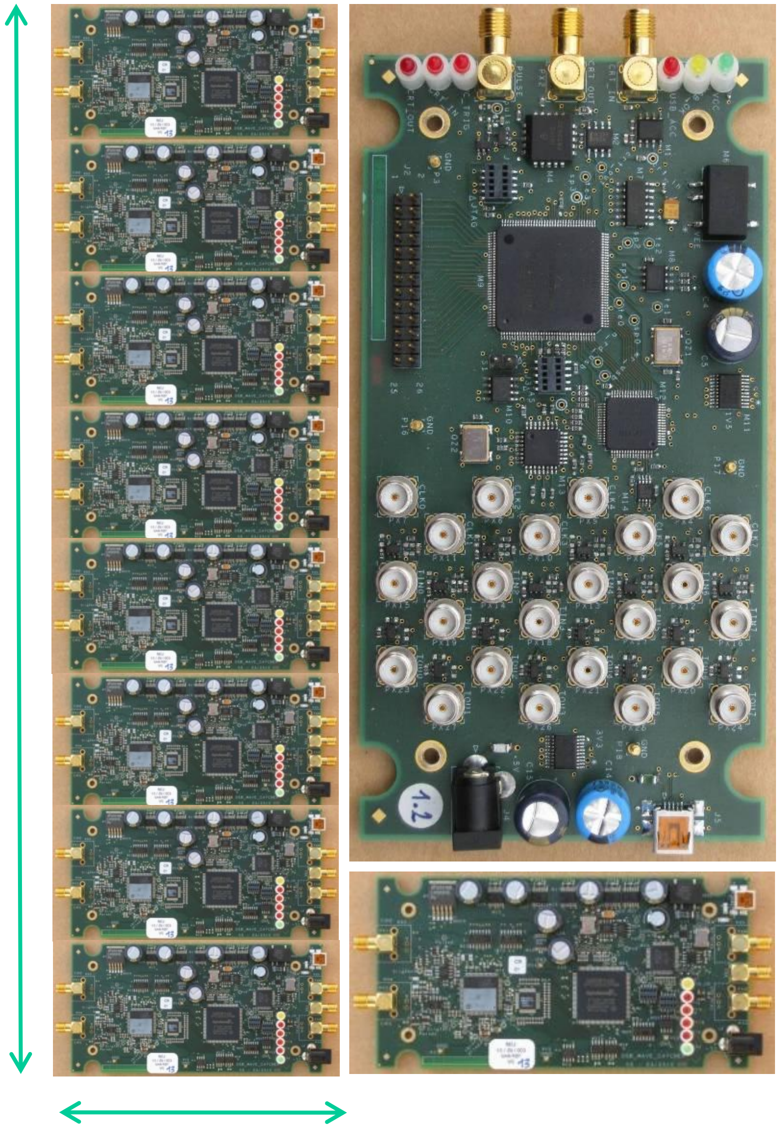


Newest developments



From a crate to a 16-channel board

8 x 75 = 600 mm !



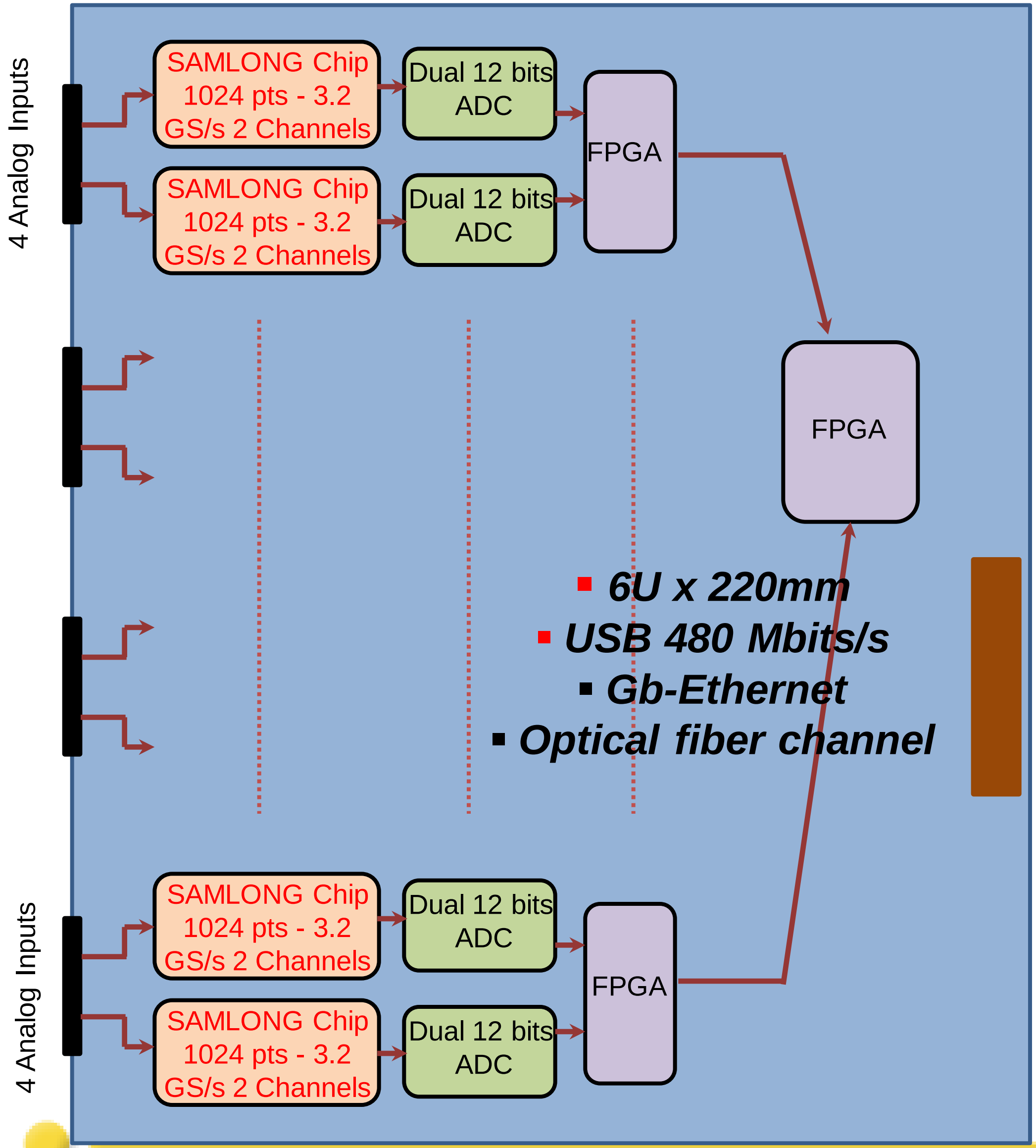
145 mm

- There is an increasing demand in **high-scale**/ very **high speed/high precision** boards.
- This kind of boards could also be used as **high precision TDC**
- **Power** and **cost** have to remain reasonable

  => < 20W

  => a few k€

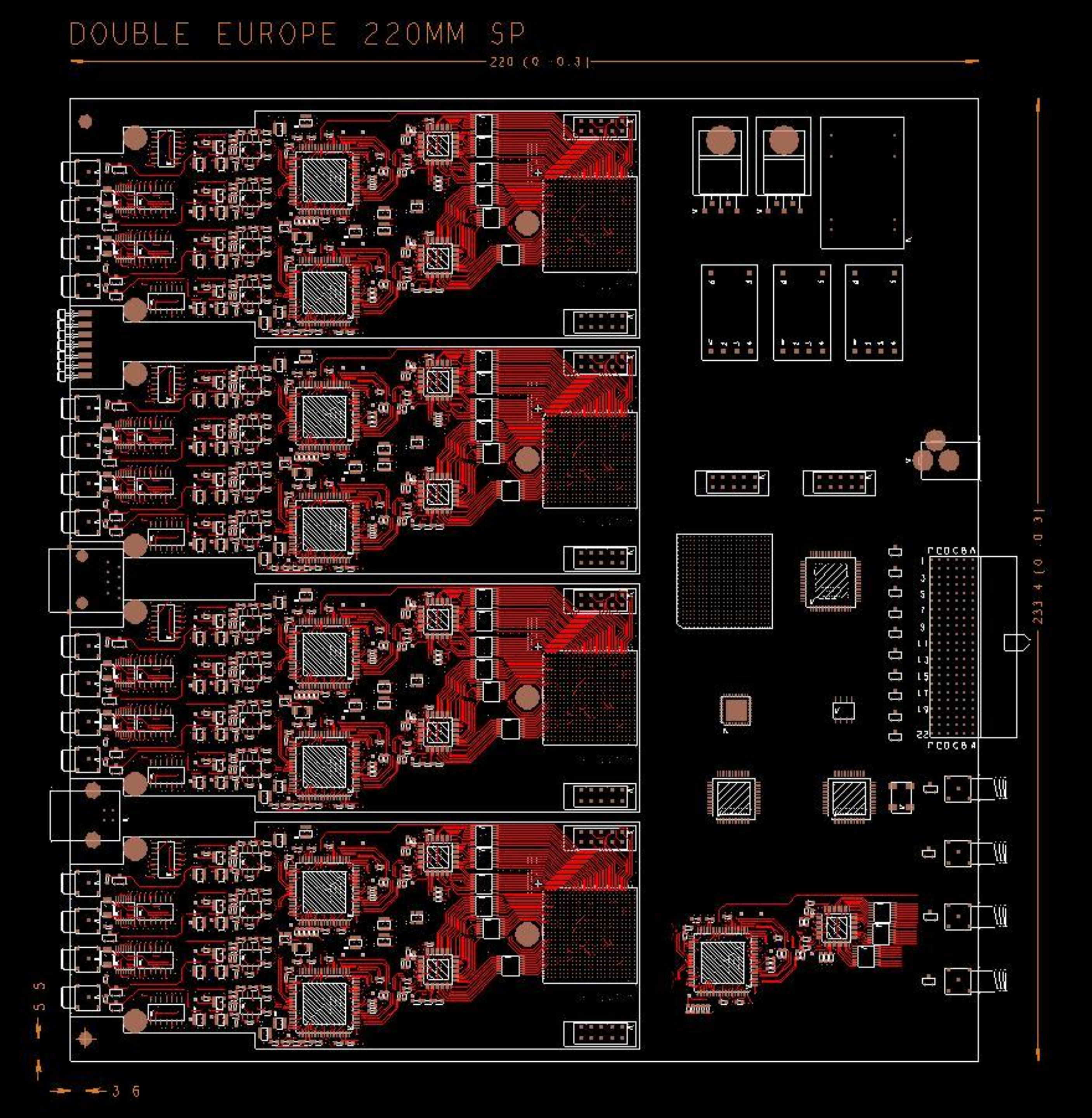
Under design: a 16-channel WaveCatcher



- Based on the very encouraging results of the 16-channel crate, we started the design of a **16-channel WaveCatcher board**
- This board will be compatible with both SAM (256 cells/ch) and SAMLONG (**1024 cells/ch**)
  - The board can be synchronized externally => possibility to scale the system up to **320 channels in a crate**
- The first prototype will be available in September 2011

Board features (not exhaustive)

- Possibility to add an **individual DC offset** on each signal
- Possibility to **chain** channels by groups of 2
- **2 individual trigger discriminators** on each channel
- External and internal trigger + numerous modes of **triggering on coïncidence** (11 possibilities including two pulses on the same channel) => useful for afterpulse studies
- **Embedded digital CFD** for time measurement
- **Embedded signal amplitude** extraction
- **Embedded charge mode** (integration starts on threshold or at a fixed location) => high rates (~ 3.5 kEvents/s)
- **2 extra memory channels** for digital signals
- One **pulse generator** on each input
- **External clock** input for multi-board applications
- Embedded **USB, Fibre Channel** and **Ethernet** interfaces



Status of PCB design

- As of last week
- 4-channel blocks can be used as mezzanine on other boards (CAEN fast waveform digitizers)

Future developments

- We have now in hand all the information we need to design **new analog memory ASICs, boards and systems** targeting one or more of:
  - A **lower power** consumption: < 100 mW/ch
  - A **higher sampling frequency**: ≥ 5 GS/s
  - A **higher signal bandwidth**: > 500 MHz
  - A **greater sampling depth**: > 1024 cells/ch
  - A **higher density**: more channels per chip
  - A **higher time precision**: ≤ 5 ps rms
  - A higher modularity between the **number of channels** and their **length**

- These circuits which should be submitted in 2011 and later will be increasingly used in many fields of **high energy physics**, astrophysics, and in **the characterization of very fast captors** (like ultra-fast PMTs, SiPMs, silicon detectors, …).

- A **PHD student** will participate in these designs from Sept 2011 on.
  - **AMS 0.18µm** technology should be used

  => good compromise for mixed signal designs

Conclusion

- **Photo-detectors** are implied in all kinds of applications. Associated electronics can be used either for their **characterization** (test benches) or for their **readout** (experiments).

- For **test benches**:
  - if the number of channels is small (≤4), then high-end oscilloscopes are commonly used. For small budgets, analog memory-based acquisition boards can do the job for cheap.
  - If the **number of channels increases**, and if one wants to study all of them in parallel, analog memories are good candidates for a reasonable price

- For **physics experiments**:
  - Dedicated A/Q/T ASICs are the natural option
  - But if one wants to see the **waveforms**, or if **time measurement** precision has to **better than 30ps rms**, analog memories seem to be the right answer