

Electronics for Photodetectors

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LPNHE Paris

New Developments In Photodetection

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331 44 27 22 37

Thanks to

Christophe de la Taille

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Dominique Breton

Thanh Hung Pham

Hervé Lebbolo

Kholdoun Torki

and many others...

- **Introduction**
- **Contexts**
 - **High Energy Physics**
 - **Space, Medical**
- **Photodetectors**
 - **Vacuum**
 - **Solid state**
- **Photodetectors Electronics**
 - **Technologies,**
 - **Photon counting**
 - **Amplitude, charge**
 - **Imaging**
 - **Timing**
 - **3D integration**
- **Conclusion**

Introduction

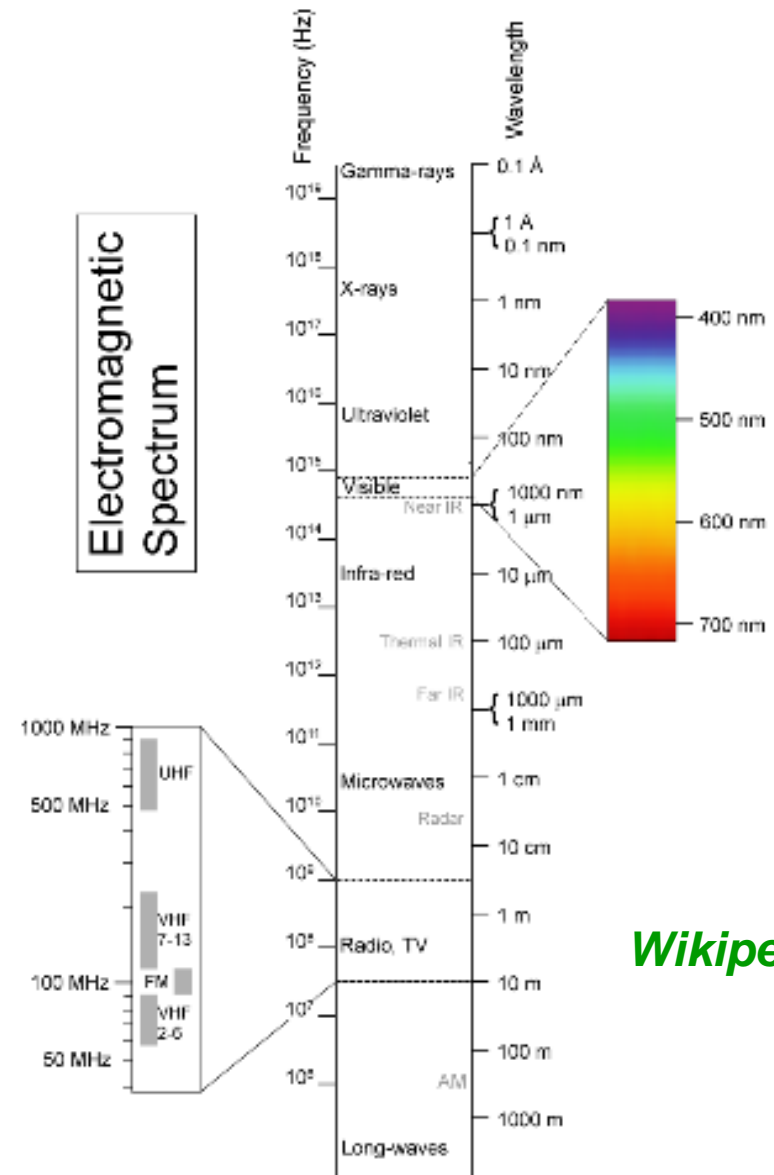
Electromagnetic wave = photon

- **Electromagnetic wave:**
Wavelength λ , Maxwell's equations

- **Photon:**
Photon wavelength hc/λ
Schrodinger's equation

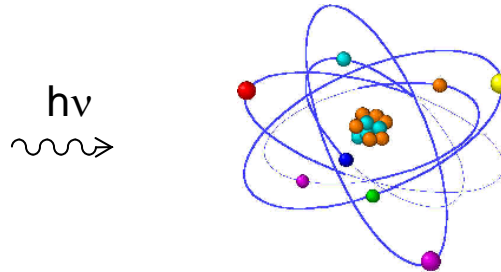
(Electromagnetic field)² :
photon's probability of presence

1eV 1.2 μ m 2.4¹⁴ Hz
Near Infra-red photon



Wikipedia

Photon Electron interaction



Photon-atom interaction:

- No absorption : Rayleigh elastic scattering no electron ejected
 - Energy change, absorption:
 - **Compton effect:** photon scattered with wavelength change
electron ejected
 - **$e^+ e^-$ pairs generation** (γ rays): 2 x 511 keV minimum energy
- « Shower » in a « radiator » measured in a (photo)-detector

Photo-detectors

Vacuum devices

- *Photo-Multipliers Tubes (PMTs)*
- *Hybrid Photo-diodes (HPDs)*
- *Micro-Channel Plates (MCPs)*

Solid state devices

- *Charge Coupled Devices (CCDs)*
- *Avalanche Photo-diodes (APDs)*
- *Silicon Photo-multipliers, (SiPMs, Geiger mode APDs)*
- *Monolithic Active Pixel Sensors (MAPS, CMOS Silicon)*

Hybrids

- *Hybrid APDs (HPD/APD)*
- *Electron Bombarded CMOS (HPD/MAPS)*

Vacuum and Solid-state

Vacuum devices

Current signal from electrons in vacuum

- *Large area, large fill factor, poor QE*
- *Full-custom Photo-cathode*
- *Electron multiplication, high gain, fast*
- *Low noise (photo-cathode noise)*
- *Some sensitivity to magnetic fields (depends on device)*
- *Readout with external ASICs*

Solid state semi-conductor devices

Current signal from e-/holes + avalanche in $\frac{1}{2}$ conductor

- *Size limited to a wafer, limited filling factor, high QE*
- *Spectral response of $\frac{1}{2}$ conductor (Si, GaAs, HgCdTe...)*
- *Multiplication in high electric fields (depleted PN junctions)*
- *Noisy due to reverse currents avalanches*
- *Noise very sensitive to irradiation*
- *No sensitivity to magnetic field*
- *Readout easy to integrate + 3D availability*

Devices

Vacuum devices

Photo-multipliers
Hybrid photo-diodes (HPDs)
Electron bombarded CMOS
Micro-Channel Plates

Solid state (semi-conductor) devices

Avalanche Photo-diodes
Silicon PMs

Hybrids

Electron bombarded Silicon

Vacuum devices

Single photo-electrons signals

Silicon Photo-Multipliers (SiPM), Micro-channel Plates (MCP)

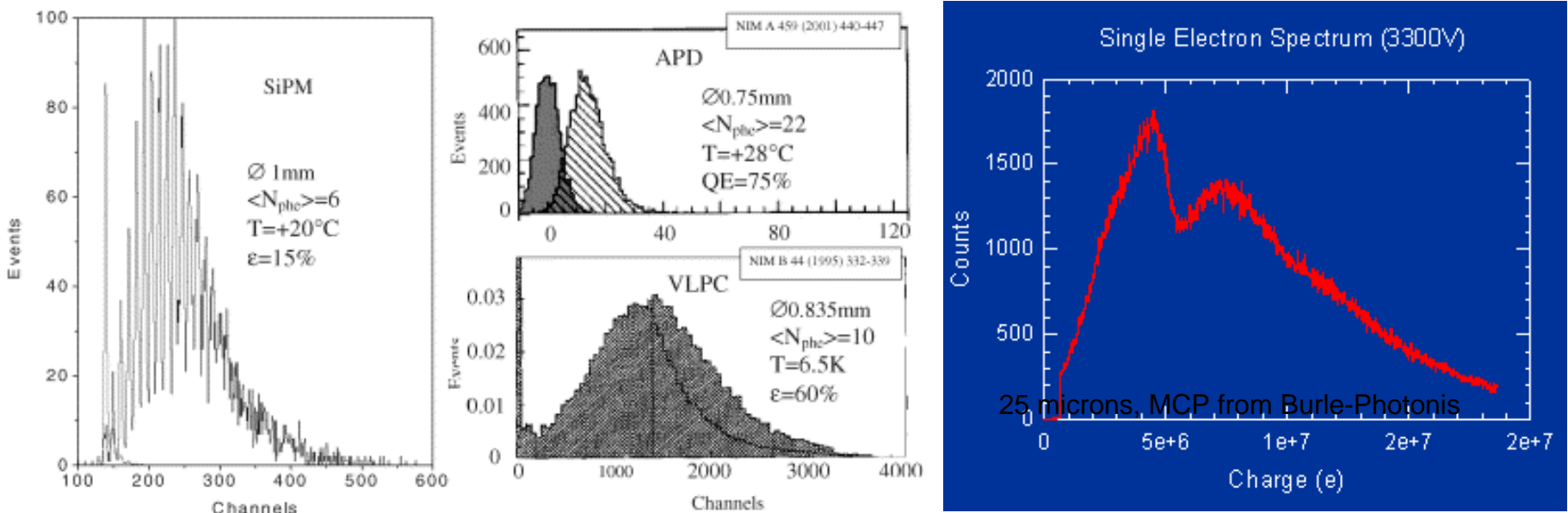


Fig. 3. SiPM application for sci fiber MIP detection (at room temperature): comparison with APD [6] (room temperature) and VLPC [7] (6.5°K).

Silicon PMs From B. Dolgoshein et al.

25 μm MCP from P. Hink (Burle-Photonis)

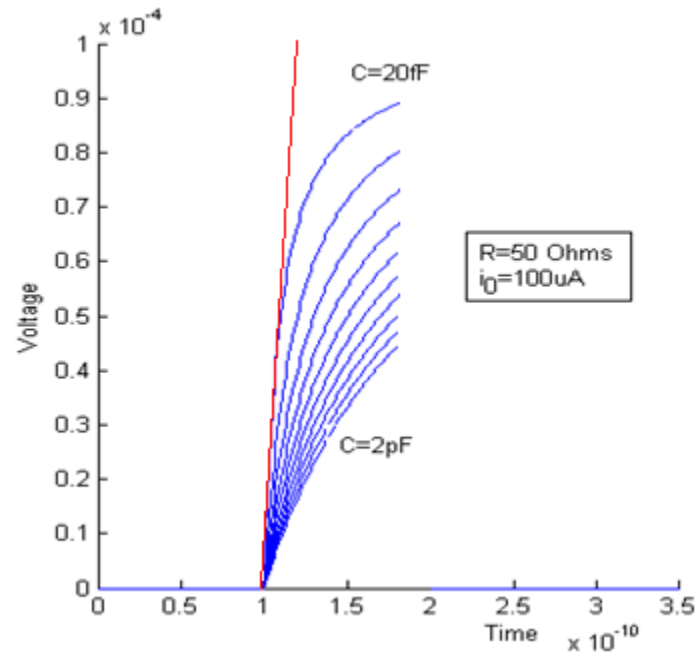
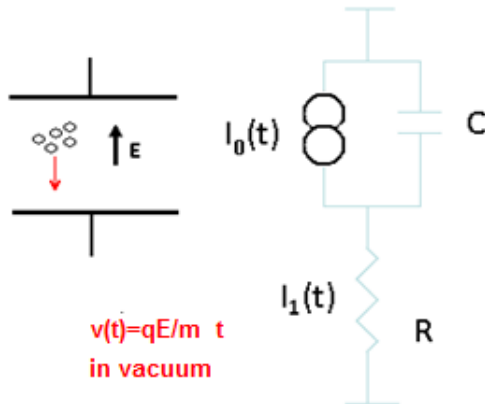
Signal development

Effect of first order passive:

$$i_0(t) = q n(t) v(t)$$

Step response:

$$i_1(t) = i_0[1 - \exp(-t / RC)]$$



- **Current signals occur as long as charges move in the detector gap**

Rise time is RC dependent at first order sets the electronics bandwidth for timing

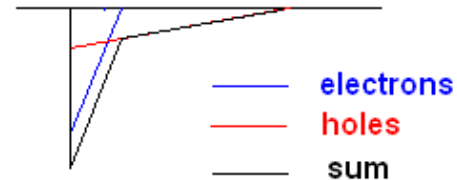
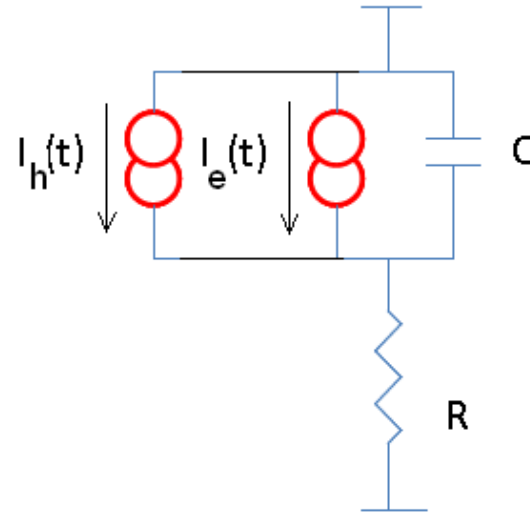
Serial noise proportional to C

R small, 50Ω or less if a common base preamp is used

Electronics should not increase C (cables, connectors...)

C is the capacitance seen during the rising edge (not a full coaxial cable length)

Signal development (1/2 conductor)



Two types of carriers:

- Electrons
- Holes, 3 times slower in silicon
- 75 electrons-holes in one micron

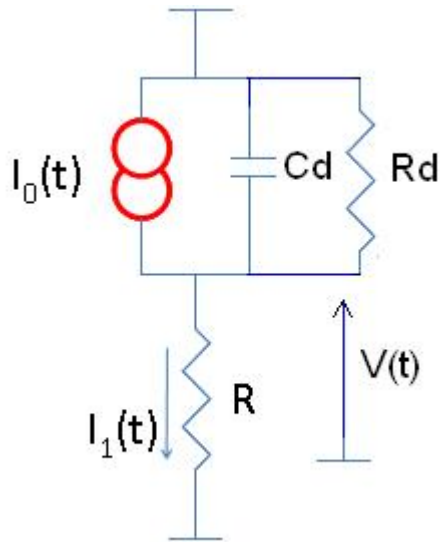
- APDs and SiPMs:

- Avalanche process is very fast, RC is observed in practice

Reduce R using a transimpedance or a current conveyor input stage

$$i_1(t) = [(i_e(t) + i_h(t))] [1 - \exp(-t / RC)]$$

Electronics and Signal Processing



Detector model

- Not much amplification needed with PMTs, MCPs, SiPMTs
1 electron is 5mV in 50Ω with a detector gain of 10^{6-7}
Or current conveying using common base input stage
- Amplification for 10^3 to 10^6 detector gains of (G)APDs, CCDs
- Filtering: “Pulse shaping” to remove amplifier noise out of the signal’s frequency content
- Digitization: Convert to a sequence of numbers using ADCs
- Feature extraction: get time, amplitude, charge...
Can digital filter as well, remove pedestals
- Send results to user: normalize, compress, error recover...

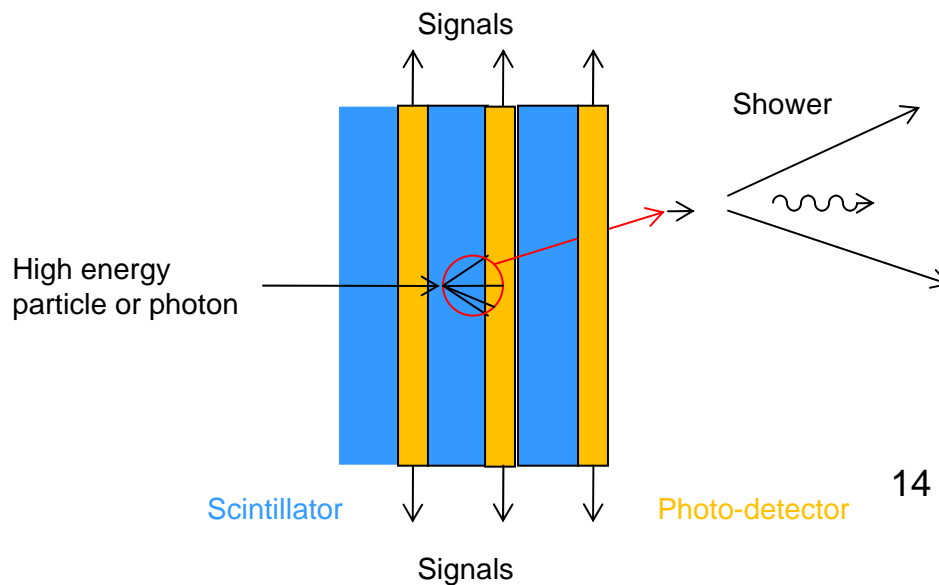
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High Energy Physics: Calorimetry

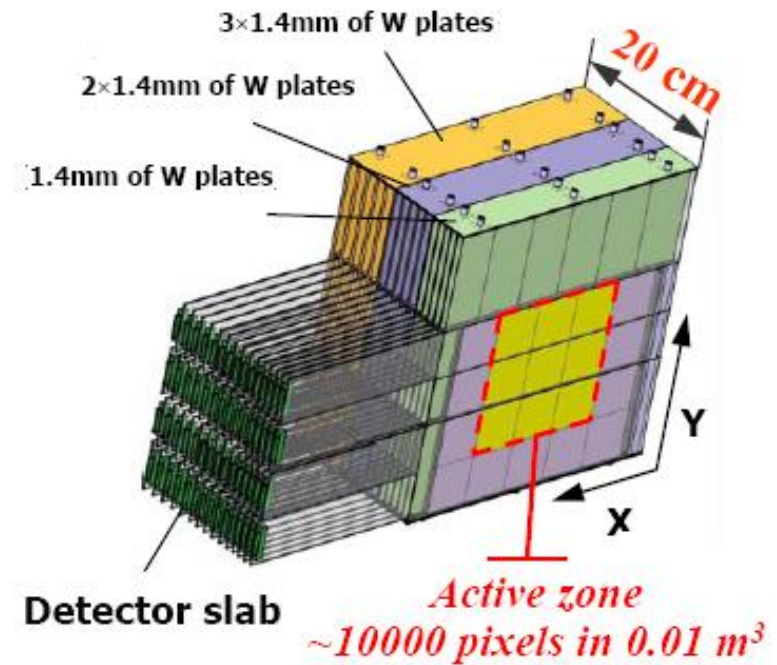
Calorimetry:

Showers develop in heavy materials Lead glass, Tungsten...

- High energy particles converted in scintillators into « showers »
 - Photo-detectors convert photons into electrical signals
 - Large dynamic range > 16-bit
- Showers are analysed and reconstructed



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Calice

ATLAS Hadron Calorimeter

ATLAS TileCal

Constraints for the front-end electronics

- Photo-multipliers rise time : 5 ns
- Least significant charge: 25 fC (20 MeV muon)
- Largest charge: 1.6 nC

- For noise and LSB of 12,5 fC
- The corresponding currents are:
 - 625 nA LSB
 - Max: 40mA

Large dynamic range, 16-bits

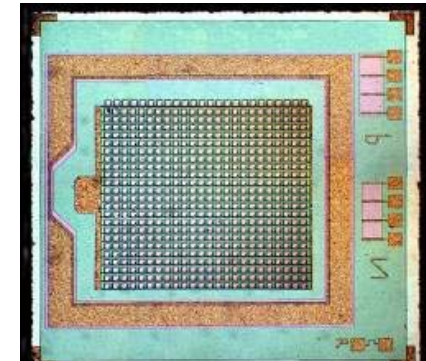
A multi-gain design is required

New photo-detectors for Calorimeters

Solid-state

▶ Array of avalanche photo diodes: “digital” photon detection

- ▶ Array can be 0.5x0.5 up to 5.0x5.0 mm²
- ▶ Pixel size can be 10 up to 100μm

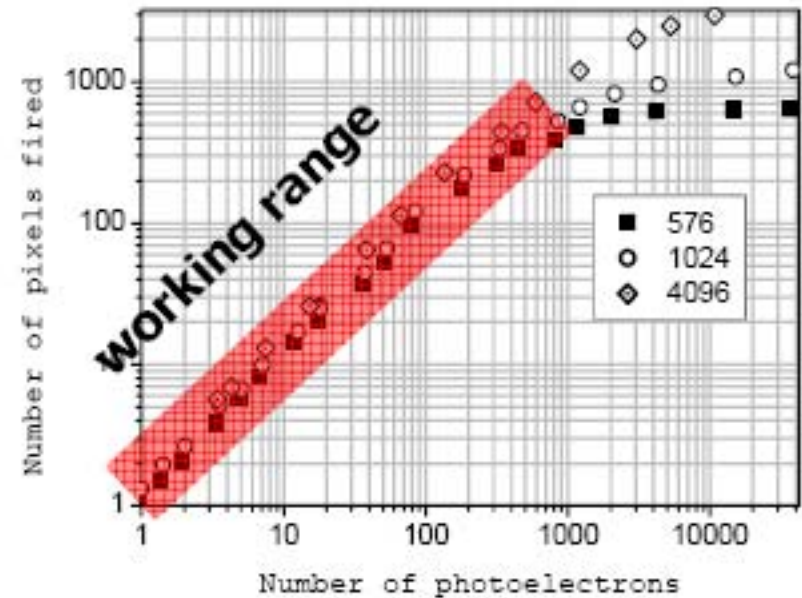


▶ All APDs connect to a single output

- ▶ Signal = sum of all cells

▶ Advantages over HPDs:

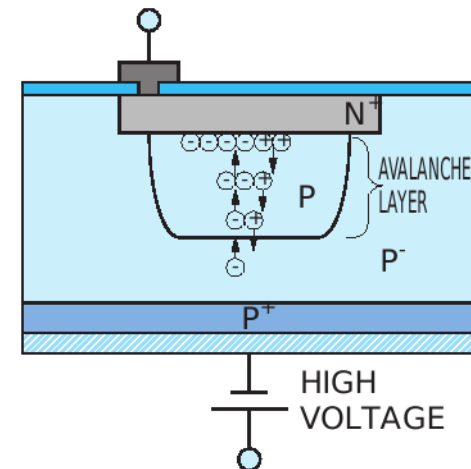
- ▶ 28% QE (x2 higher) and **10⁶ gain** (x500 higher)
- ▶ More light (40 pe/GeV),
less photo-statistics broadening
- ▶ Very high gain can be used to give timing
shaping/filtering



New photo-detectors for Calorimeters

Solid-state

- Reverse biased PN junction operated over breakdown voltage;
Geiger Avalanche triggered by the incoming photo-electron in the high electric field.
- Needs « quenching » to stop the current: biasing through a large resistor that drops the voltage (30-50V)
- A SiPM cell comprises several GAPDs having each a quench resistor, all GAPDs tied in parallel: analog sum
- Gain 10^5 - 10^7
- High Quantum efficiency (90%) but poor fill factor (quenching access electrodes)
- High dark counts, optical crosstalk, dead time,
- High Voltage process +CMOS readout (Philips patent)



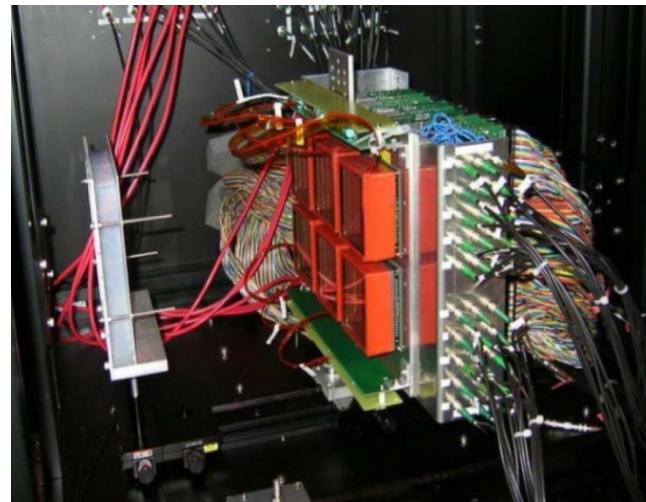
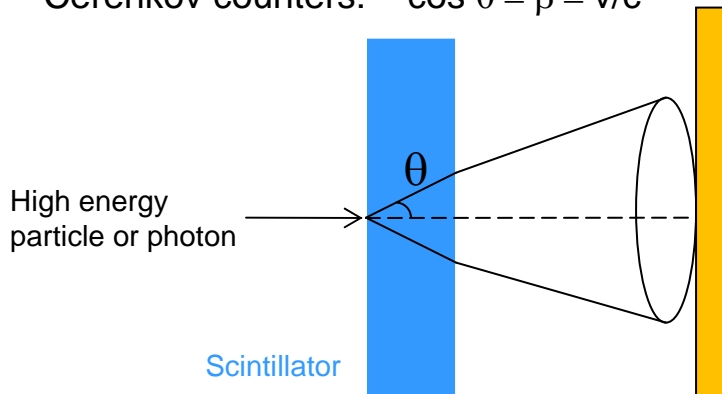
R. Mirzoyan (MePhy, MPI)

http://heapnet.mppmu.mpg.de/documents/oct_07/03_Photodac-07-Mirzoyan.pdf

High Energy Physics: Particle ID

Particle Identification:

- Cerenkov counters: $\cos \theta = \beta = v/c$



	SPECIFICATION	ACTUAL
Sampling Rate	500 MS/s-17GS/s	2.5 GSa/s-17GS/s
# Channels	4	4
Sampling Depth	256 cells	256 Cells
Sampling Window	$256 * (\text{Sampling Rate})^{-1}$	$256 * (\text{Sampling Rate})^{-1}$
Input Noise	1 mV RMS	1-1.5 mV RMS
Analog Bandwidth	1.5 GHz	Average 600 MHz
ADC conversion	Up to 12 bit @ 2GHz	Up to ~10 bit @ 2GHz
Latency	2 μ s (min) – 16 μ s (max)	3 μ s (min) – 30 μ s (max)
Internal Trigger	yes	yes

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Improved with 100ps resolution Time of Flight

Example:

**Fast timing readout using 10 GS/s
Analog Memory ASIC (SCA):**



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Space applications

Imagers

Space boarded Telescopes

JWST

Need to observe single photons with fair position resolution in all spectral domains, in particular (near to far) infra-red

Pixellated devices such as Charge Coupled Devices, Photo-detectors can be:

- Silicon in the visible
- Compounds materials
 - CdTe for soft Xrays
 - CdZnTe for hard Xrays
 - InGaAs for near IR
 - HgCdTe for far IR

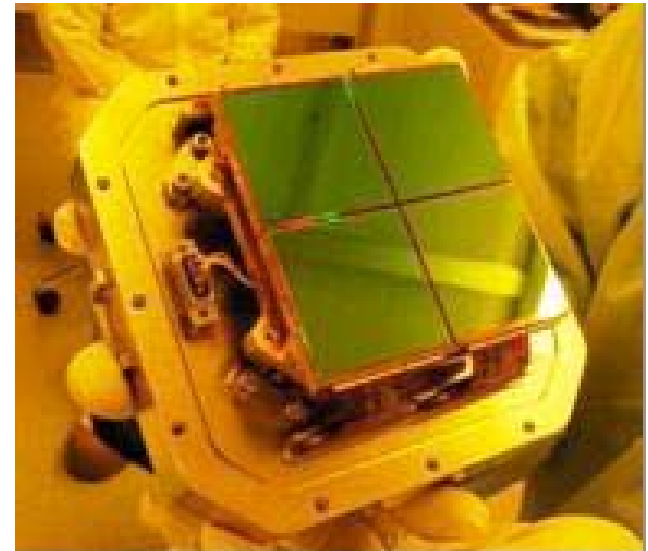
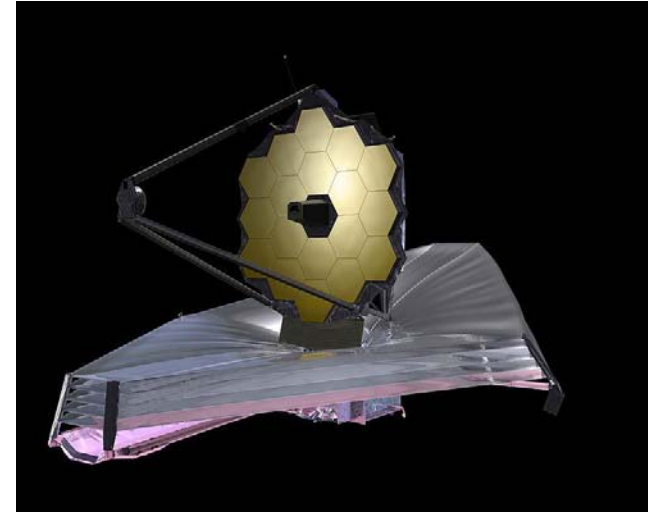
Pixels as small as $5 \times 5 \mu\text{m}$, can be instrumented.

Passive (CCDs) or active (Active Pixel Sensors)

Space boarded X ray detectors for imaging and spectrometry

<http://www.jwst.nasa.gov/>

« Asynchronous » events (no trigger)



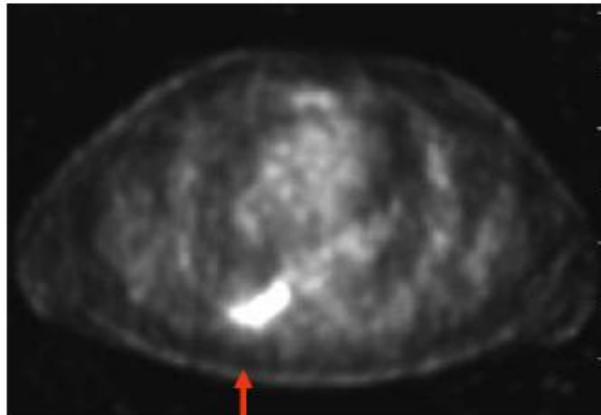
JWST Focal Plane Array

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3. Résultats

Comparaison d'images: basse dose/haute dose

Emission TEP



Scanner high dose

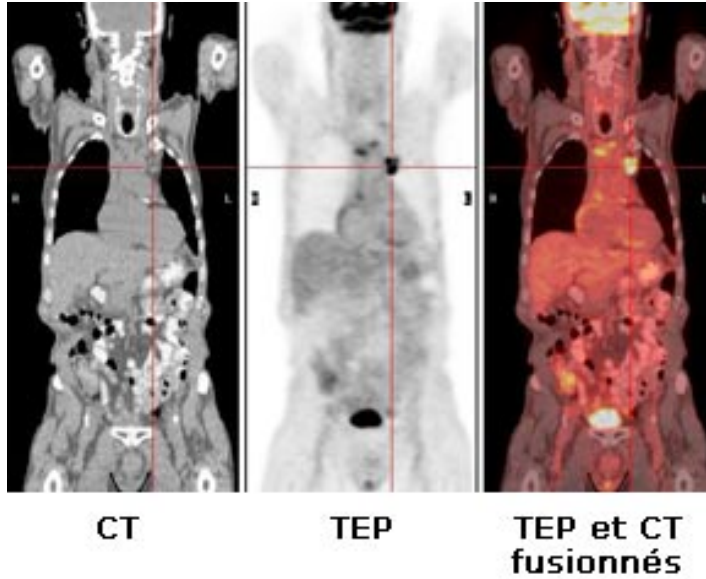


Scanner low dose

10 - Optimisation de la TEP-TDM dans le bilan d'un lymphome- Institut Curie- ROUSSEAU Aline -
13/04/2007

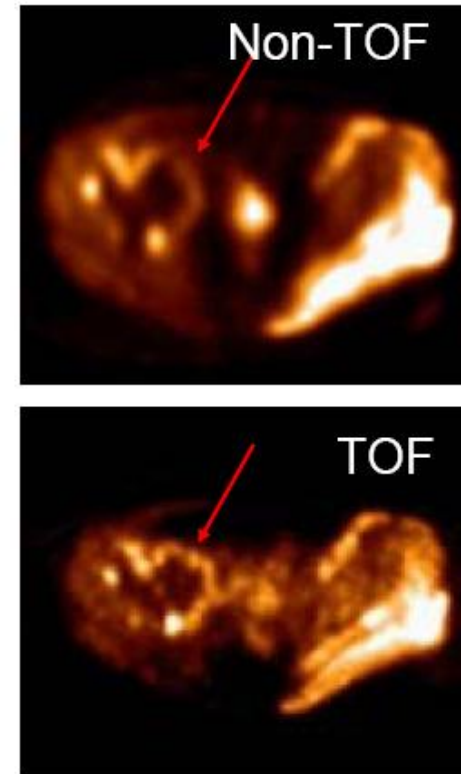
« Asynchronous » events (no trigger)

PET + CT TOF-PET



Combined PET-CT

AREVA



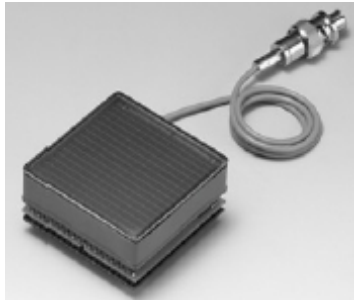
W.W. Moses

« Asynchronous » events (no trigger)

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Timing-Imaging Device (visible)

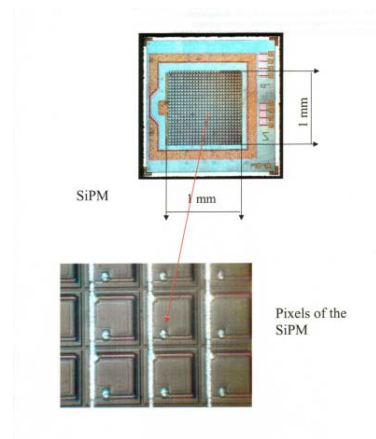
Multi-anodes PMTs Dynodes



Hybrid Photo-Diodes Electrons on Silicon EBCMOS



Silicon-PMTs Quenched Geiger



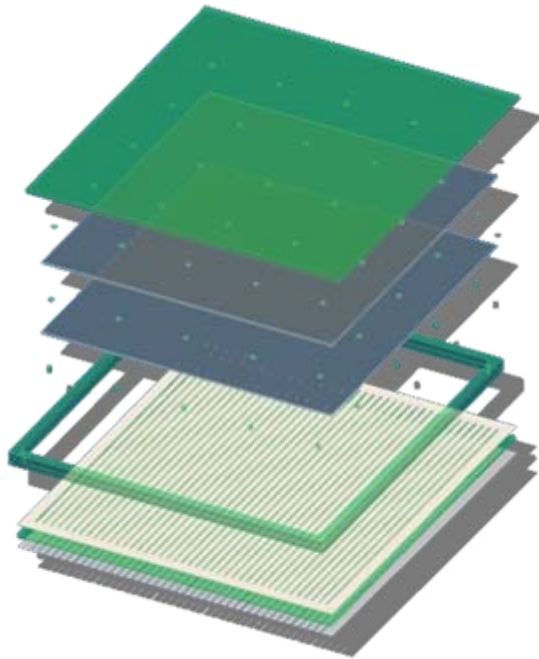
Micro-Channel Plates Micro-Pores



Quantum Eff.	25%	25%	90%	25%
Collection Eff.	90%	90%	70%	70%
Gain	10^6	10^{2-4}	10^6	10^6
Rise-time	1-5ns	1-5ns	250ps	50-500ps
Timing resolution (1PE)	150ps	100ps	100ps	20-30ps
Pixel size	$2 \times 2 \text{ mm}^2$	$10 \times 10 \mu\text{m}^2$	$50 \times 50 \mu\text{m}^2$	$1.5 \times 1.5 \text{ mm}^2$
Dark counts	$1-10 \text{ Hz/cm}^2$	$1 \text{ Hz}-40 \text{ kHz/cm}^2$	$1-10 \text{ MHz/pixel}$	$1 \text{ Hz}-1 \text{ kHz/cm}^2$
Dead time	5ns		100-500ns	1μs
Magnetic field	no	1.5T	yes	1.5T
Radiation hardness			1kRad=noisex10	good (glass, Al_2O_3)

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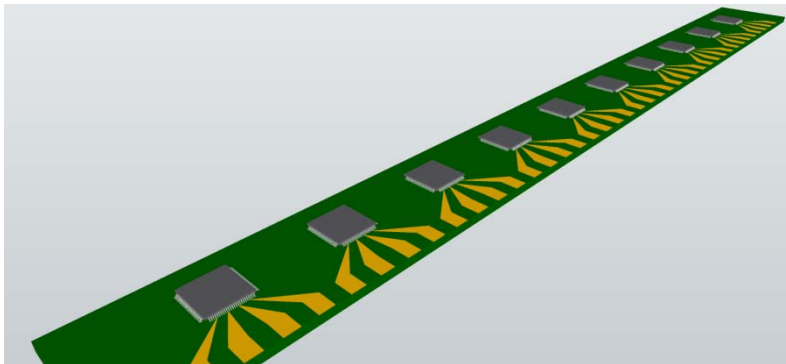
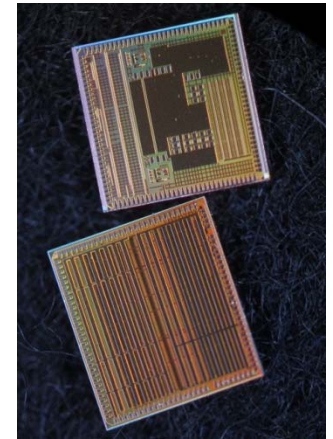
Large Area Micro-Channel Plates



20 x 20 cm² MCP structure:

- Custom photo-cathode
- 2-plate chevron (high gain)
- Transmission line 2D readout

limit the number of electronics channels

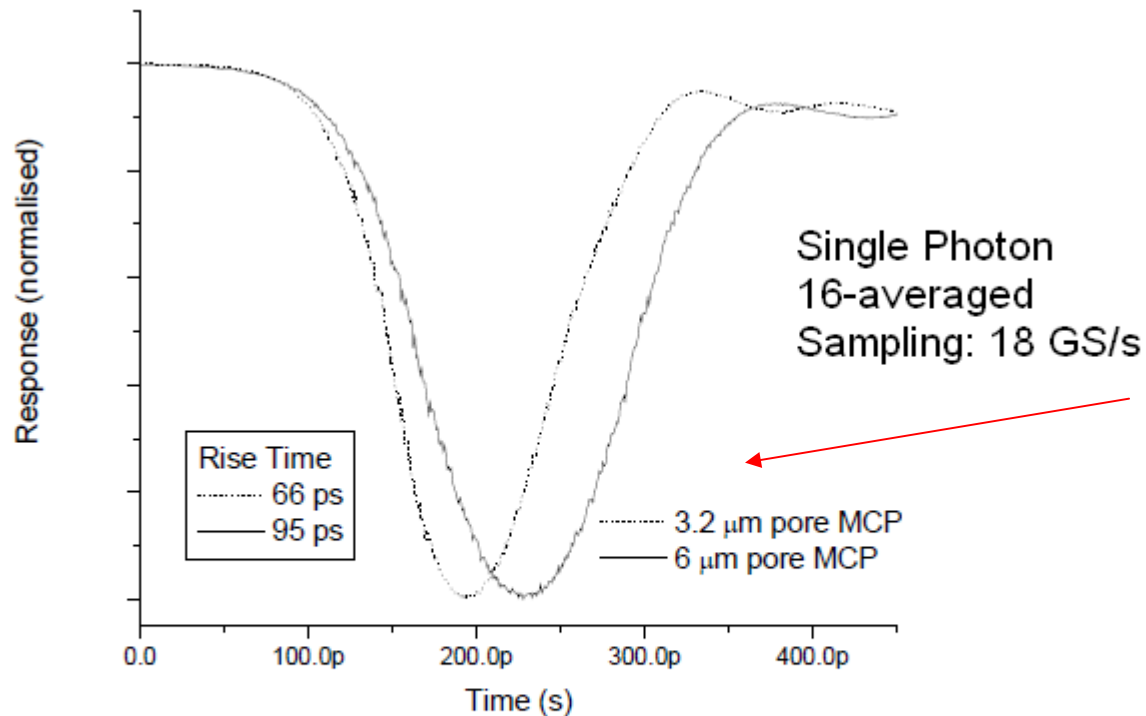


Electronics:

- **GS/s Flipped-Chip ASICs:**

Waveform Sampling + Digital Signal Processing

Micro-Channel Plate Signals



Time response curves for two models of PMT110 with different MCP pore diameters.

From Photek

The fastest photo-detector to date

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APDs

Multiplication initiated by electron-hole, thermally or induced within the APD and accelerated in the high electric field at the APD junction.

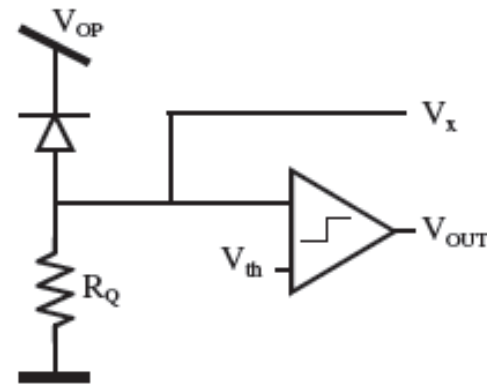
Proportional mode

- Bias: slightly *BELOW* breakdown
- Linear-mode: it's an *AMPLIFIER*
- Gain: limited < 1000

Geiger-mode

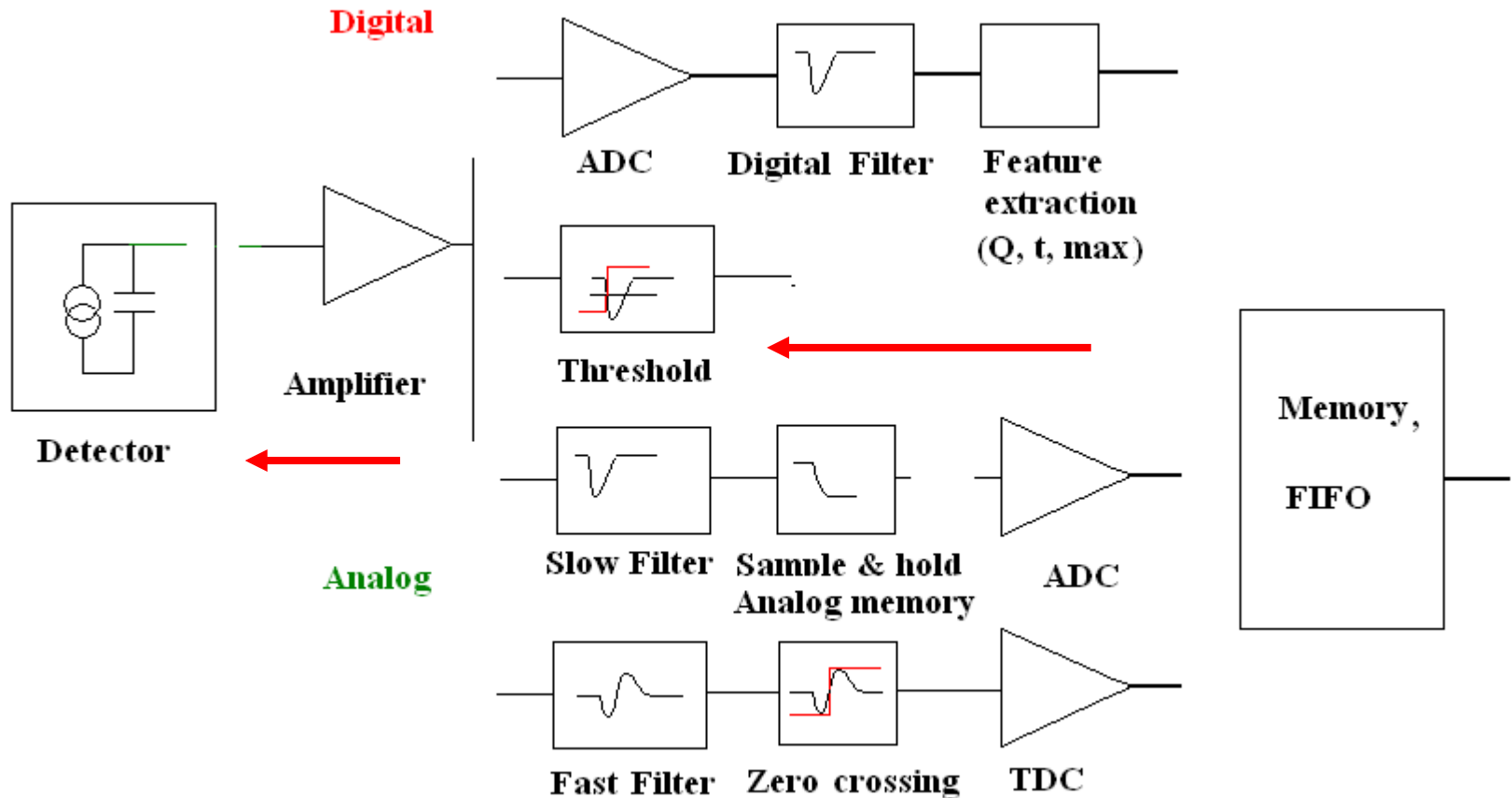
- Bias: *ABOVE* breakdown
- Geiger-mode: it's a *TRIGGER* device!!
- Gain: meaningless ... or “infinite” !!

A. Dieguez (U Barcelona)



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Typical Readout Components



Present trends: Move ADC to Front-end and Amplifier to Detector

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Technologies

Best results in analog design:

ASIC implementation at the transistor level

Position resolution requires smaller pixels

Increased on-pixel signal processing up to ADCs

Thinner feature size processes (65nm and less are coming...)

Available technologies:

- **Standard Deep Sub-Micron CMOS down to 65nm**
- **High voltage CMOS**
 - Large dynamic range readout (but multi-gain possible with std CMOS)
 - CCD clocks generation
- **Silicon Germanium (SiGe) for faster and low 1/f noise applications**
 - Higher mobility (GBW=300GHz)
 - Larger current gain (beta)
 - CMOS compatible (0.25 or 0.35 μ m) for mixed-signal design

ASICs feature size

The smaller the components, the faster, the less power, the greater density

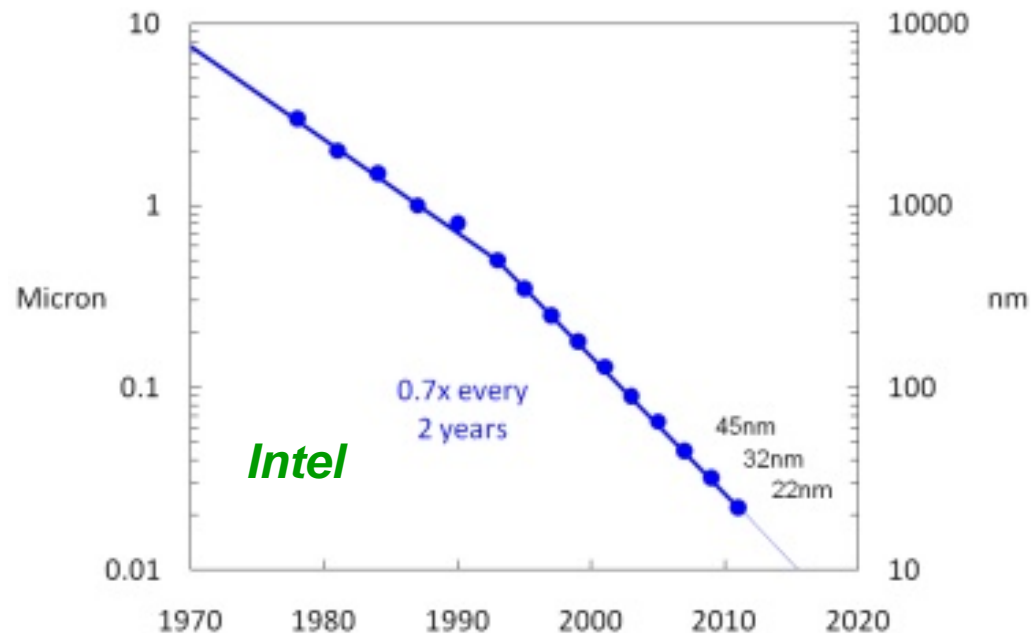
$$BW = 1/2\pi RC, \quad W_c = CV^2 \quad ENC \propto 1/C_{det}$$

Reduce capacitances wherever possible

But reduced dynamic range
since **voltage supply decreases**

$V_{dd} = 1.2-1.6V$ in 65nm
Multi V_{dd} – Multi V_t technologies

Multi-gain designs

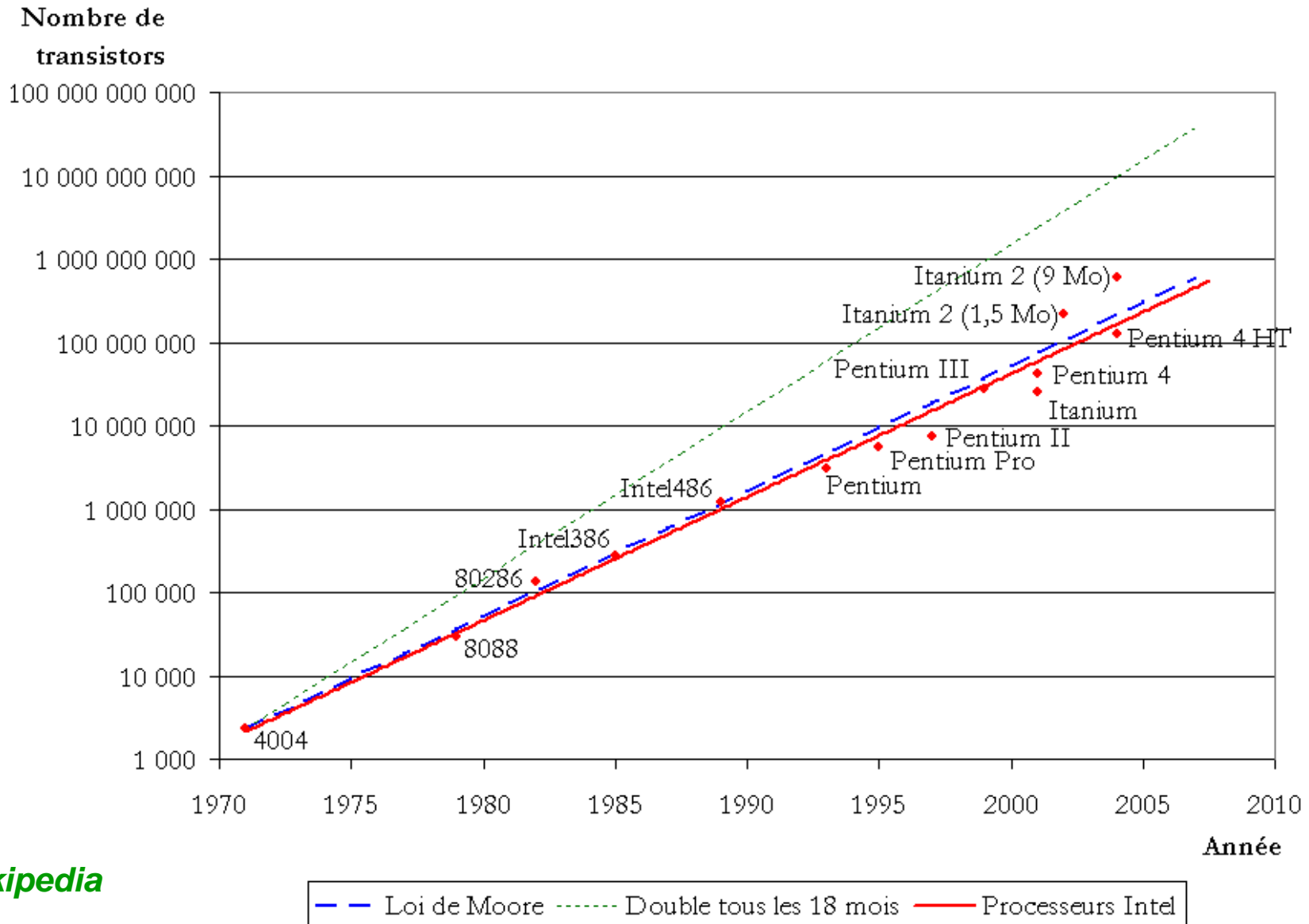


Moore's law: 1968

Computing power will double every two years, for approximately the same cost

35

ASICs integration level



isity:

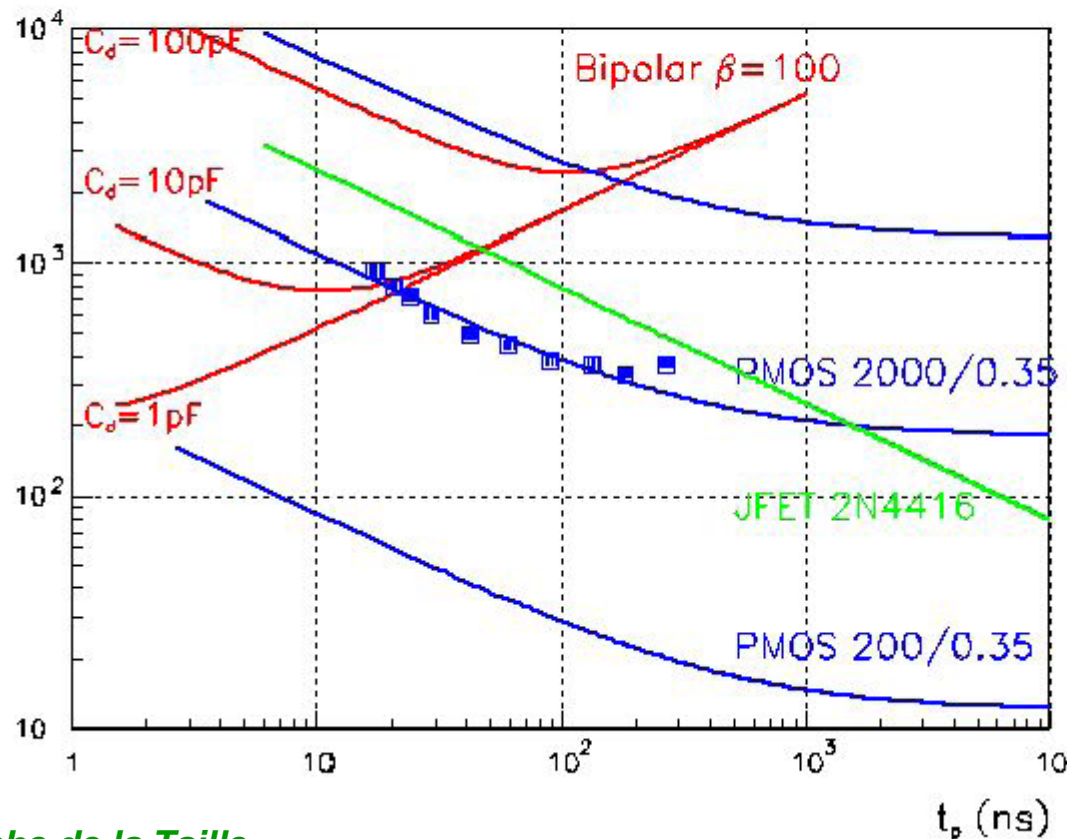
Wikipedia

Noise vs Technology

ENC for various technologies

ENC for $C_d=1, 10$ and 100 pF at $I_D = 500$ μ A

- MOS transistors best between 20 ns - 2 μ s



Parameters

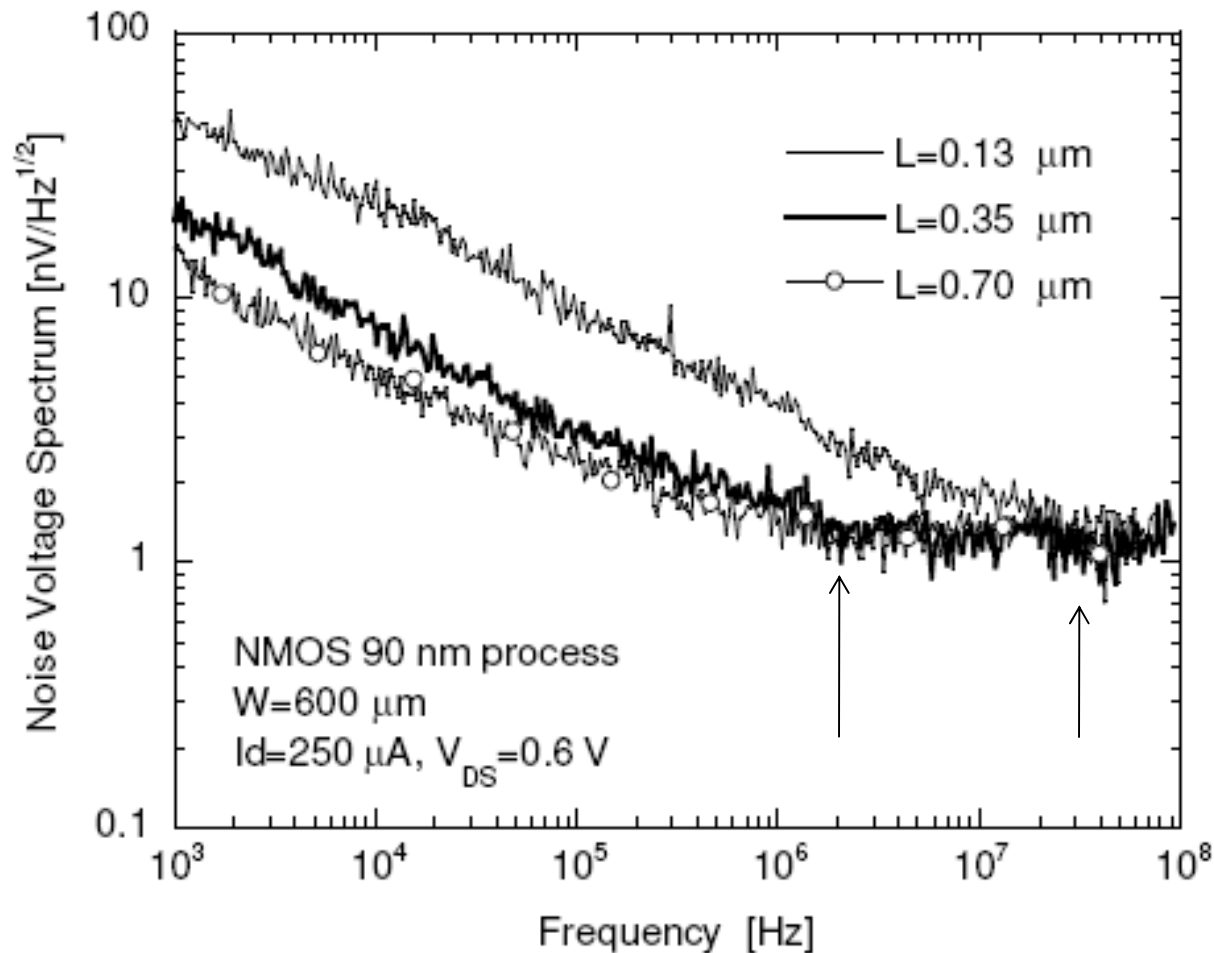
Bipolar :

- $g_m = 20$ mA/V
- $R_{BB} = 25$ Ω
- $e_n = 1$ nV/ $\sqrt{\text{Hz}}$
- $I_B = 5$ μ A
- $i_n = 1$ pA/ $\sqrt{\text{Hz}}$
- $C_{PA} = 100$ fF

PMOS 2000/0.35

- $g_m = 10$ mA/V
- $e_n = 1.4$ nV/ $\sqrt{\text{Hz}}$
- $C_{PA} = 5$ pF
- $1/f$:

Noise vs gate length



Noise spectral densities for 90nm at $L = 700, 350, 130\text{nm}$

M. Manghisoni

ASICs Costs

Costs of MPW (Source: Europractice) <http://www.europractice-ic.com>

Process	Feature	Cost Eur/mm ²	
CMOS 180nm		0.6k	UMC
180nm	HV 50V	1.2k	AMS
130nm		1.1k	UMC
90nm		2.8k	
CMOS 350nm	Opto	0.7k	AMS
SiGe 350nm		0.9k	AMS
250nm	30 GHz	1.9k	IHP
	180	4.4k	
130nm+ CMOS	300	5.4k	IHP
	400	6.0k	

50-100 parts / MPW run

Some minimum area (25, 16, 12 mm required)

Masks (production): 100-200k

Packaging

Ceramic: 20-30€/chip

Plastic : 2k€ + 1-2 €/chip

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Photon Counting

Space and Medical application: no trigger, asynchronous recording

High Energy Physics: a beam synchronous signal is usually available

Visible photons have 1 – 3 eV energy

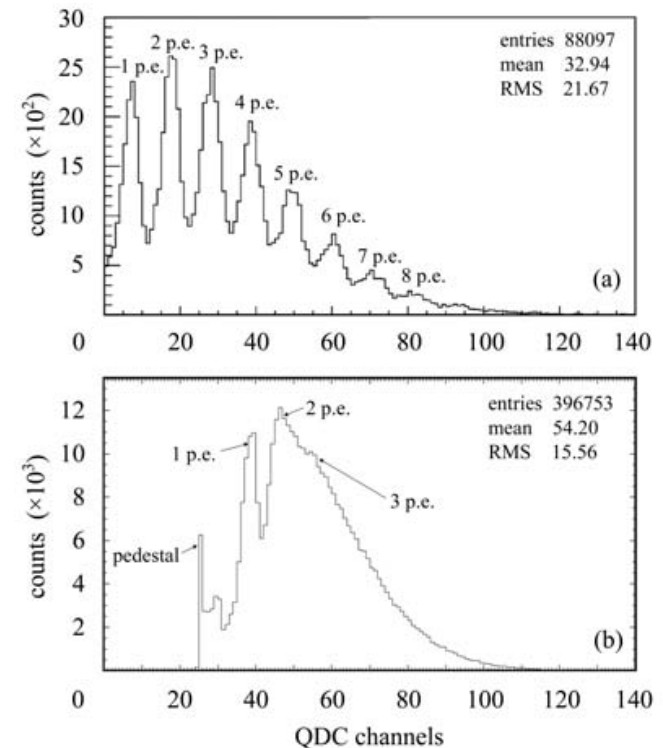
- Photo-cathodes have QEs of 30% at best
- In semi-conductors, gap is 1.12 eV for Silicon, 1.4 eV for GaAs

Only 1 electron-hole pair per photon

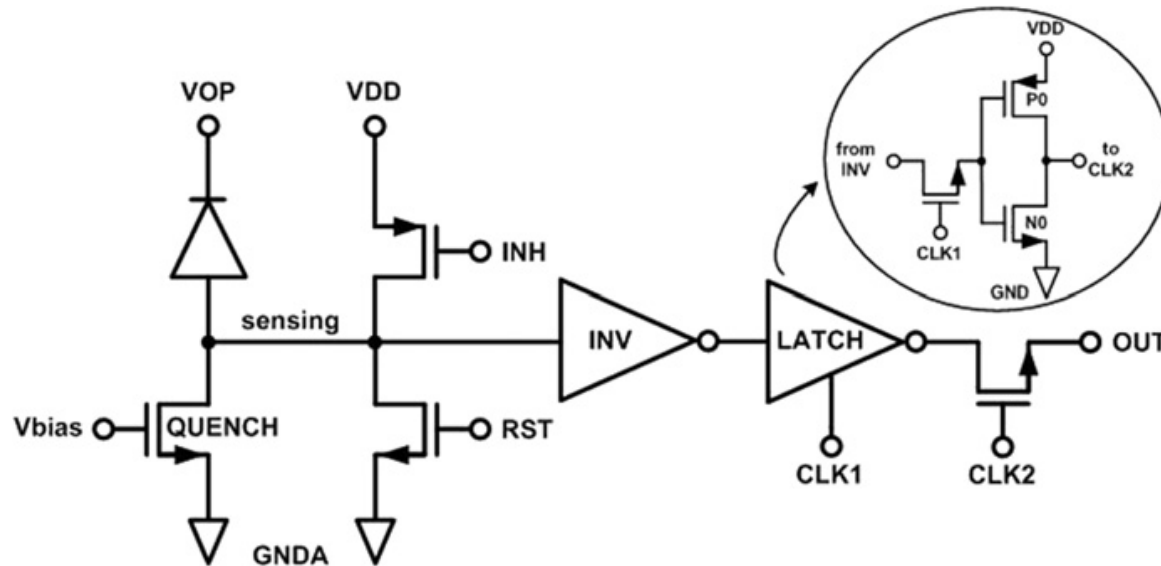
**Single photon counting,
noise below 1 electron**

**Silicon PM and Vacuum PMT
responses compared**

<http://hepnp.ihep.ac.cn/qikan/manage/wenzhang/20110111.pdf>



Silicon PMs (Geiger-APDs) readout



E. Villela et al. NIM A 2010

Readout electronics for low dark count pixel detectors

Quenching resistor: high value

Inhibit / Reset switches

Inv

Latch

Clk2

NMOS transistor

Switch sensing node to Vdd / Gnd

Shaping to logic levels

Memorize Inv state on clk1

enable latch on the output bus

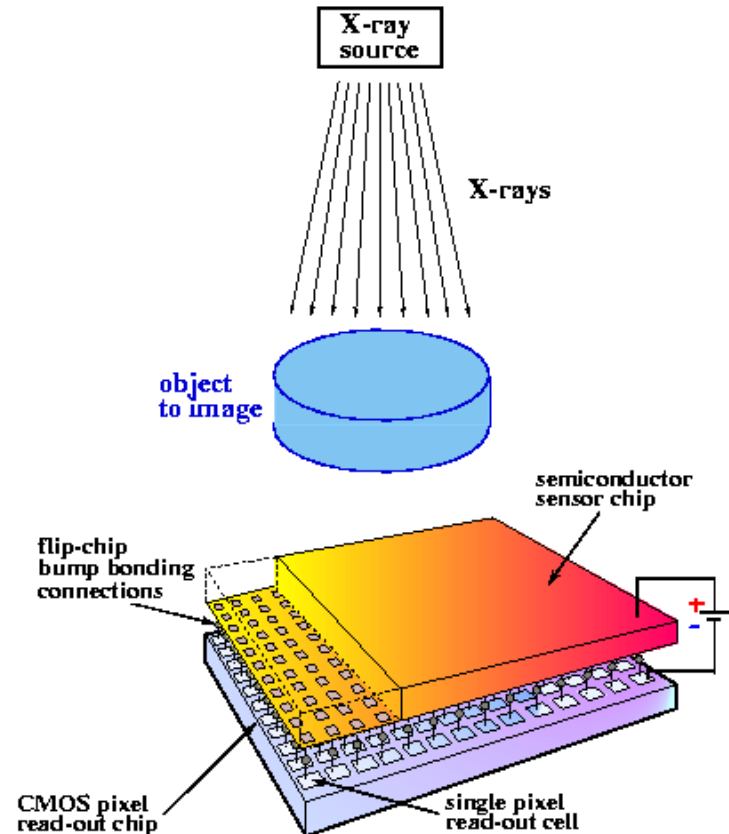
Medipix (EUDET)

MEDIPIX1-3 :

Readout chip to be bonded to an imaging semi-conductor detector (X rays)

- Asynchronous for photon counting,
- Time over threshold provides raw energy estimate

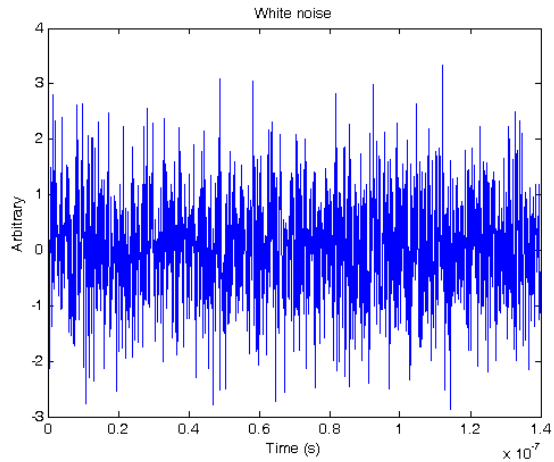
MEDIPIX3: Dead-timeless readout
(two counters, one counts, one is read)



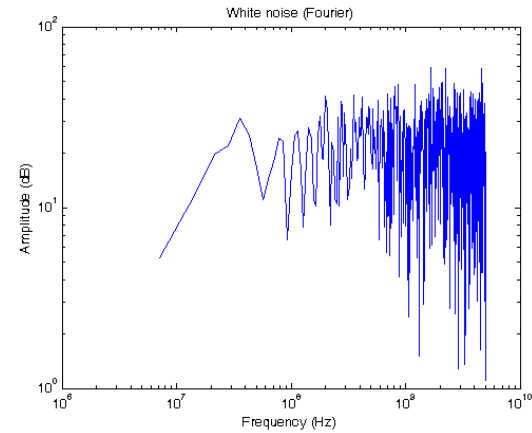
MEDIPIX Website

- Introduction
- Contexts
 - High Energy Physics
 - Space, Medical
- Photodetectors
 - Vacuum
 - Solid state
- Photodetectors Electronics
 - Components
 - Technologies
 - Photon counting
 - Amplitude, charge
 - Imaging
 - Timing
 - 3D integration
- Conclusion

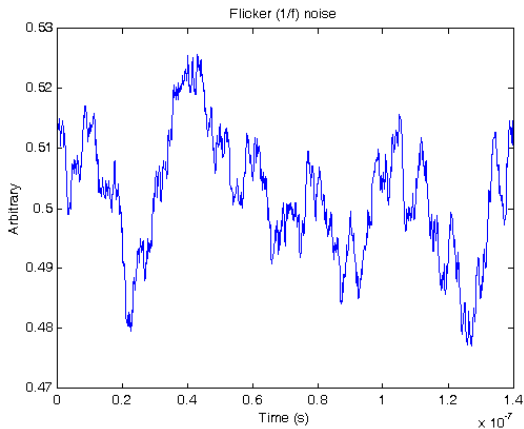
Noise



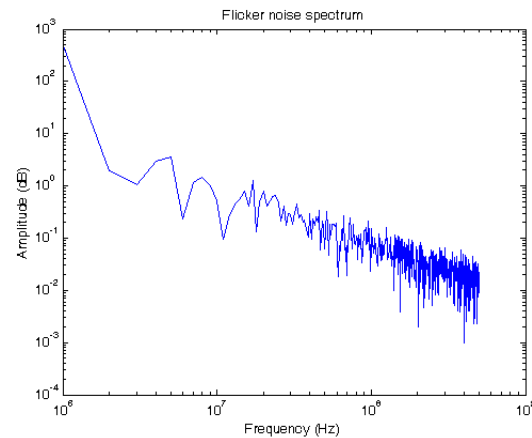
White



Flat spectral density



Flicker (1/f)



Spectral density S_v is 1/f (log scale)

Total voltage squared noise:

$$V_n^2 = \int S_v(\omega) d\omega / 2\pi$$

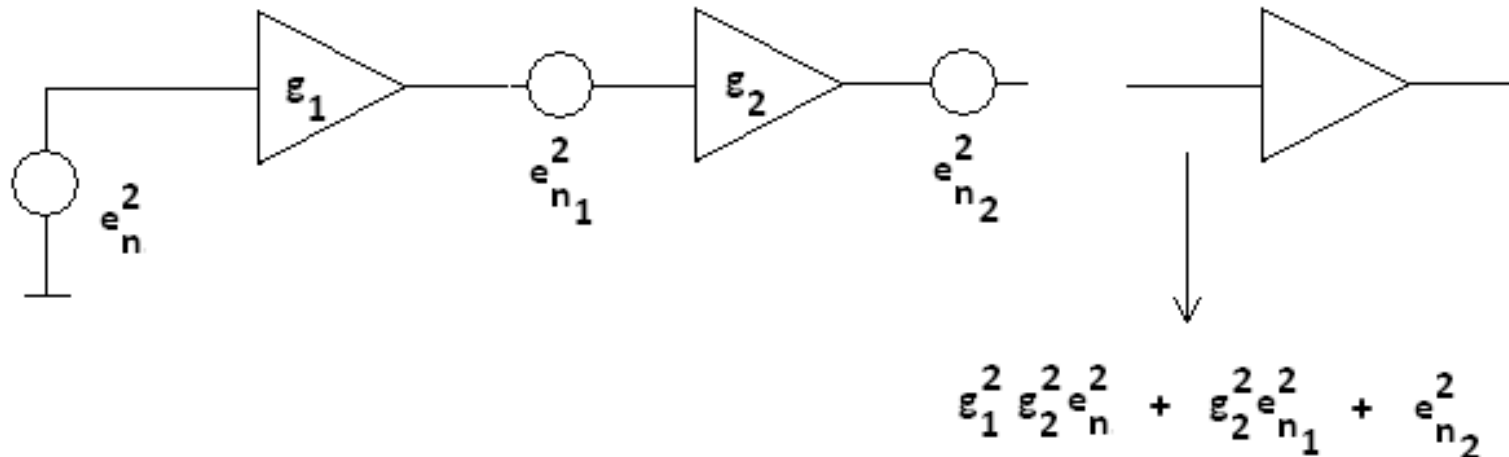
Equivalent Noise Charge

Equivalent Noise Charge:

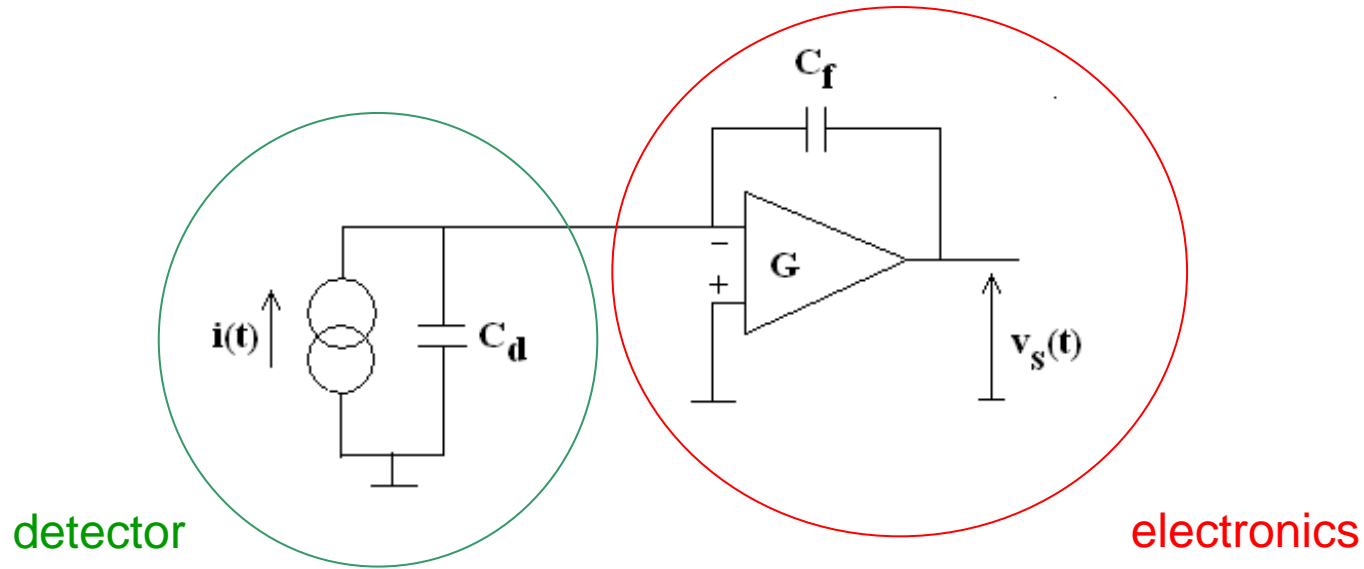
The charge (in electrons) that produces the same rms output as the noise of the full device with no input signal.

The **first stage** of the electronics chain is the **main contributor** to the output noise since it is multiplied by the whole gain of the chain.

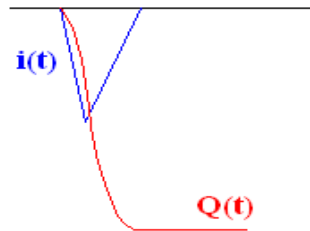
Subsequent noise contributions are multiplied by the product of last gains only



Amplification: Ideal charge sensitive amplifier



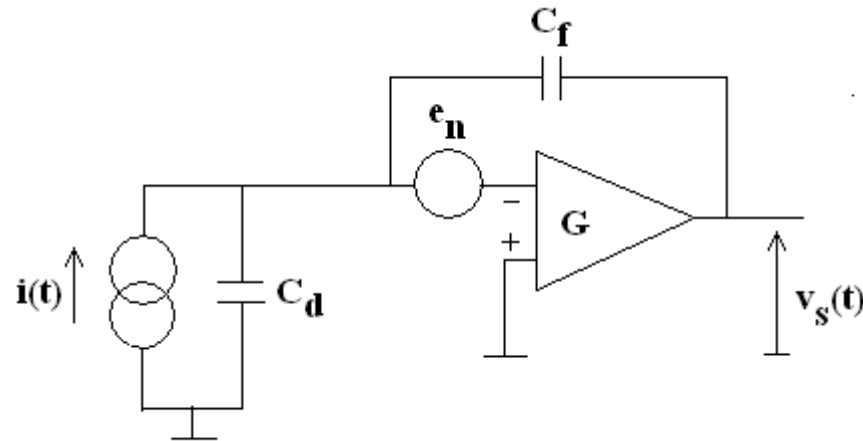
$$v_s(t) = \frac{-\int i(t) dt}{C_f + (C_f + C_d)/G} \approx \frac{-\int i(t) dt}{C_f} = -\frac{Q(t)}{C_f}$$



Charge sensitive amplifier

Serial noise

Serial noise: preamplifier
first stage



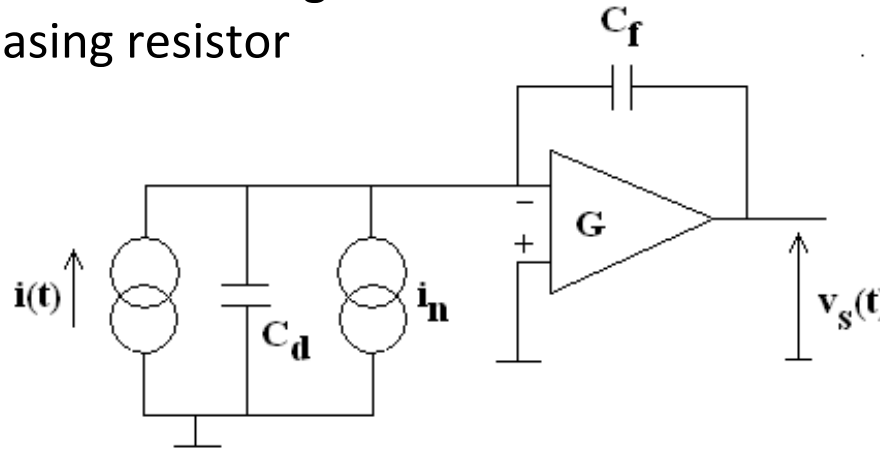
$$v_s(t) = \frac{-\int i(t) dt + e_n C_d}{C_f + (C_f + C_d) / G} \approx = \frac{Q(t) + e_n C_d}{C_f}$$

Serial noise is proportional to detector capacitance:
Weighted by C_d/C_f

Charge sensitive amplifier

Parallel noise

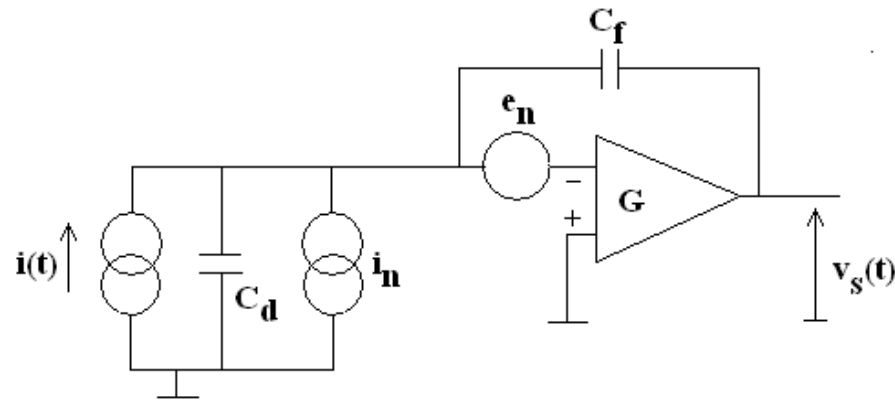
Parallel noise: detector leakages
biasing resistor



$$v_s(t) = \frac{-\int [i(t) + i_n] dt}{C_f + (C_f + C_d) / G} \approx - \frac{Q(t) + \int i_n dt}{C_f}$$

Parallel noise integrated adds to signal

Charge sensitive amplifier Total noise



Noise total spectral density

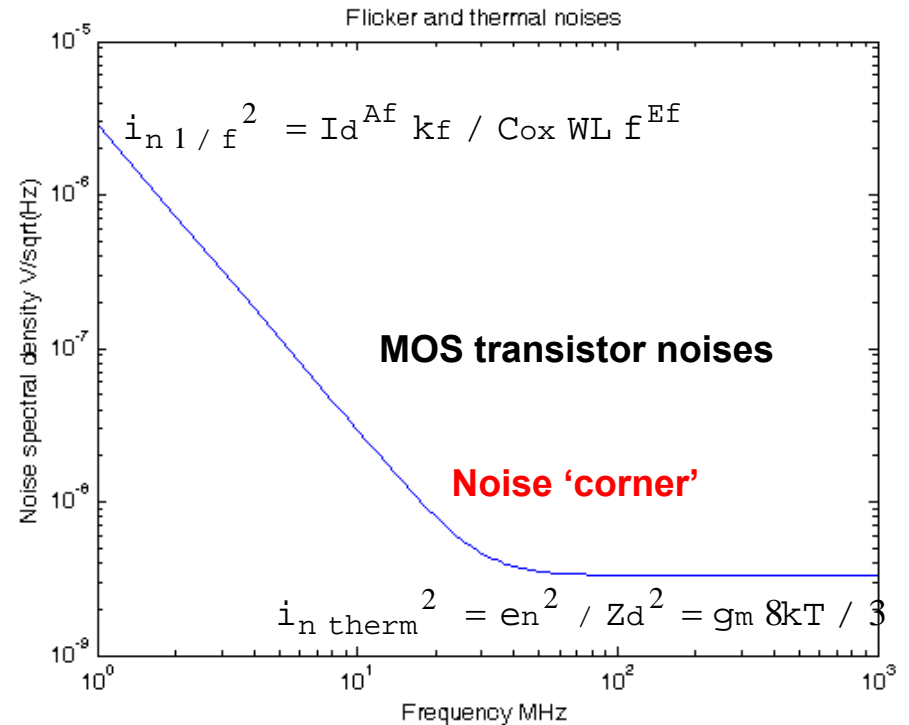
$$V / \sqrt{\text{Hz}}$$

$$S(\omega) = [i_n^2 + e_n^2 / Z_d^2] / \omega^2 C_f^2 = i_n^2 / \omega^2 C_f^2 + e_n^2 C_d^2 / C_f^2$$

Parallel noise = $1 / \omega^2$

Serial noise flat

$$\text{noise rms} = \sqrt{\int_0^\infty S(\omega) d\omega / 2\pi}$$



Input transistor sizing

Noise is mainly produced in the input stage, as it is multiplied afterwards by the gain of the other stages
The input transistor is critical

MOS transistor Inversion regimes:

Strong linear : $V_{GS} > V_{th}$ and $V_{DS} < (V_{GS} - V_{th})$

$$I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

Strong saturation: $V_{GS} > V_{th}$ and $V_{DS} > (V_{GS} - V_{th})$

$$I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_{th})^2 (1 + \lambda(V_{DS} - V_{Dsat})) \right]$$

Weak: $V_{GS} < V_{th}$

$$I_d = I_{d0} \exp \frac{V_{gs} - V_{th}}{n V_t}$$

Input transistor sizing

Reduce power going from strong to moderate-weak inversion

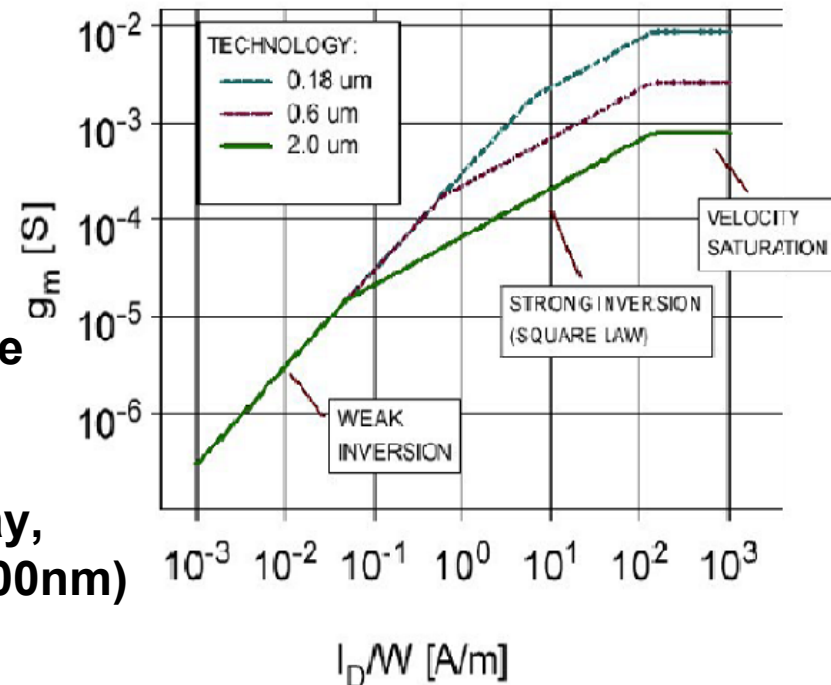
- Strong inversion: g_m proportional to $W/L \sqrt{I_d}$
- C_{gs} proportional to WL
- ENC proportional to $(C_{det} + C_{gs}) / \sqrt{g_m}$
- Optimum W/L : $C_{gs} = 1/3 C_{det}$
- Large transistors are easy in moderate/weak inversion at low

currents

Optimum size in weak inversion

- g_m independent of W , L , proportional to I_d
- ENC minimal for C_{gs} minimal, provided the transistor remains in weak inversion

MOSFETs models are pretty accurate today,
even for deep submicron processes ($L < 100\text{nm}$)



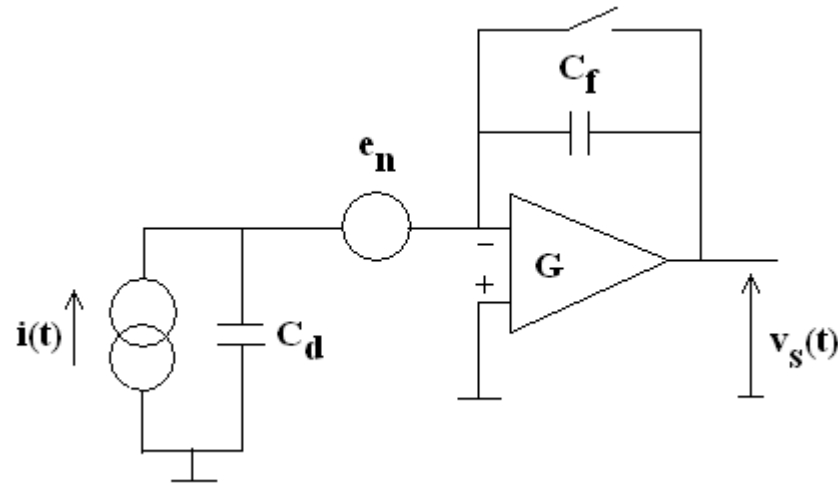
Example: Cd(Zn)Te Xrays detectors readout

16 x 16 pixels readout (camera of 2048 pixels / 8 cm²)

- **32-channel front-end self triggering**
- **RC² shaper**
- **Peak detector**
- **Baseline holder (pulses have a long tail due to slow holes in CdTe)**
- **Variable gain stage, 50, 100, 150, 200 mV/fC**
- **ENC=68 e⁻ at 5.4 μ s peaking time and 2 pF input capacitance to achieve 1 keV FWHM energy resolution at 60 keV**
- **1 MeV dynamic range**
- **Discriminator, DAC threshold**
- **AMS 350nm**
- **SEL Radiation hard library**
- **0.8 mW / channel**

IdEFX Saclay

Charge amplifier reset

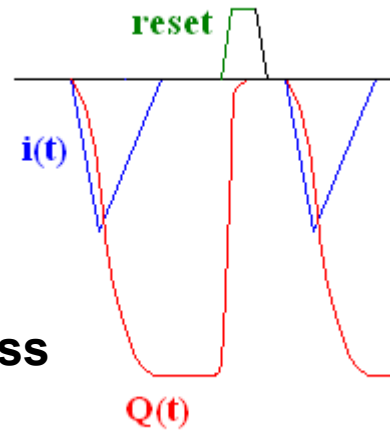


detector

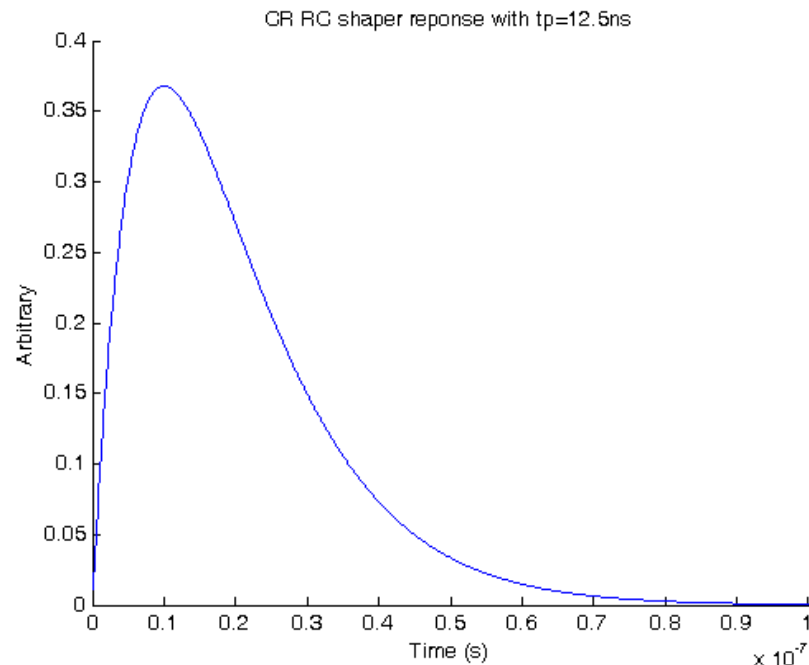
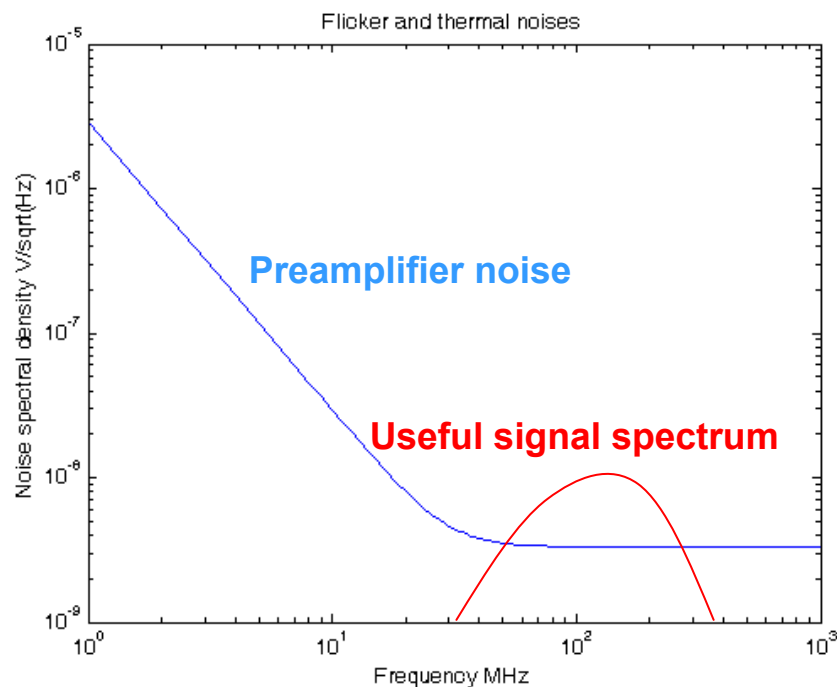
electronics

Reset switch:

- MOS transistor: kT/C noise
- Resistance: thermal noise
- Optical pulse: needs opto process



Pulse Shaping



Analog filtering at frequencies that optimize signal/noise
E.g. CR RC, CR RC²

or digitize (if speed and power allow)

Digital filtering

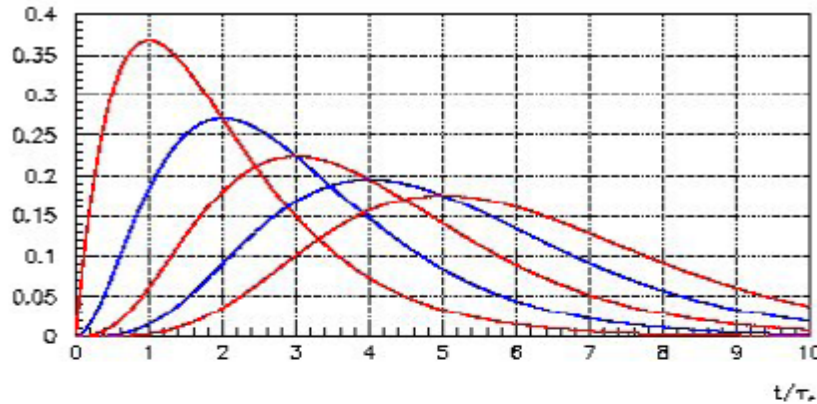
ENC after CR-RCⁿ Pulse shaping

CR: high pass

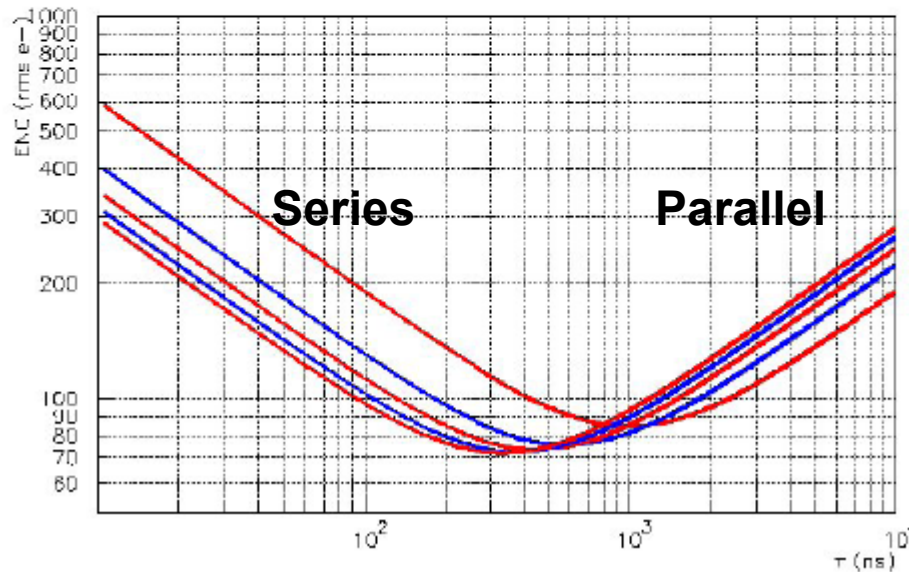
RCⁿ: low pass

**Limit $n \rightarrow \infty$
is gaussian**

**But higher
order filters
have
drawbacks
(noise...)**



Waveform vs shaping time

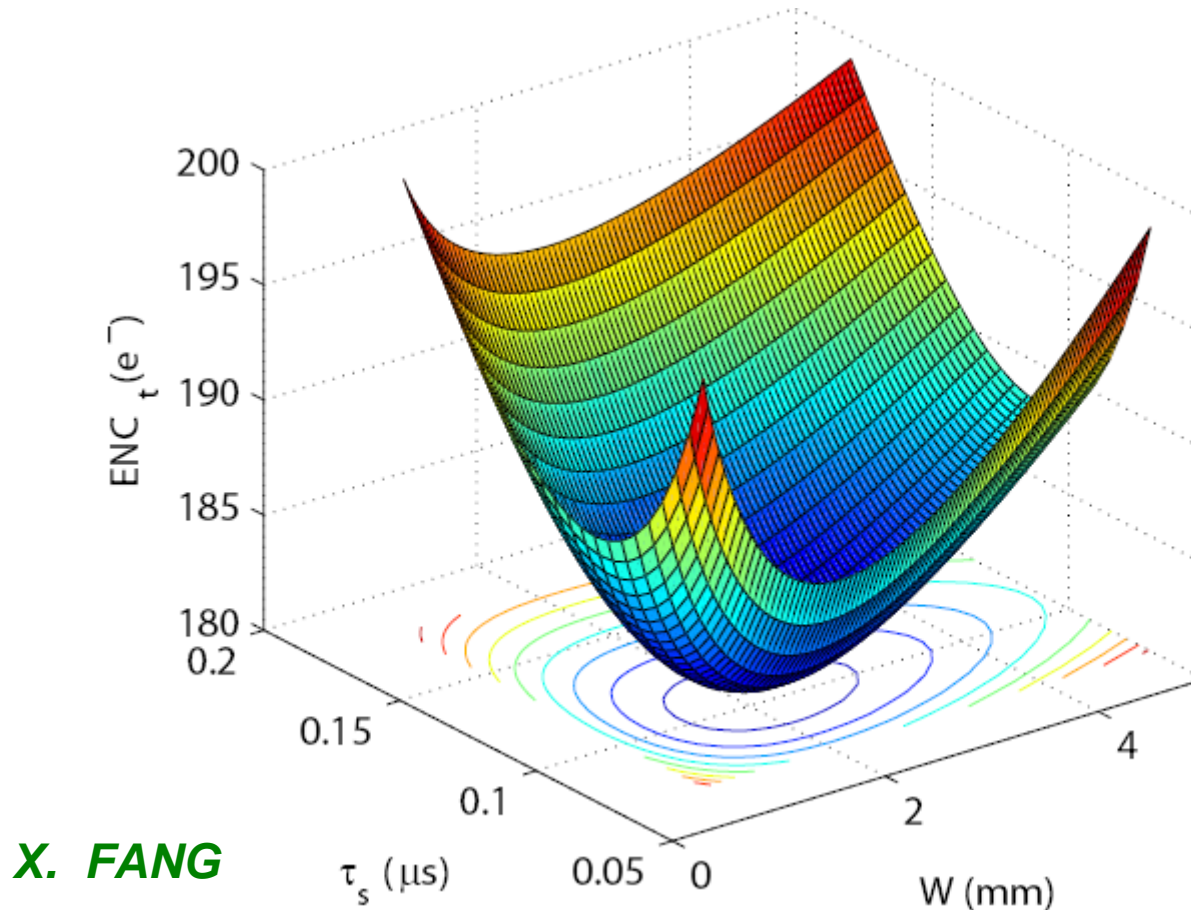


ENC vs shaping time

Series noise in $1 / \sqrt{\tau}$ Parallel noise in $\sqrt{\tau}$ 1/f noise independent of τ

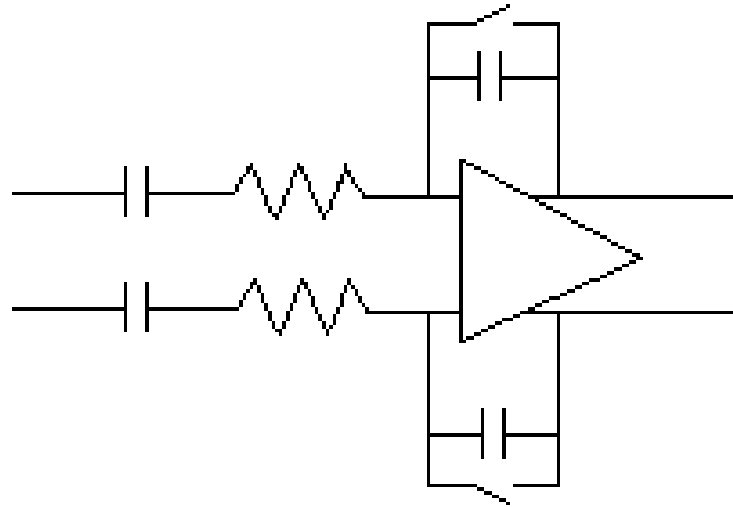
ENC optimization in sub-micron CMOS

Example: Charge amplifier for Avalanche Photo-Diodes readout



Exemple of noise minimization vs shaping time and width of the input transistor
 $\tau_s = 136\text{ns}$, $W = 2\text{mm}$

Switched Integration



- Convolution with a window function (Band-pass, Sinc)
- The switch is implemented easily (instead of large resistors)
- Fast reset: no pile-up
- Needs synchronous operations
- Performance similar to $CR-RC^n$

Transimpedance amplifier

Gain = R $V_s(\omega) / I_{\text{det}}(\omega) = \frac{-R}{1 + Z_f / GZ_d}$

High counting rate

Typically used for optical link receivers

Easily ringing with capacitive detector

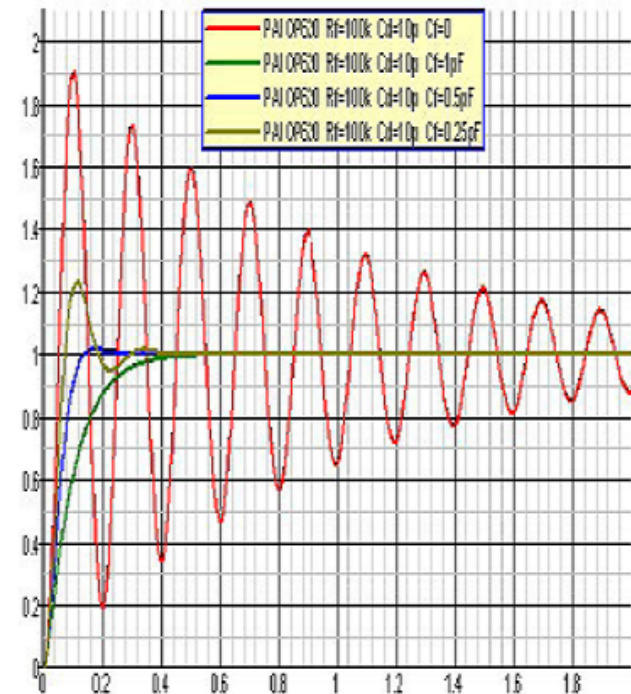
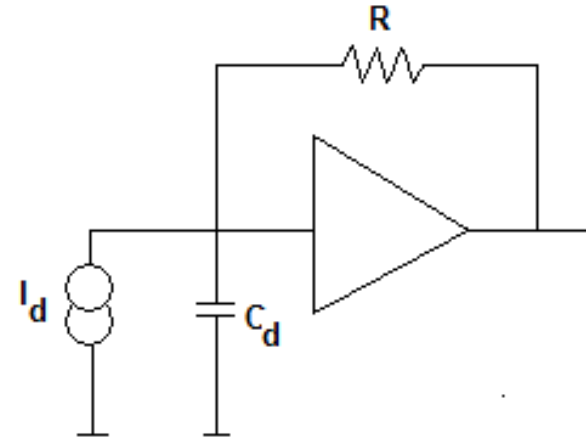
Inductive input impedance $L_{\text{eq}} = R / \omega_c$

Resonance at : $f_{\text{res}} = 1 / 2\pi \sqrt{L_{\text{eq}} C_d}$

**Quality factor: $Q = R / \sqrt{L_{\text{eq}} / C_d} Q > 1/2$
induces ringing**

Damping with capacitance $C_f = 2 \sqrt{\frac{C_d}{RG\omega_0}}$

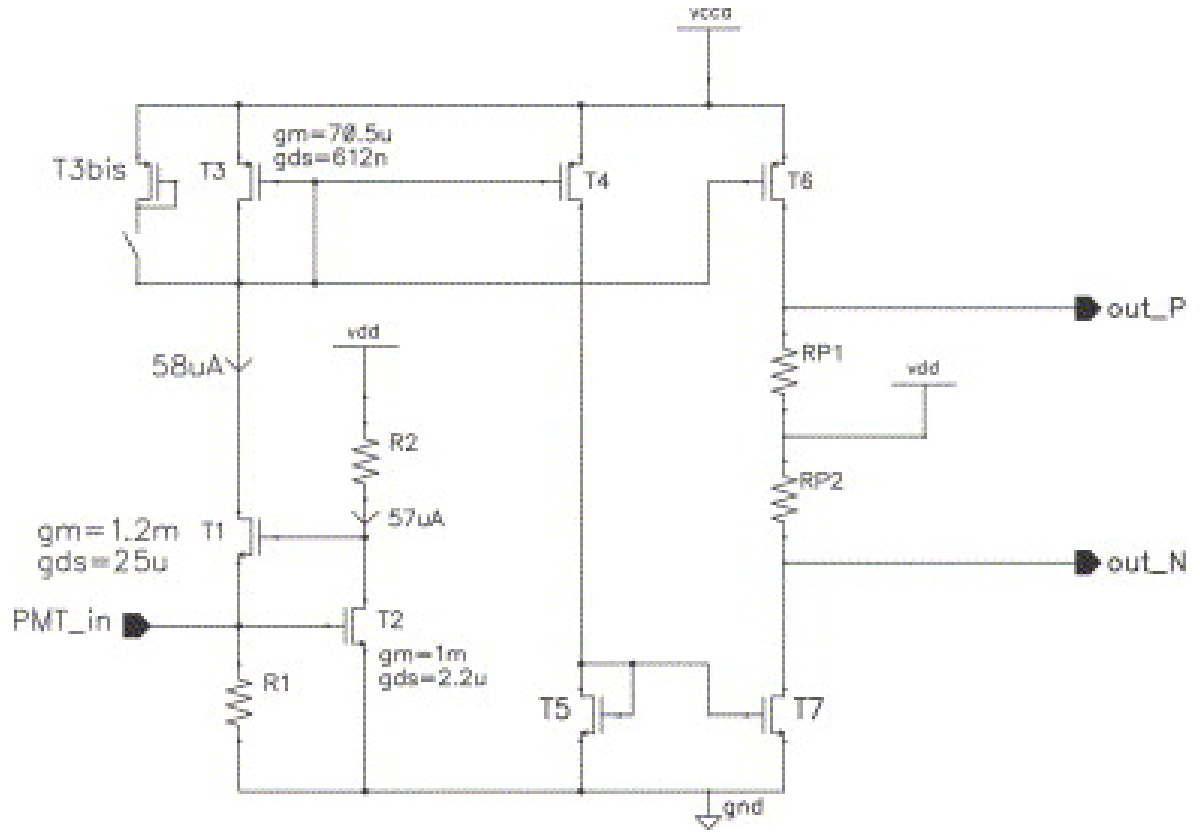
Easier with fast amplifiers



C de la Taille

Current conveyor

- Very low input impedance: less sensitive to crosstalk, electromagnetic interferences
- Differential output



J. Lecoq



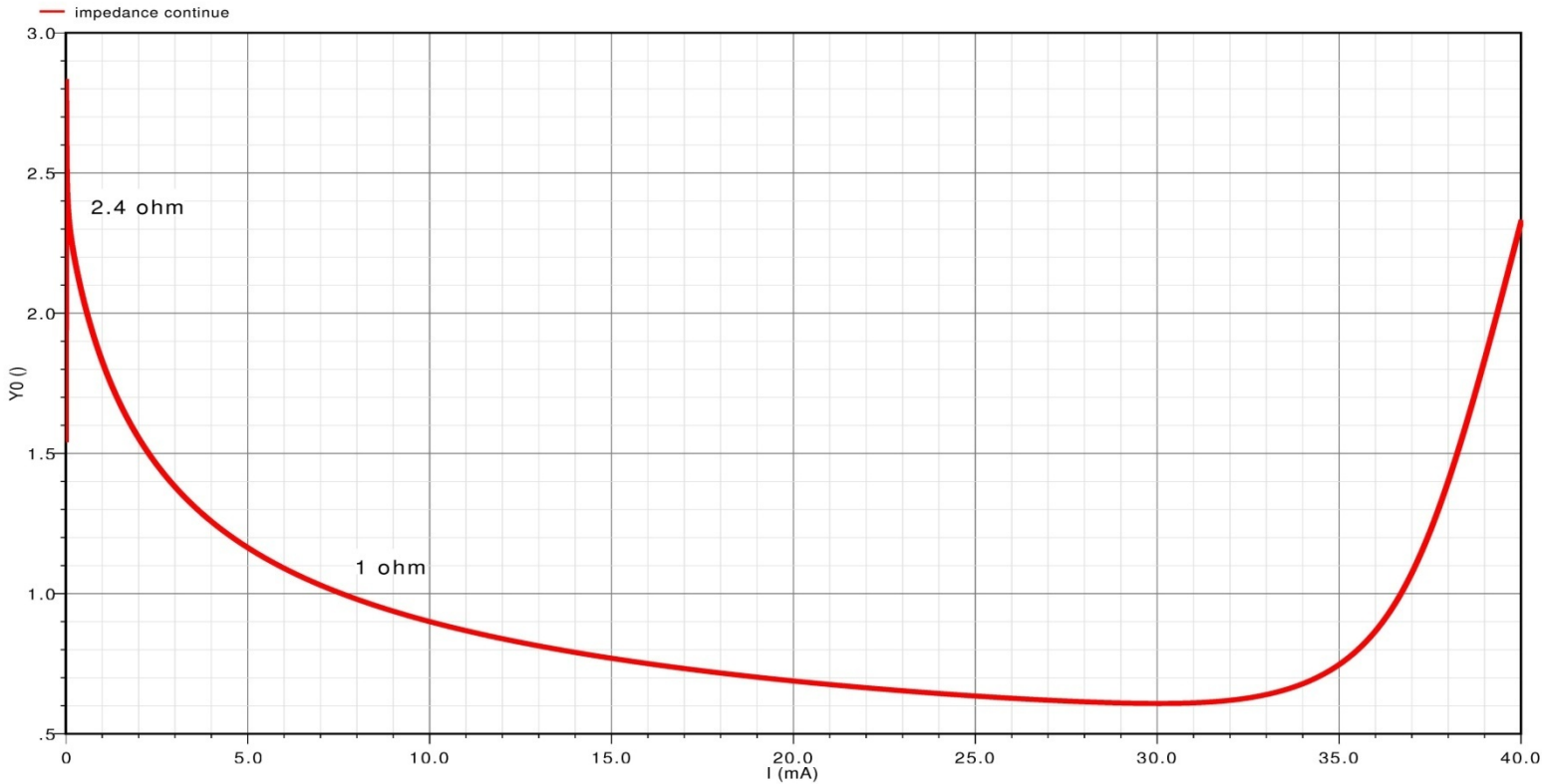
Input impedance versus magnitude



User: bohner Date: Feb 3, 2010 4:55:56 PM CET Graph Window 22

Feb 3, 2010

Y-1



J. Lecoq

Charge vs Current preamplifiers

Charge preamps

Best noise performance

Best with short signals

Best with small capacitance detectors

Current preamps

Best for long signals

Best for high counting rate

Significant parallel noise

C de la Taille

Guidelines for low-noise design

Noise

- Reduce detector capacitance
- Avoid as much as possible connectors and cables, try to digitize on front-end
- Increase the first stage gain keeping matching with C_{det}
- Shape at the optimum peaking time

ADCs (see J. Lecoq presentation in 2007)

Ramp ADCs

Convert to time (TDC). Compare level to a ramp until trigger.

Very effective if many channels in parallel (switched capacitors arrays)

A few MHz at more.

- 1 comparator/channel

- 1 common (Gray) counter

- 1 ramp generator

Can be speeded up using an analog feedback from already eliminated codes

Successive approximation (SAR)

Compare level bit after bit to bit-voltages references..

Subtract the winner bit up to LSB.

Faster by $N/2N$ Conversion times 1-10 MHz

- 1 shift register

- 1 digital to analog converter/channel

- 1 subtractor/channel

- 1 comparator/channel

Flash ADCs

Compare level to all possible codings generated from a voltage divider bridge

Very heavy, power hungry, but very effective

GS/s speeds

- 2^N comparators/channels

- Encoding logic

Pipe-line

Digitize on N-bit, subtract DAC encoded result

Multiply residual by 2 to a next identical stage, up to LSB 64

- N-bit ADC

- 1 multiplication by 2

- 1 comparator

ADCs

it fractional

Pipe-line structure, with two thresholds/bit to manage code borders, delaying decision to the next stage after signal amplified by 2.

Sigma-Delta

Continuously sampling device. One_bit output obtained from comparison between the integral of the previous differences between level and this normalized bit-output. Output oscillates when conversion achieved. Average level of the bits stream is proportional to the input signal level. Low pass filter recovers the digital data in binary format

- Very accurate (>20-bit)
- Very slow (kHz range)
- 1 integrator, 1 comparator, 1-bit DAC/channel

These ADC have replaced ramp ADCs

But photo-detection needs mainly ramp ADCs: high channel count to convert in parallel

All ADCs need an input sample and hold device to assert a stable level during conversion

Many hybrid devices, depending on the best case-dependent trade-off between area, power, technology cost e.g. SAR/flash

Photo-detectors

Very application dependent: CCD need parallel operation for column readout, pixels can accomodate one low resolution ADC/pixel

<http://www.in2p3.fr/actions/formation/microelectronique07/porquerolpdf2007.pdf>

Pulse Sampling ADCs, IPs

Trade-off precision / sampling speed / power

Example:

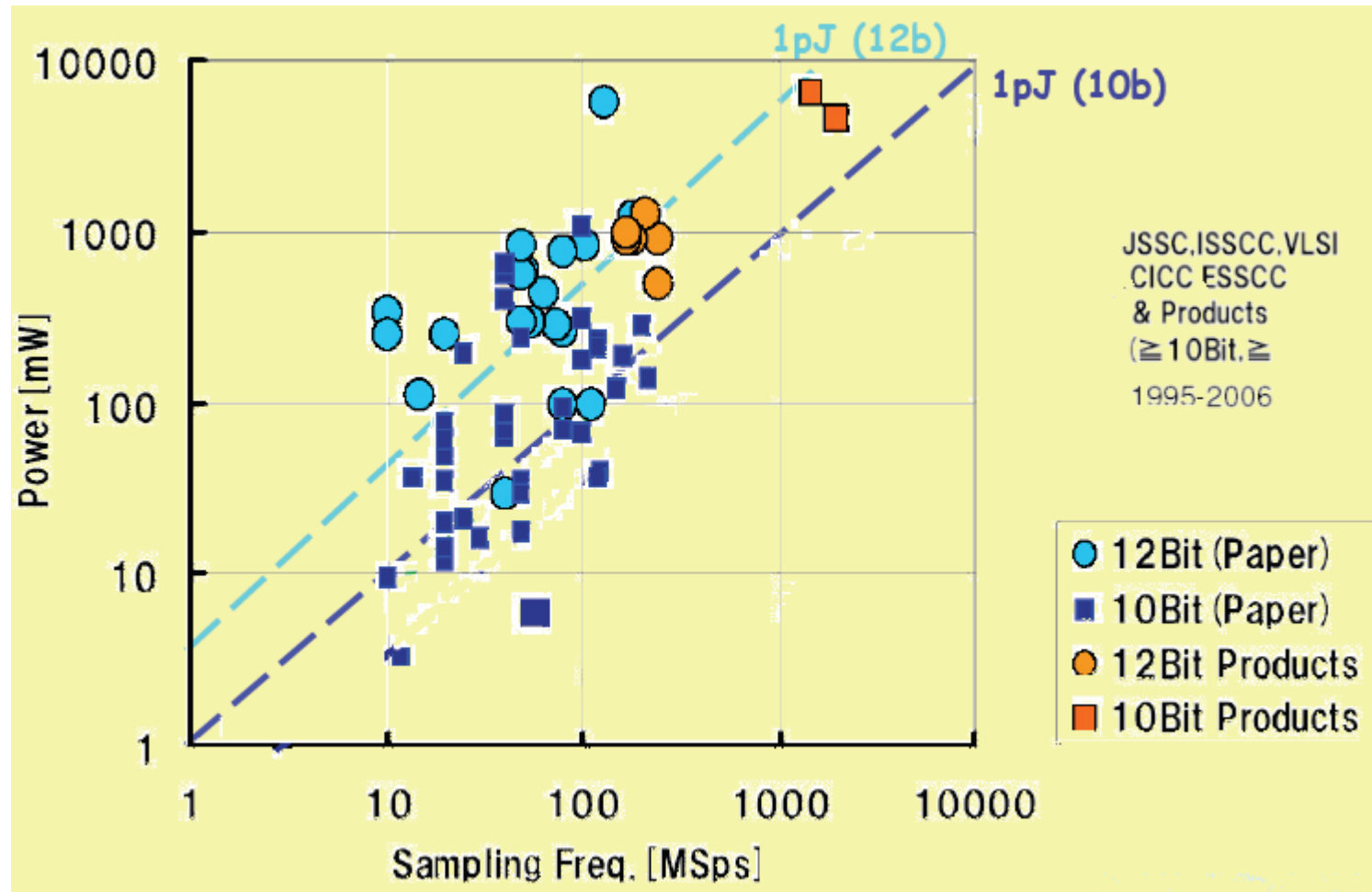
Discrete ADCs on the market

24-b Σ/Δ Dual-slope 16-bit SA + Flash
12-b 3.6GS/s
8-b 56GS/s

Custom IPs:

AMS 350nm	12-b 1MHz		purchased by IN2P3
TSMC 130nm	14-b 150 MHz	300mW	nSilition (Belgium)
SOS 90nm	12-b 220 MHz	50mW	Anacatum (Sweden)
Chartered 350nm	8-b 40 MHz		NTLab (Russia)
IHP BiCMOS 250nm	14-b 25 MHz		NTLab (Russia)
IHP BiCMOS 250nm	2x 12-b 8kHz		NTLab (Russia)
TSMC 130nm	4.25 Gb/s	Quad SerDes	Mixel (USA)
TSMC 28nm	PLL 2-3.6GHz	1ps jitter	Silicon Creation (USA)
Chartered 350nm	PLL 300MHz		NTLab (Russia)

ADCs Power



P. O'Connor

Photo-multiplier readout

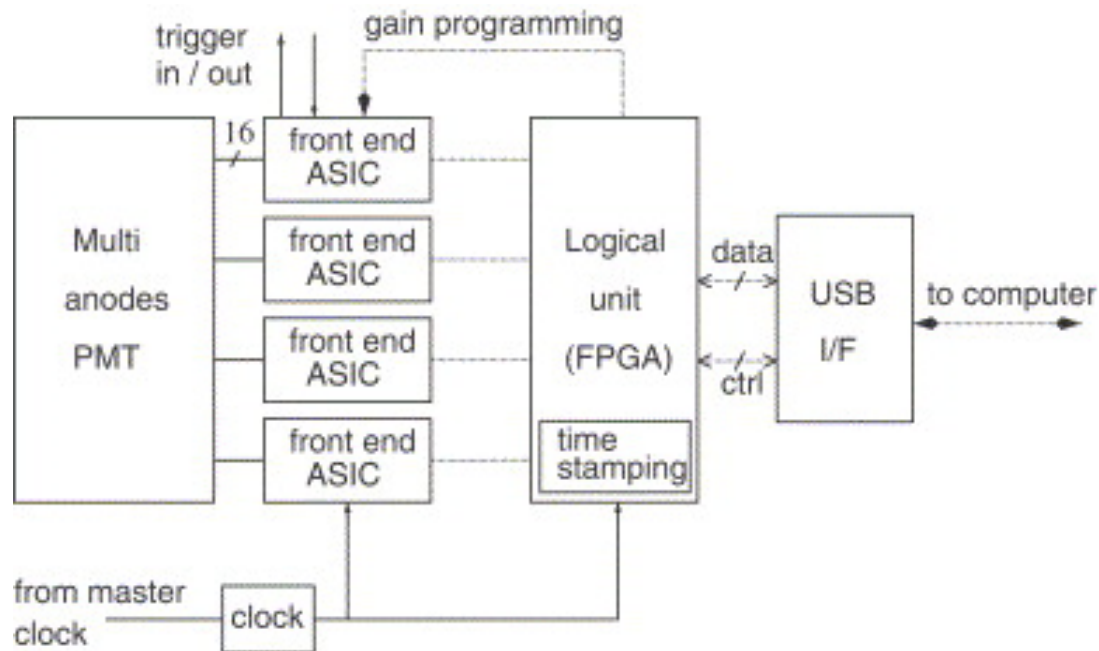
64-anode MaPMT photo-detector

16-channel ASIC in AMS 350nm

Includes:

- Input integrator
- 8_bit ADC
- Parallel to Serial conversion

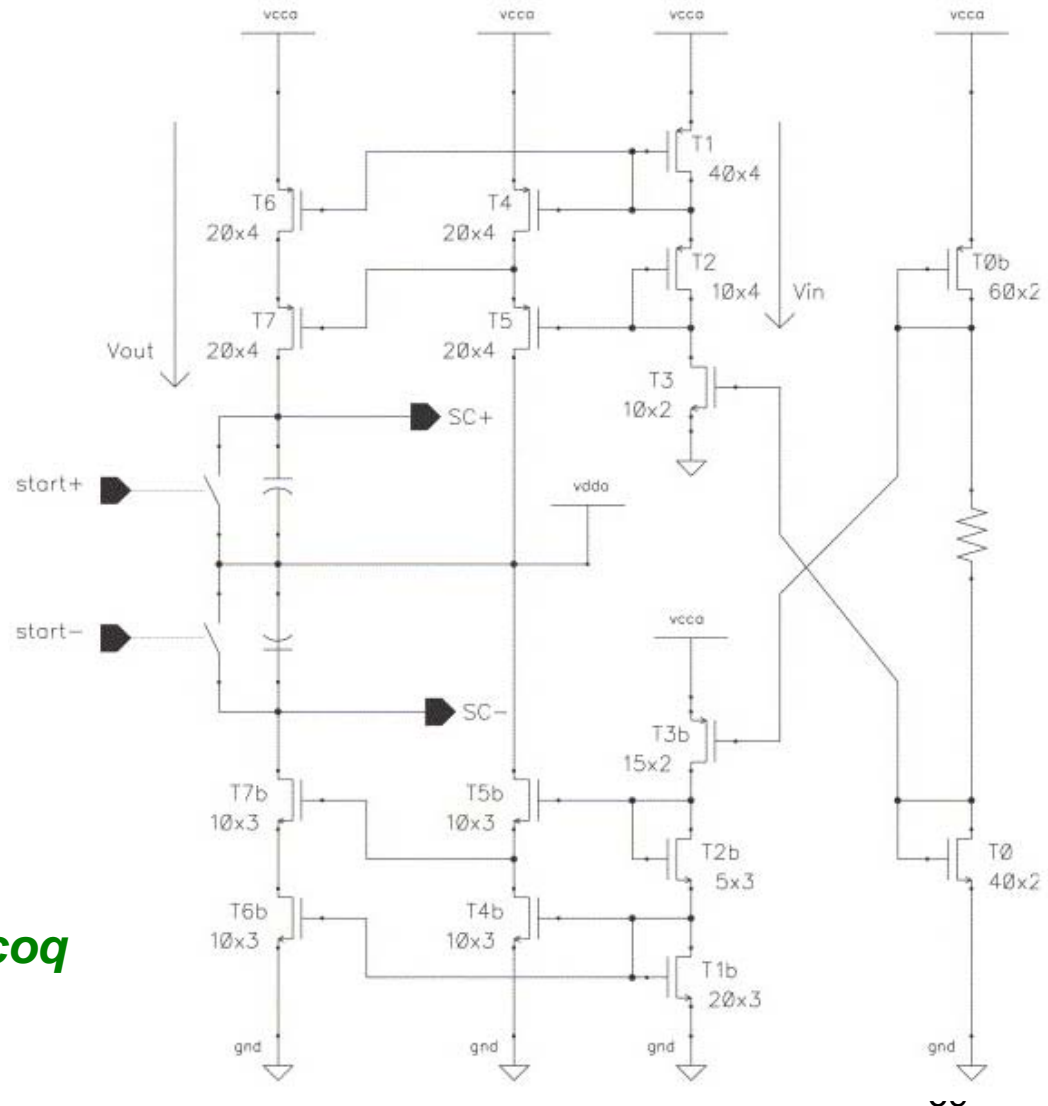
J. Lecoq



CMOS 8-bit ADC ramp generator

- Charge capacitors at constant current
- Cascoded current sources (linearity)
- Two symmetric ramps
- 5.12 μs duration
- 4V range
- Linearity 0.085%

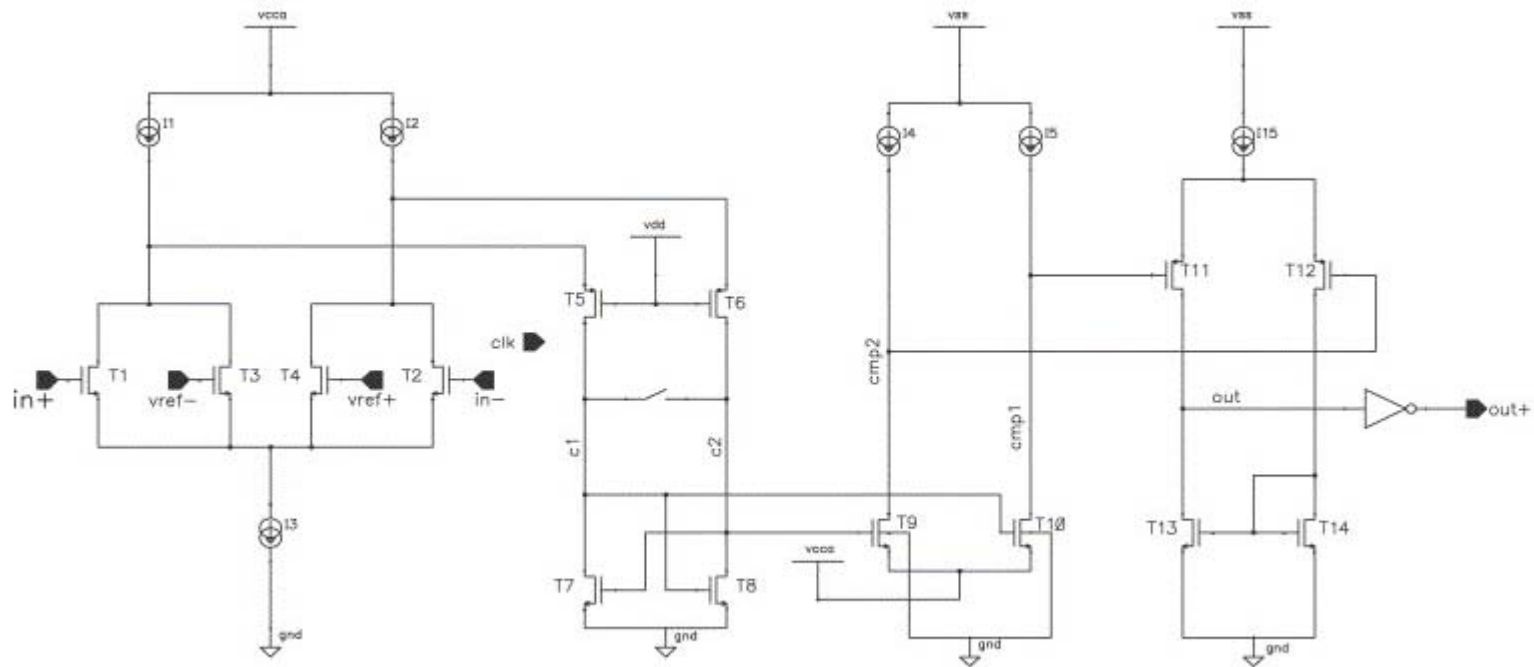
J. Lecoq



CMOS ADC latched comparator

- Differential
- Cascoded
- Positive feedback
- 300 μV sensitivity

J. Lecoq

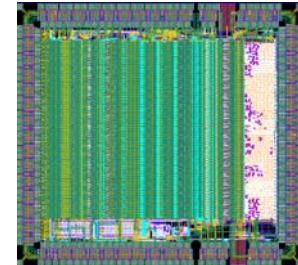


Silicon PMT readout

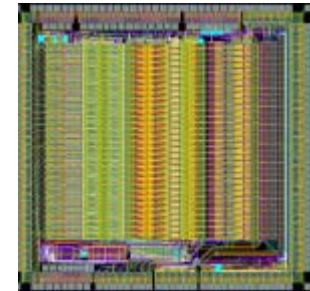
AMS SiGe 350nm technology line from LAL Orsay

C de la Taille

Maroc 64-channel photon counting
1/3 Photo-Electron trigger sensitivity
50fC dynamic range
Tunable slow channel for charge
Tunable fast channel for timing
Internal 8-12 ramp ADC



Easiroc 32 inputs
8-bit DAC for gain adjustment
Two control analog channels
Fast trigger channels for timing
Low power: 5mW/ch



Contact LAL Orsay: P Barrillon

<http://www.omega.in2p3.fr>
(Need registration)

Full Orsay 0.35 μ m SiGe line

Chip	Optimized for	#ch	#triggers	Data type	Outputs
MAROC	MaPMT	64	64	Th Q	1 Q analog + dig
SPIROC	SiPM	36		Th Q t	1 Q analog Dig
EASIROC	SiPM	32	32	Th Q	2 Q analog
HARDROC	RPC	64		Th Q	1 Q analog Dig
MICROROC	MicroMegas	64		Th Q	1 Q analog Dig
SKIROC	PIN diodes	64		Th Q	1 Q analog Dig
PARISROC	PMTs Matrix	16	16	Th Q t	Dig
SPACIROC	MaPMT	64	64	Th Q	9 Q

<http://www.omega.in2p3.fr>

Multi-anode PMT readout (JEM-EUSO)

C. de la Taille

AMS SiGe 350nm technology line from LAL Orsay

Spaciroc 64-channel photon counting for JEM-EUSO
1/3 Photo-Electron trigger sensitivity
10-1500 PE dynamic range
Tunable slow channel for charge
Tunable fast channel for timing
Internal 8-12 ramp ADC
Low power: 1mW/ch required by the ISS

<http://www.omega.in2p3.fr>
(Need registration)

Fast Switched Capacitors Arrays (SCA)

- Fast photo-detectors as Micro-Channel Plates or Silicon Photo-Multipliers signals analysed on-chip as with digital oscilloscopes
- Regular PMTs sampled to 13-bit dynamic range (E. Delagnes, D. Breton)

Principle of SCA ASICs:

Write fast (1-10GS/s)

Read as possible (10-100 MHz)

Digitize all caps in parallel with a ramp ADC

Input discriminator as trigger to stop sampling

Limitations:

Random noise

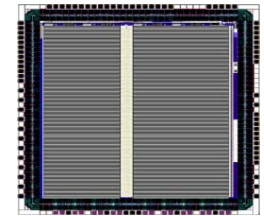
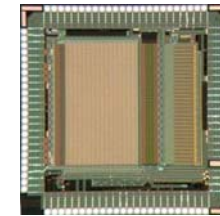
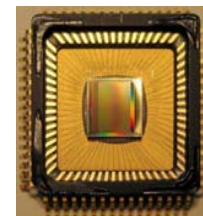
Sample aperture jitter

Sampling timebase jitter

Key component of digital scopes

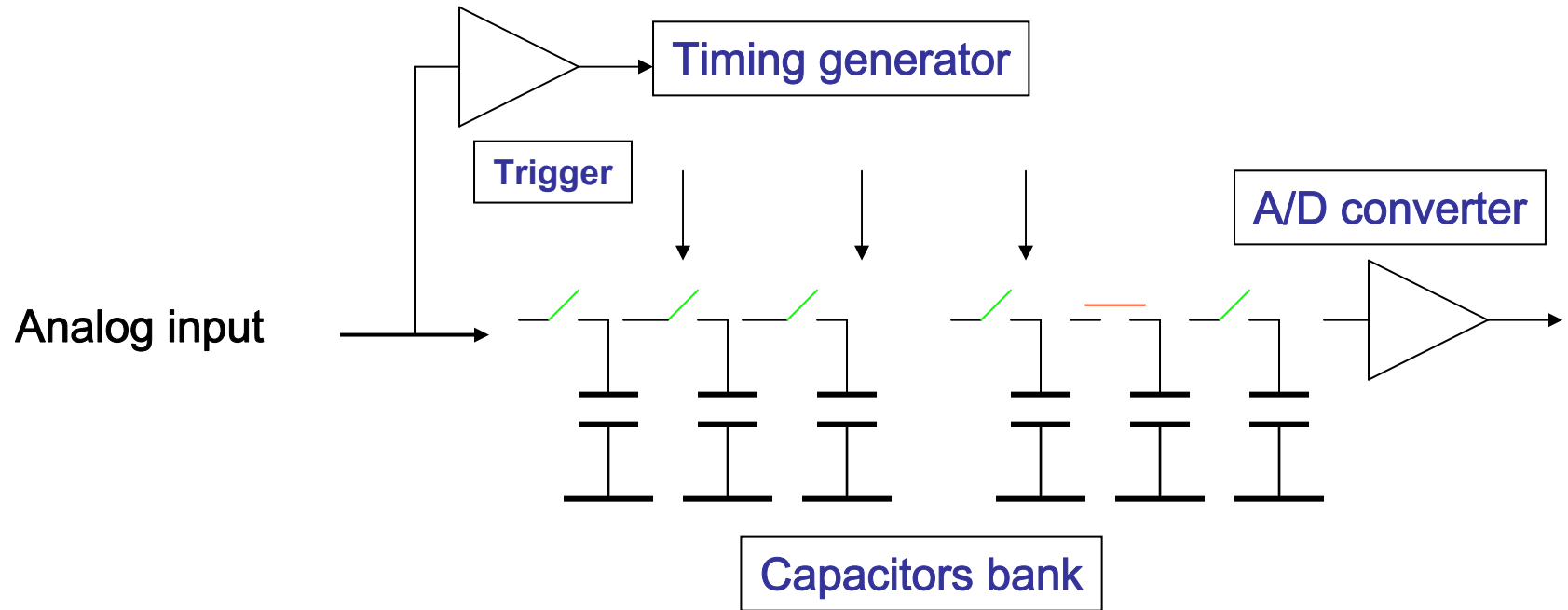
Examples:

DRS4	S. Ritt (PSI)
SAM	D. Breton, E. Delagnes (France)
LAB	G Varner (Hawaii)
PSEC	H Grabas, E. Oberla (Chicago)



6GS/s	850 MHz	250nm
3GS/s	300 MHz	350nm
6GS/s	900 MHz	250nm
15GS/s	600 MHz	130nm

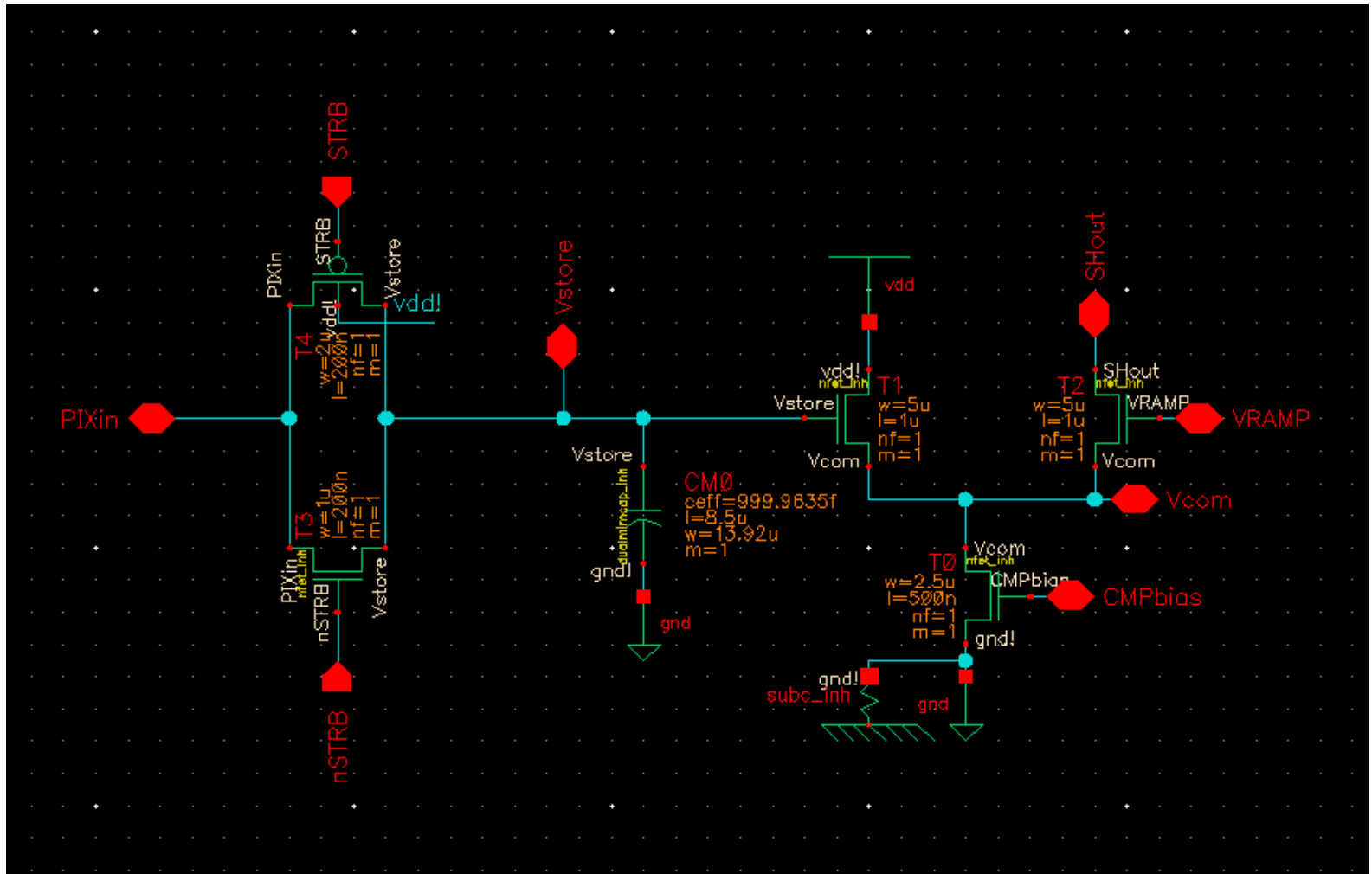
SCAs



Main features:

- **Sampling frequency**
- **Analog bandwidth**
- **Analog dynamic range (ADC bits)**
- **Depth**
- **Readout frequency**

SCA sampling cell



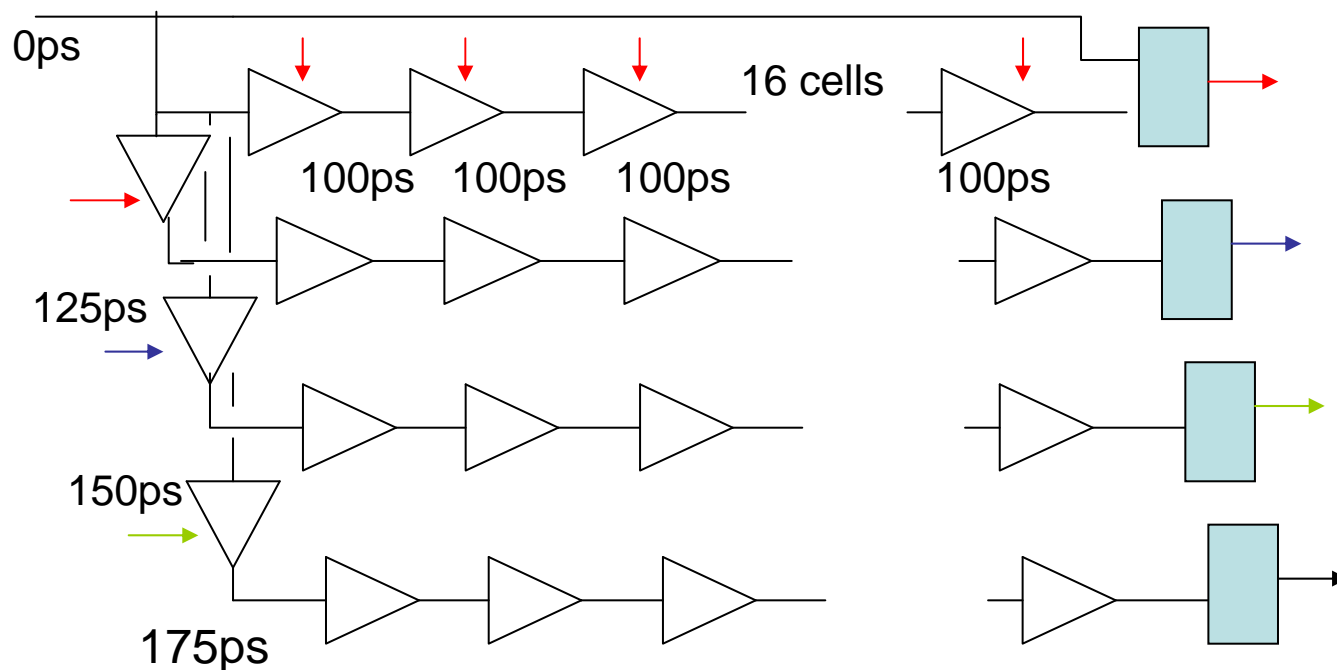
L. Ruckman

Sampling cell + ADC comparator

76

40 GS/s Timing generator

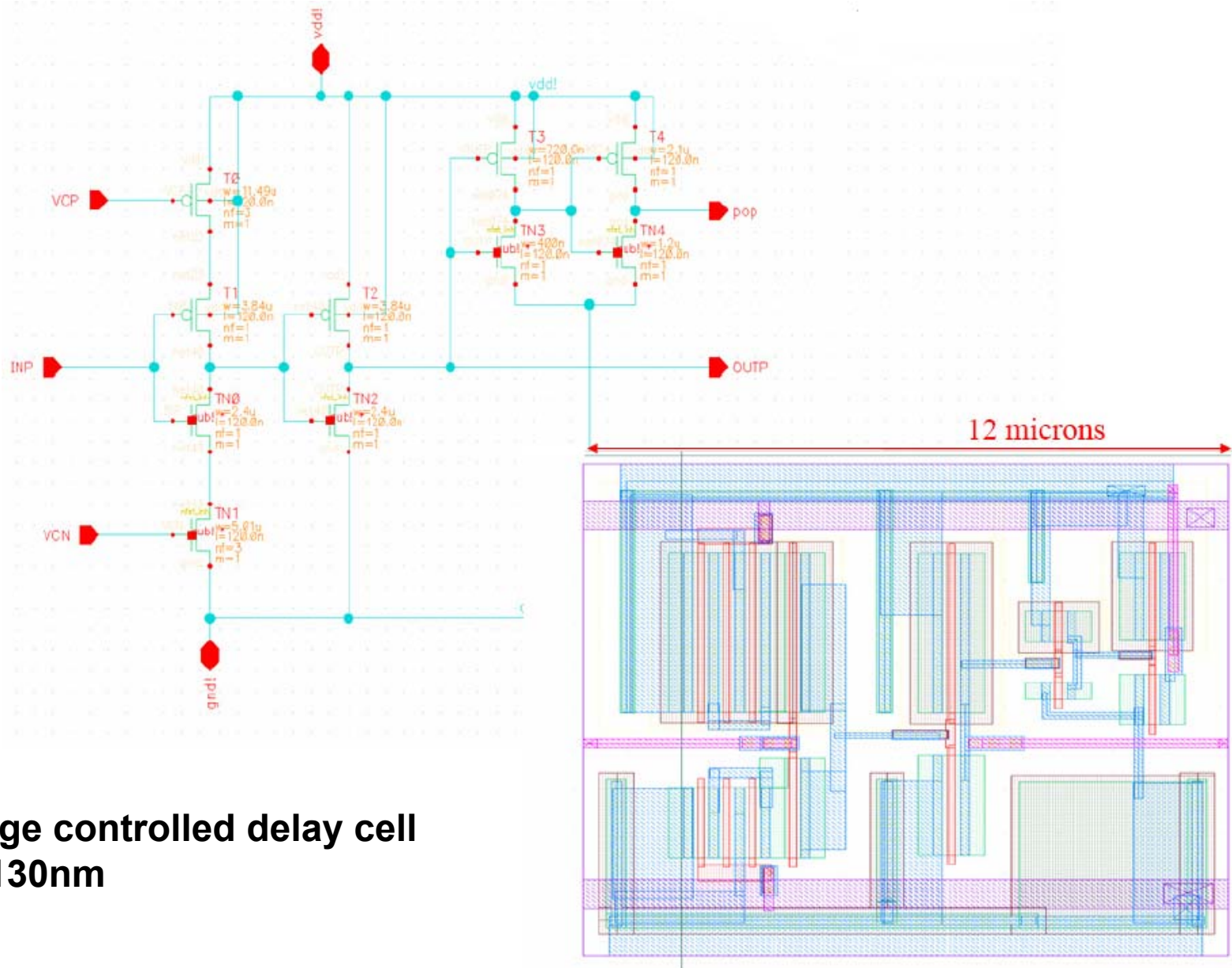
640 MHz clock in



16 x 4 = 64 cells, 25ps step delays

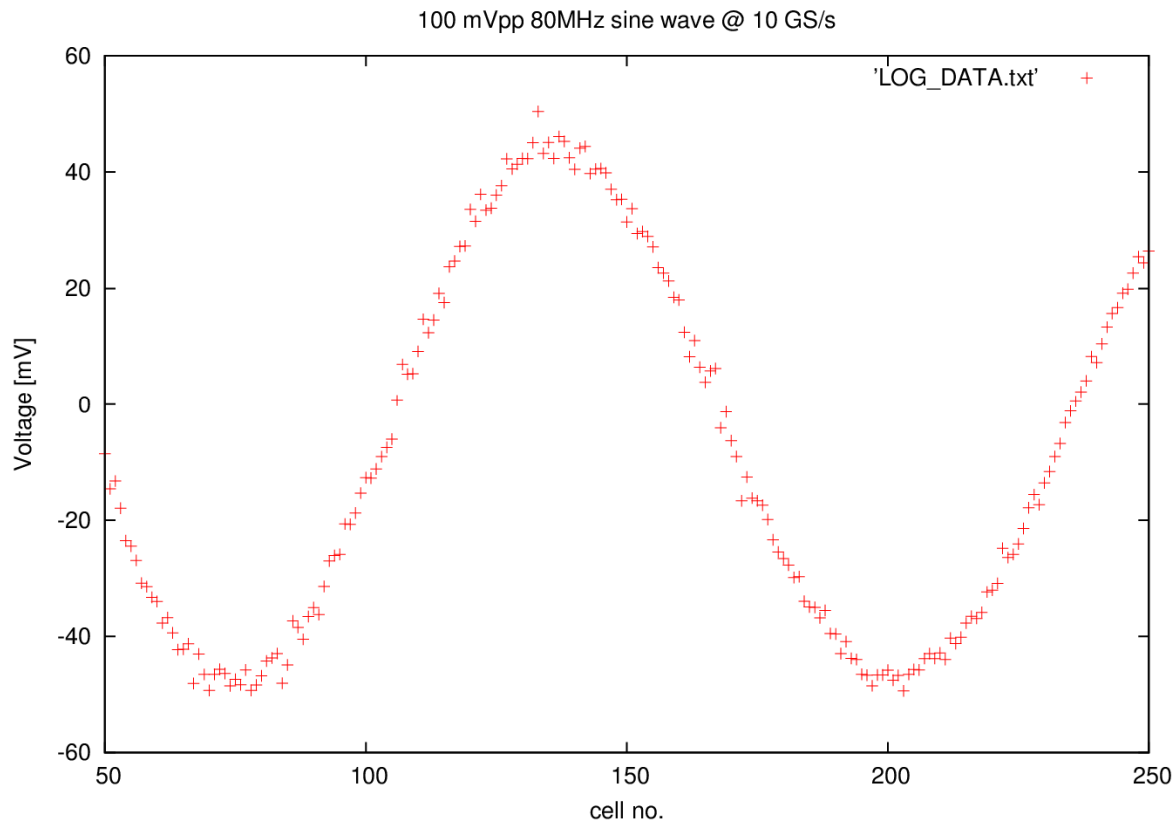
J. Christiansen (CERN)

15 GS/s Timing generator



Voltage controlled delay cell
IBM 130nm

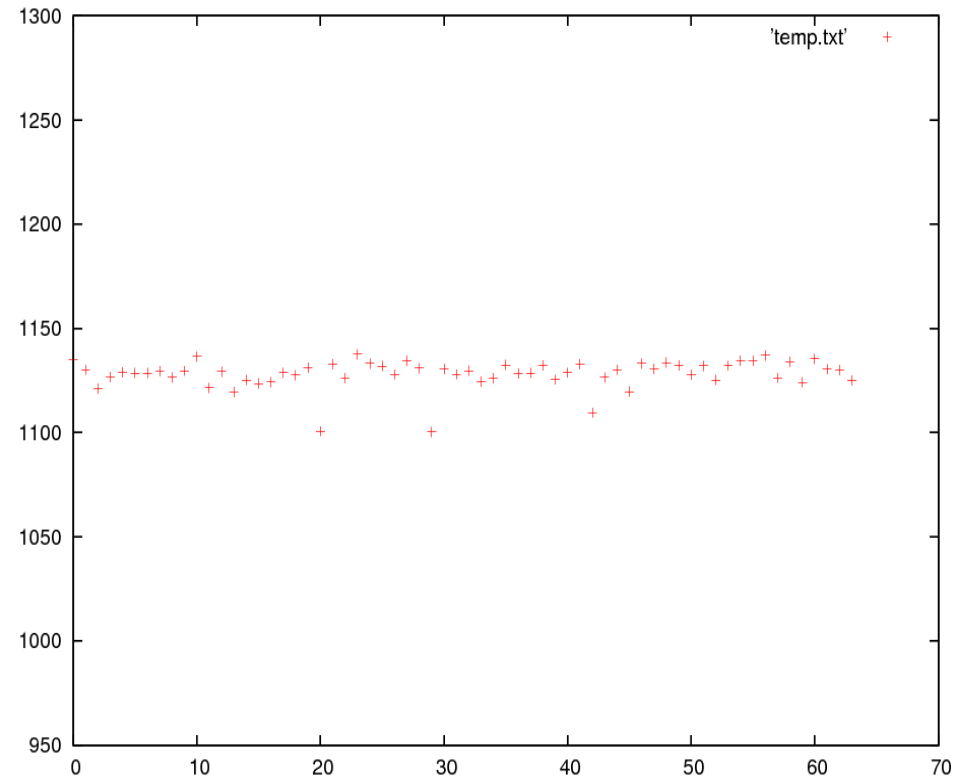
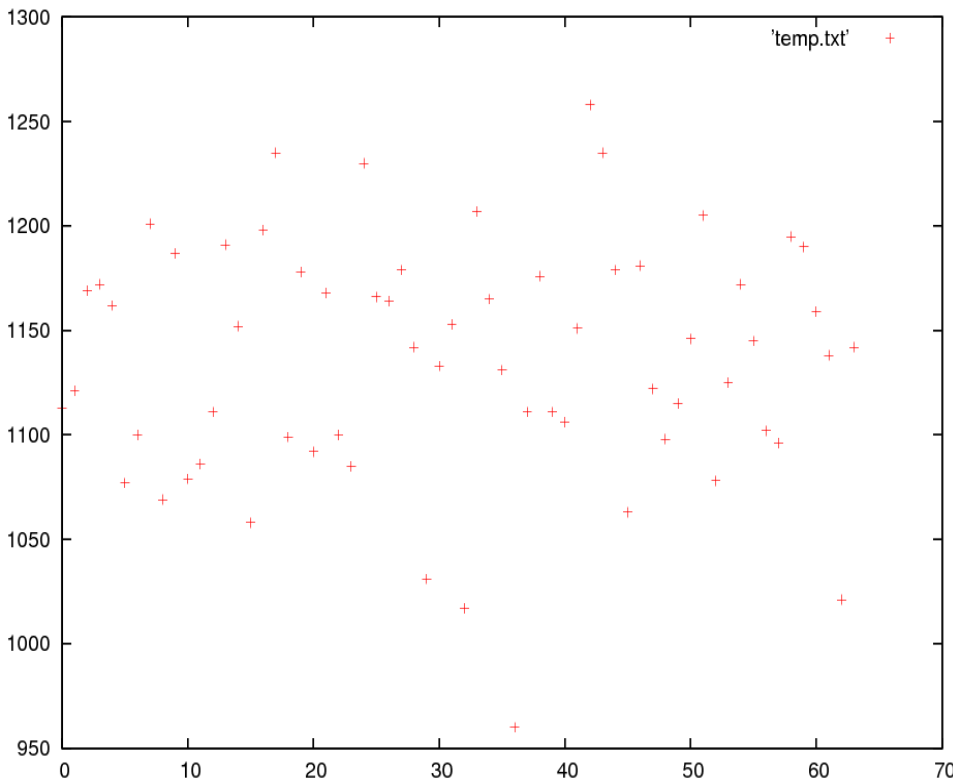
80 MHz sine wave sampled at 10GS/s



**80 MHz, 100 mV pp sine wave sampled
at 10 GS/s, after on-chip digitization and offset corrections**

Eric Oberla (Univ Chicago)

SCA Offsets distribution



Sampled DC value before and after offsets subtraction

Offsets due to voltage threshold spreads (fixed pattern)

Eric Oberla (Univ Chicago)

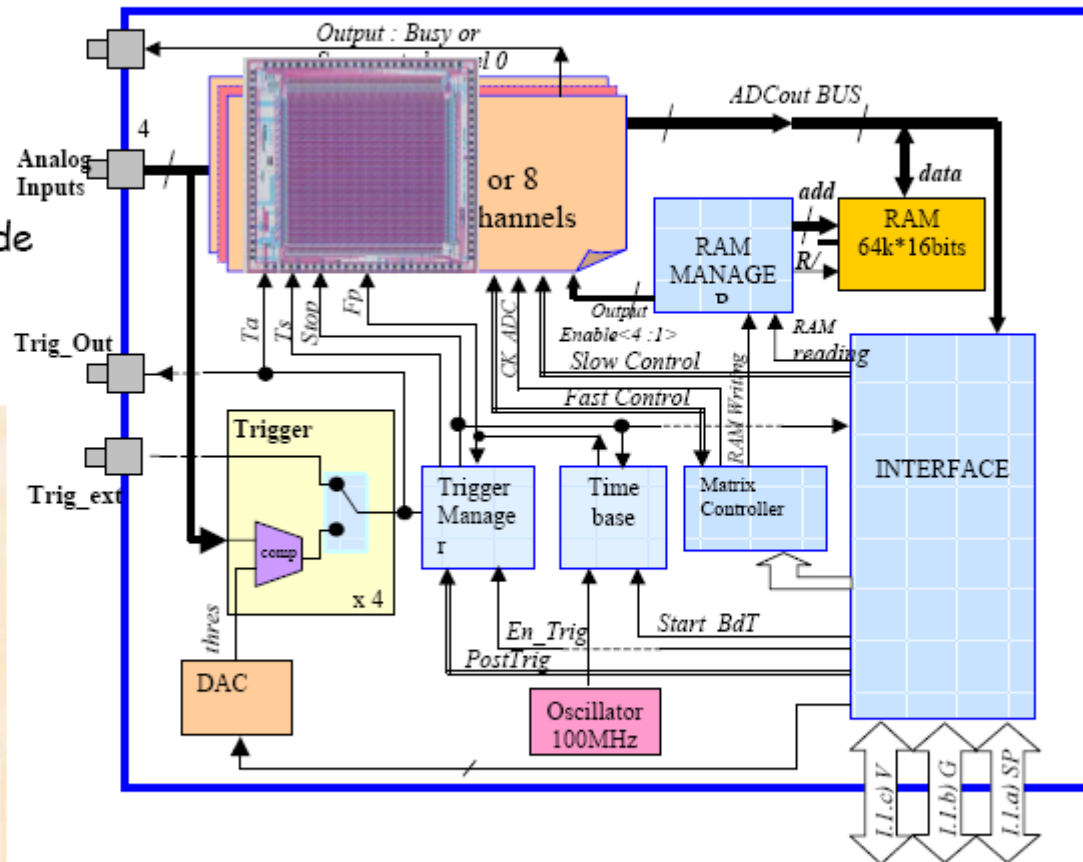
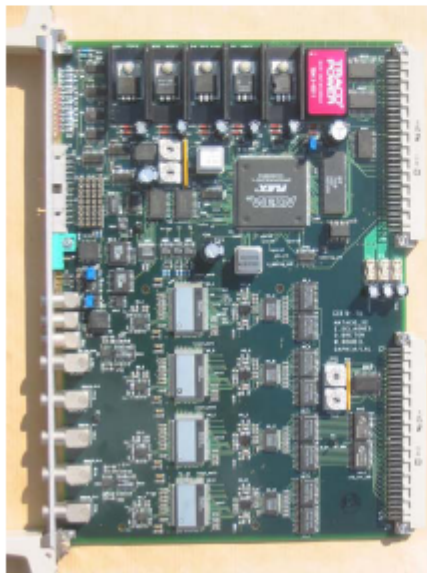
VME board equipped with SCA chips

Pipeline 12b 2GHz

©D. Breton

■ MATAQVME

- VME board with 4-8 channels
- 2 GHz - 12 bits
- Auto-trigger mode
- Sold by CAEN



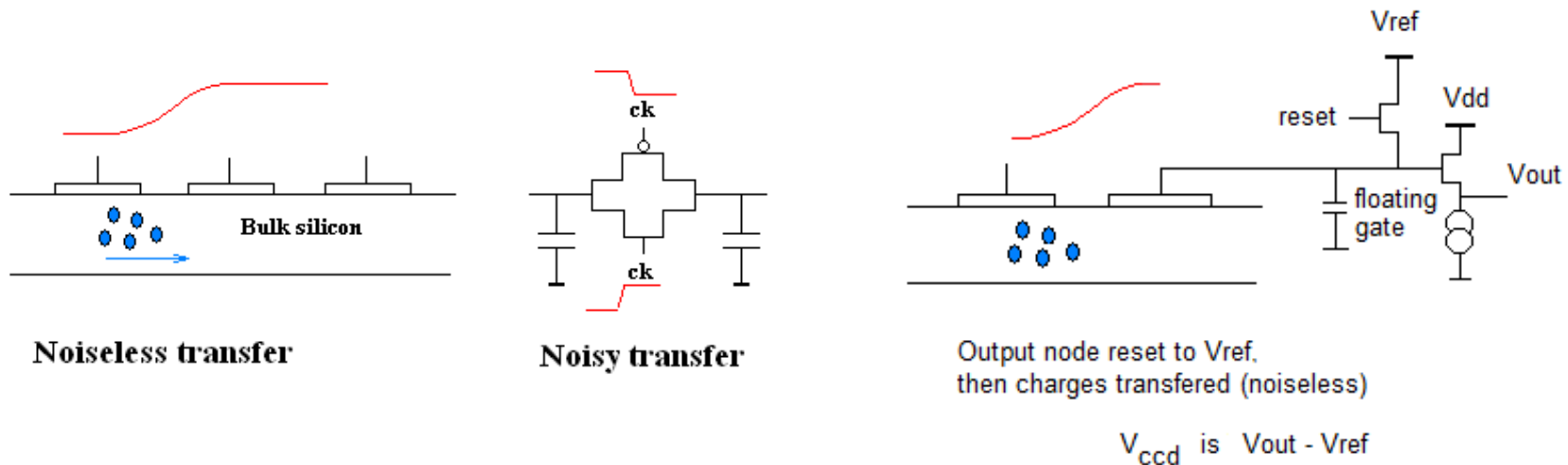
D. Breton, E. Delagnes

- **Introduction**
- **Contexts**
 - **High Energy Physics**
 - **Space, Medical**
- **Photodetectors**
 - **Vacuum**
 - **Solid state**
- **Photodetectors Electronics**
 - **Components**
 - **Technologies**
 - **Photon counting**
 - **Amplitude, charge**
 - **Imaging**
 - **Timing**
 - **3D integration**
- **Conclusion**

Charge Coupled Devices (CCD)

Set of electrodes on top of high resistivity silicon, top or backside illuminated
Scientific CCDs: huge dynamic range (16-bit), single electron sensitivity if cooled.

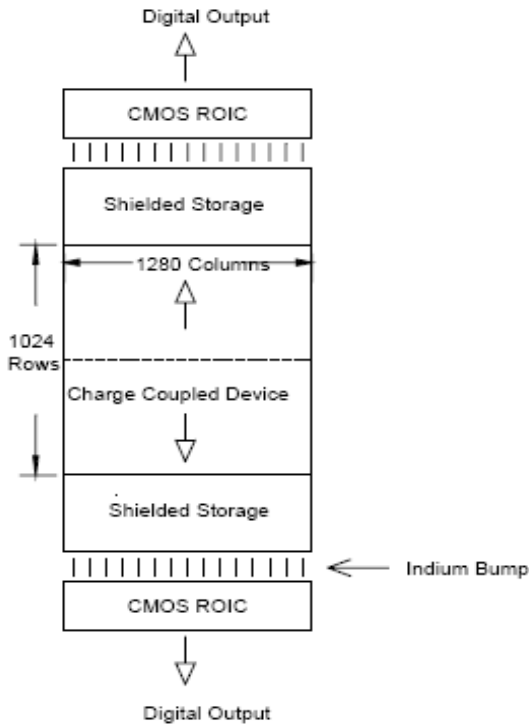
Pixels are readout serially with fast amplifiers (one per electrodes array)
Charge shifts horizontally into vertical registers which are readout serially.



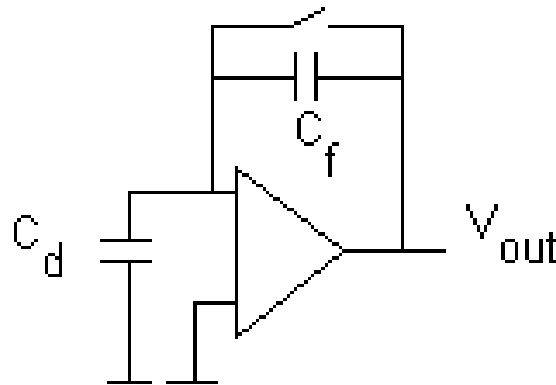
- Transfer from cell to cell is noiseless, 99.999%... efficiency
- Charge is transferred from the last pixel to a voltage follower (floating gate) after resetting the node. The node is sensed before and after transfer

Correlated Double Sampling (CDS, eliminates reset noise)

CCDs readout



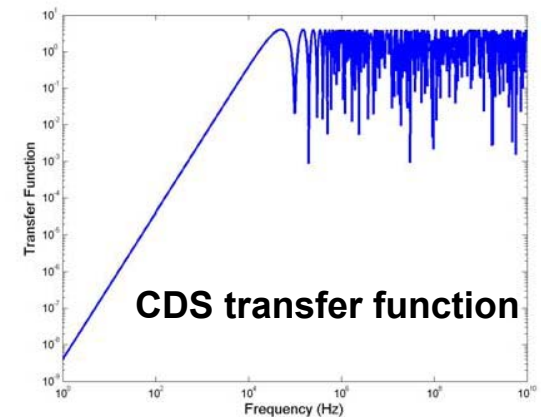
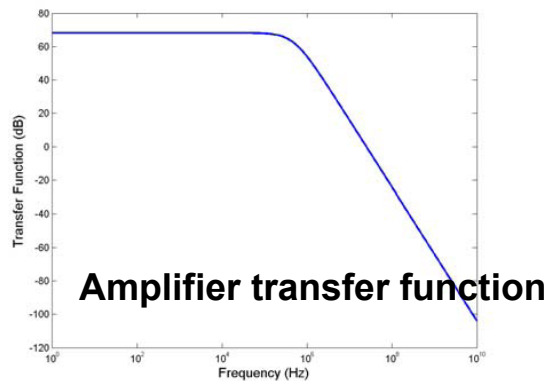
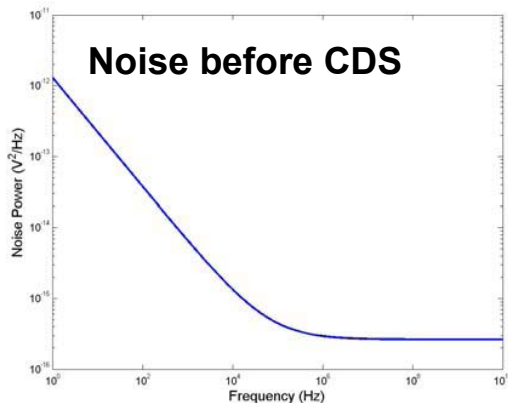
Off-chip amplification, noiseless transfer
CCD to readout chip



Fairchild

On readout chip capacitive transimpedance amplifier after on-CCD CDS

[http://www.fairchildimaging.com/main/documents/CCD CMOS Hybrid FPA for Low Light Level Imaging.pdf](http://www.fairchildimaging.com/main/documents/CCD_CMOS_Hybrid_FPA_for_Low_Light_Level_Imaging.pdf)



CCD readout

- Most CCD noise is system noise after CDS
- Cooled at -100°C (173K), dark current is negligible
- Charge transfer efficiency almost perfect (i.e. 1 ppm charge diffusion)
- Companion (bi)CMOS ASIC needed for amplification, ADC, clock generation

CCD readout ASICs:

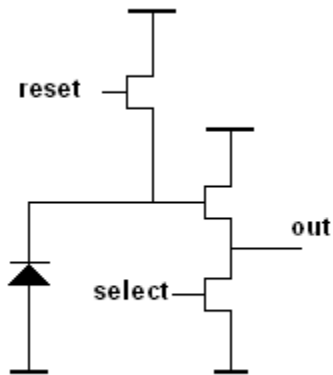
- **ASPIC (LPNHE Paris) for the Large Synoptic Survey Telescope (LSST) focal plane at 173K. 350 CMOS.**
 - > 16-bit dynamic range, noise < $7\text{ }\mu\text{V rms}$
 - Correlated Double Sampling
- **CRIC (LBNL) for SuperNovae Acceleration Probe / Joint Dark Energy Mission (SNAP/JDEM). Space boarded telescope at 140K, 10 kRad tolerance. 250nm CMOS.**
 - Correlated Double Sampling
 - > On-chip pipe-line ADC (13-bit),
 - noise < $6.8\text{ }\mu\text{V rms}$
- **Sidecar (Teledyne)**
 - Up to 16 Mpixel support
 - 36 analog channels, Correlated Double Sampling
 - 16-bit ADC 100 kHz
 - 12-bit AC 10 MHz
 - CCD clock signals generation: kHz-MHz, 10-20V clocks

<http://www.teledyne-si.com/imaging/sidecar.html>

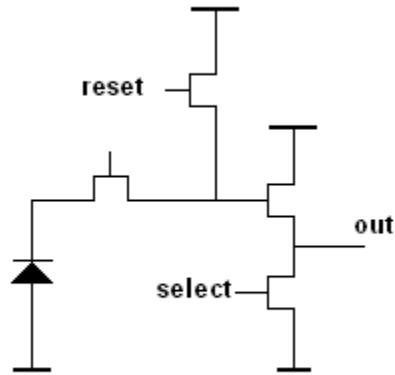
Monolithic Active Pixel Sensors (MAPS)

Pixels instrumented with amplifier and switches

Sensitive volume is a silicon epitaxial layer surrounded by a reverse biased collecting PN junction



3-transistor structure



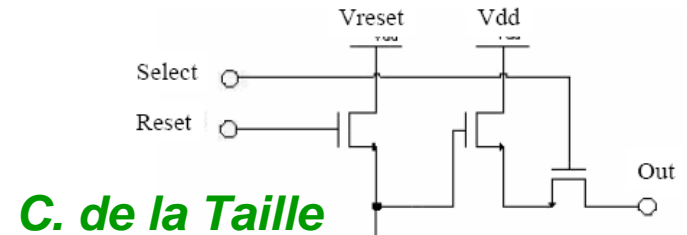
4-transistor structure

4-T isolates pixel and multiplexer structures allowing using CDS

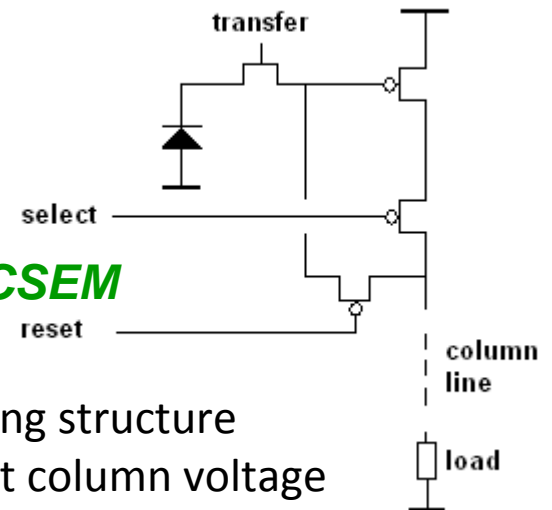
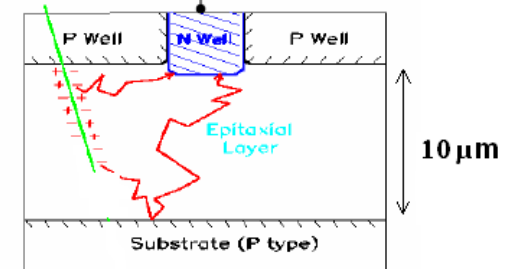
IEEE Trans Nucl Sci Vol 57 n5 Oct 2010, p2490-2496

M. Tyndel, R. Turchetta et al.

Jean-Francois Genat, New Developments in Photo-detection, July 4-8th 2011 Lyon, France



C. de la Taille

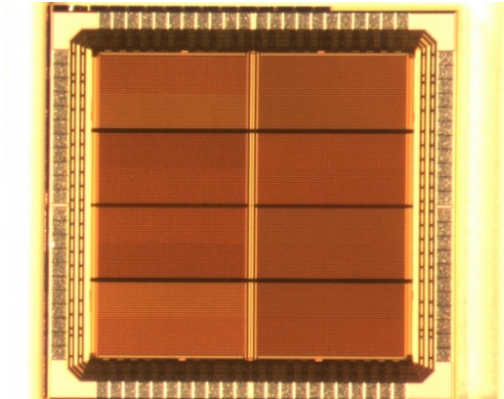


Amplifying structure
Resets at column voltage

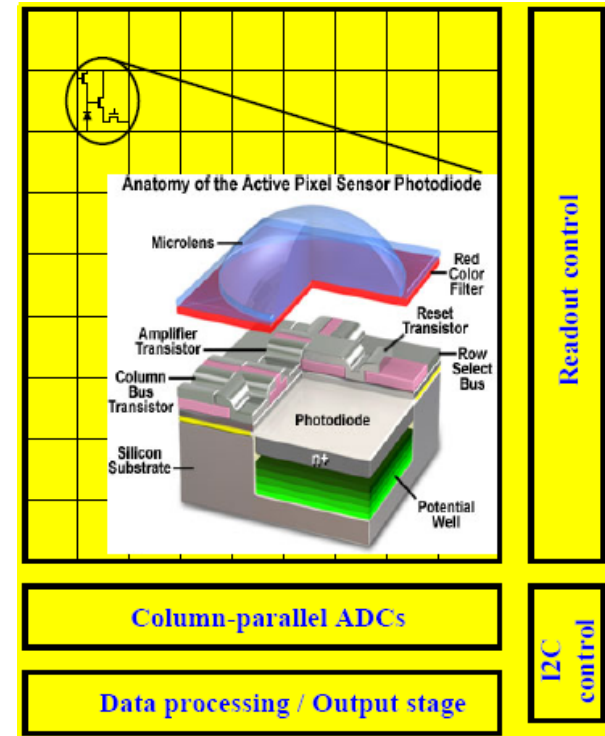
Monolithic Active Pixel Sensors (MAPS)

Pixel ADC: limited area

Time over threshold see FEI4
One comparator / pixel needed



C Hu, IPHC Strasbourg



R. Turchetta, RAL

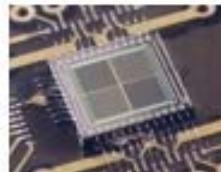
IEEE Trans Nucl Sci Vol 57 n5 Oct 2010, p2490-2496

M. Tyndel, R. Turchetta et al

Monolithic Active Pixel Sensors (MAPS)



many chips



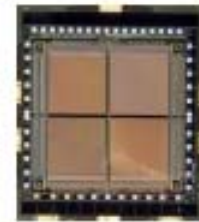
mimosa 01



mimosa 02



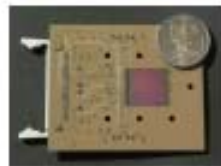
mimosa 03



mimosa 04



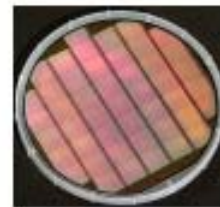
mimosa 05



mimosa 05 +
PCB



mimosa 05
wafer



mimosa 05
wafer



mimosa 05 wafer
(detail)



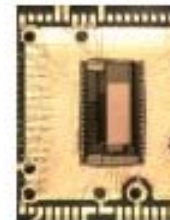
mimosa 06
layout



mimosa 07



mimosa 07
layout



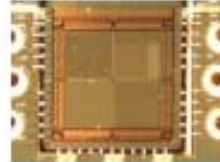
mimosa 08



mimosa 08 +
PCB



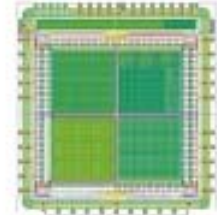
mimosa 08



mimosa 09

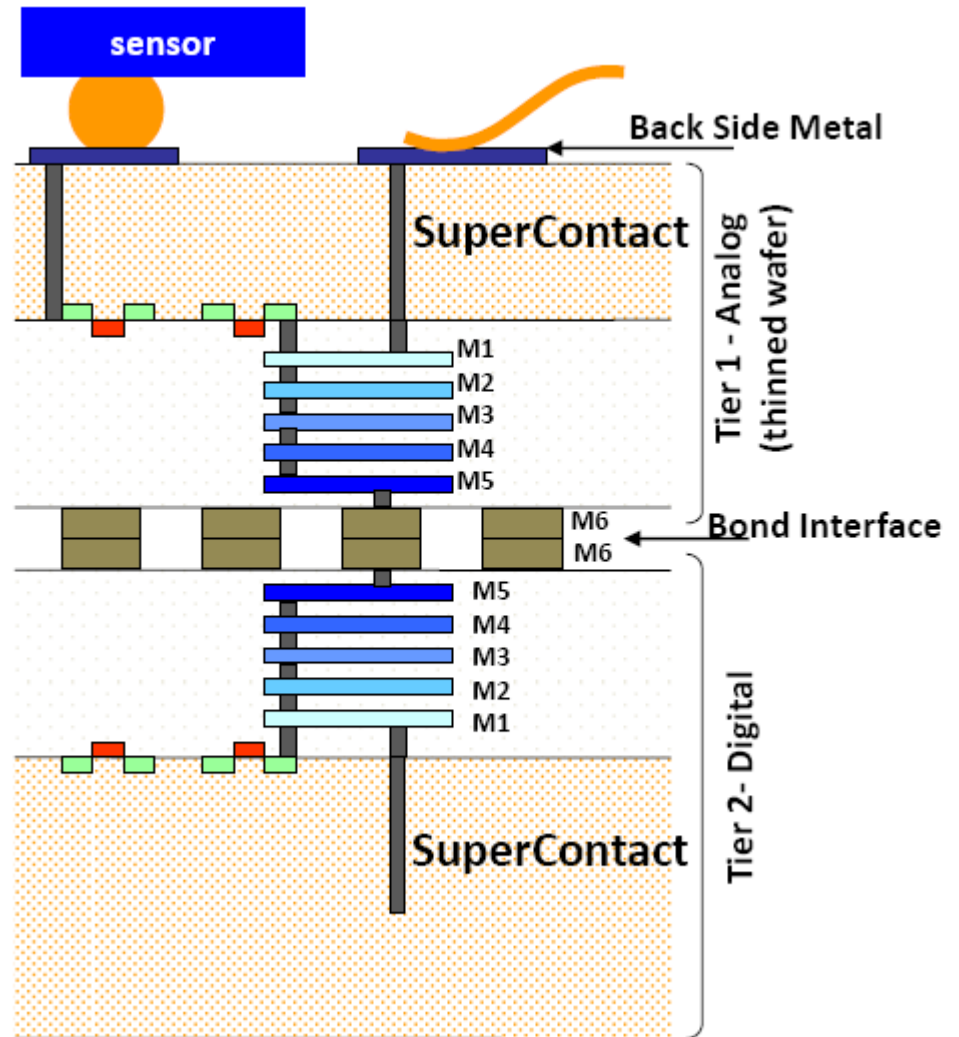


mimosa 09



Mimosa line
IPHC
Strasbourg

Hybrid Pixel Sensors (see 3D section)



Detector of **any material and type**
bump-bonded to readout electronics

2-tier (analog + digital)

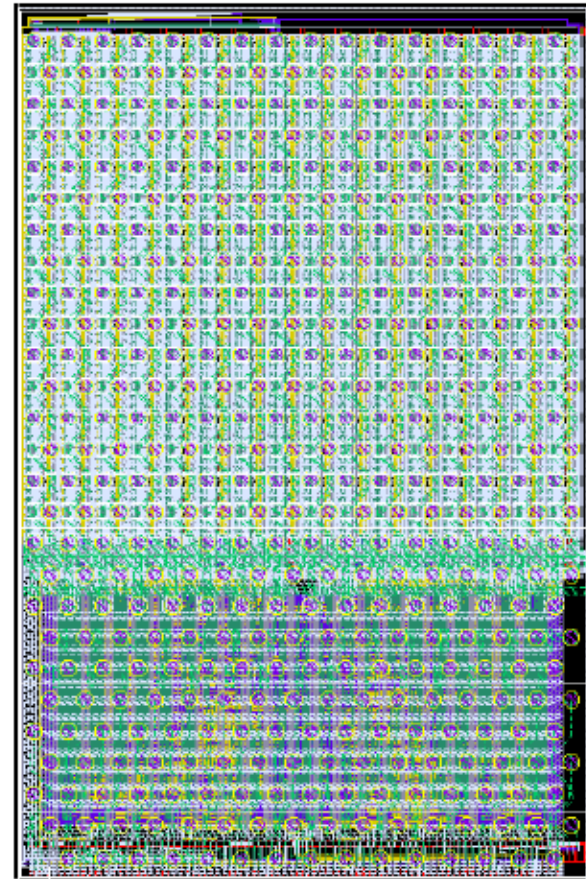
Silicon Vias (TSV)

DEPFET readout CMOS 180nm

DEPFET: modulate the drain current of a MOSFET with ionisation created on the gate (MPI, Germany)

DCDB Production Details

- Implemented in UMC 180nm CMOS technology
- Area: 3240x4969 μm^2
- ~ 2x3 Mini@sic Blocks on a EuroPractice MPW run
- Additional 7th metal layer (redistribution layer) with bump-bond pads including bumps
- Production + bumping costs: ~ 20800 EUR (for 60 pcs.)
- Production time: 5 months total
 - 3 months: MPW run
 - 2 months: 7th metal layer + bumping



J. Knopf

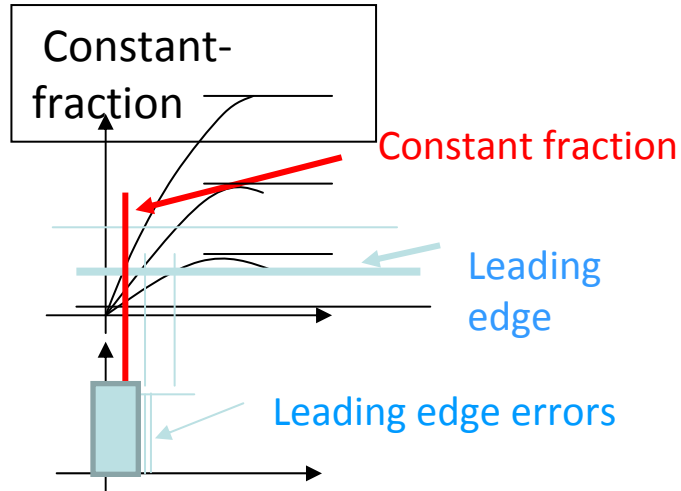


- **Introduction**
- **Contexts**
 - **High Energy Physics**
 - **Space, Medical**
- **Photodetectors**
 - **Vacuum**
 - **Solid state**
- **Photodetectors Electronics**
 - **Components**
 - **Technologies,**
 - **Photon counting**
 - **Amplitude, charge**
 - **Imaging**
 - **Timing**
 - **3D integration**
- **Conclusion**

Timing techniques

$$\sigma_t = \frac{\sqrt{t_r t_s}}{SN}$$

Threshold based + TDCs

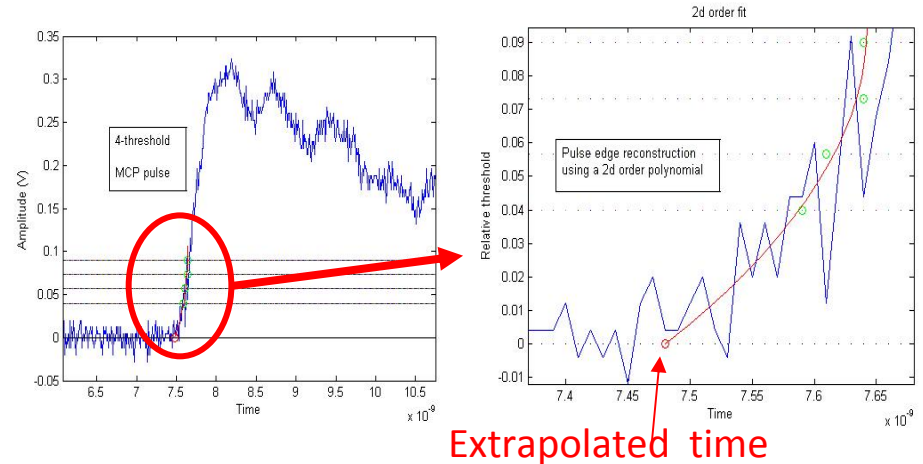


Constant Fraction: Amplitude independent

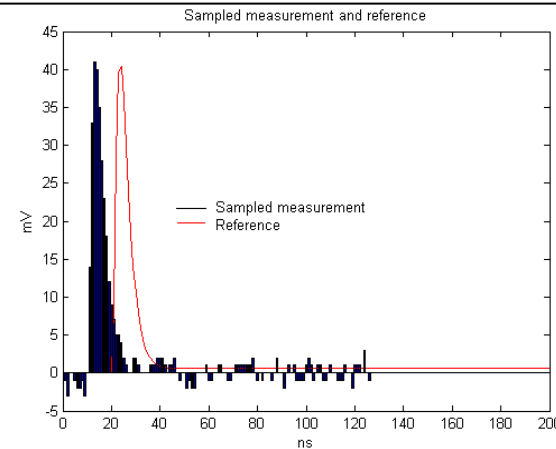
Waveform sampling + Digital Signal Processing

Sample, digitize,
Fit to the known waveform

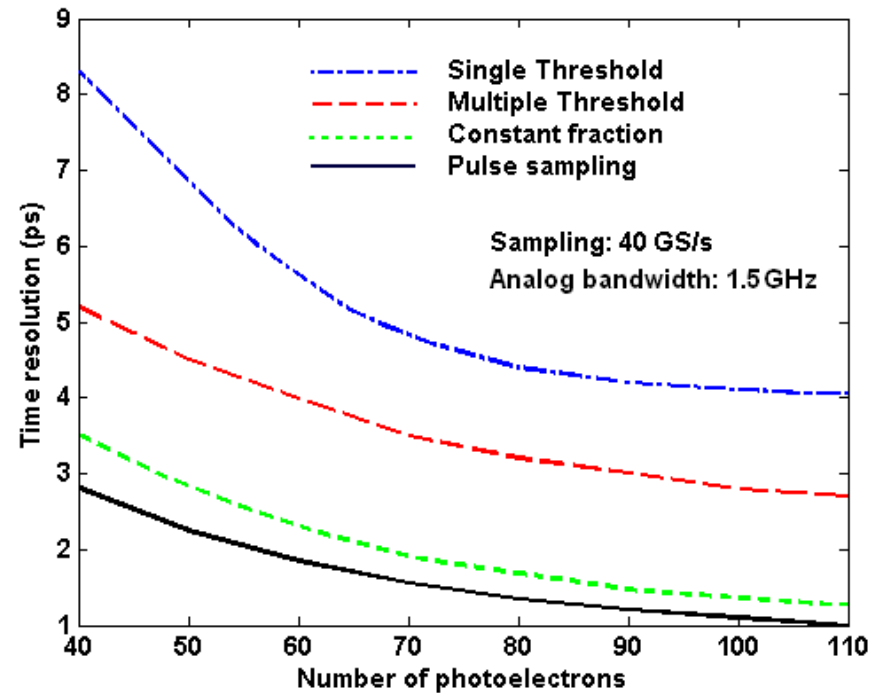
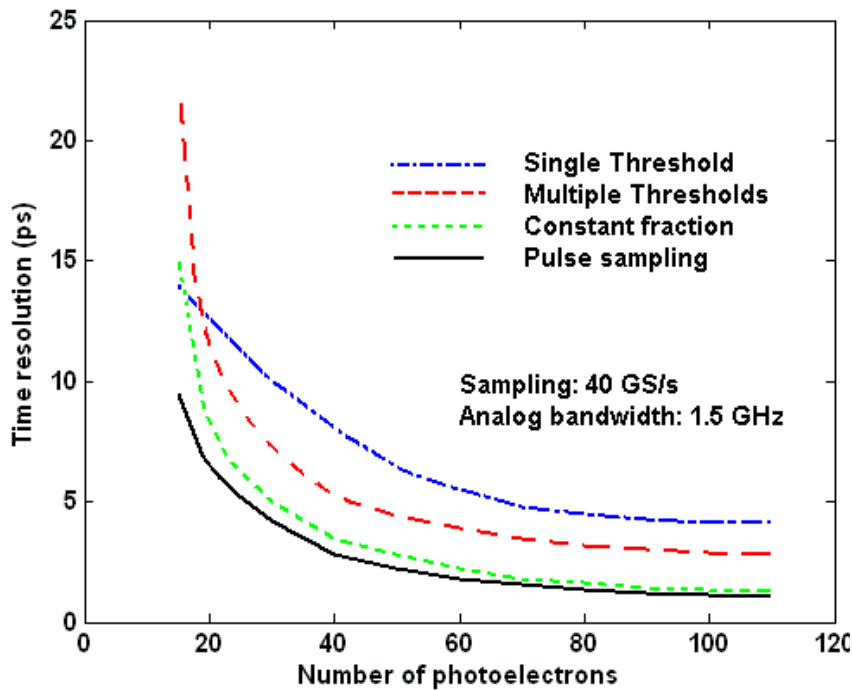
Multi-threshold



Pulse sampling and Waveform analysis



Methods compared (simulation)



zoom

Time resolution vs Number of photo-electrons

Time to Digital Conversion

Many custom ASICs based on analog or digital techniques

Analog

- Ramp between T_{start} and T_{stop}
- Digitize level with an ADC, or ramp down slow and count

10ps resolution possible

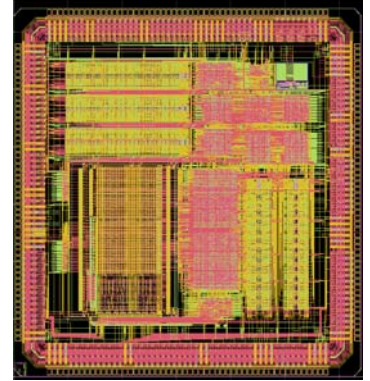
Digital

- Count clock for coarse time (<100MHz)
- Interpolate with vernier digital delay lines locked on clock

10ps resolution possible

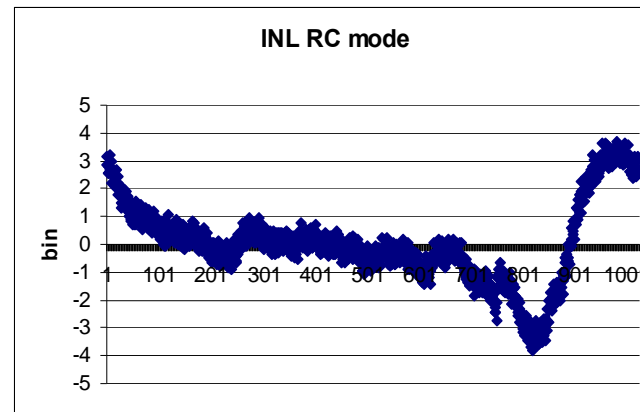
Hybrids !

HPTDC (CERN)

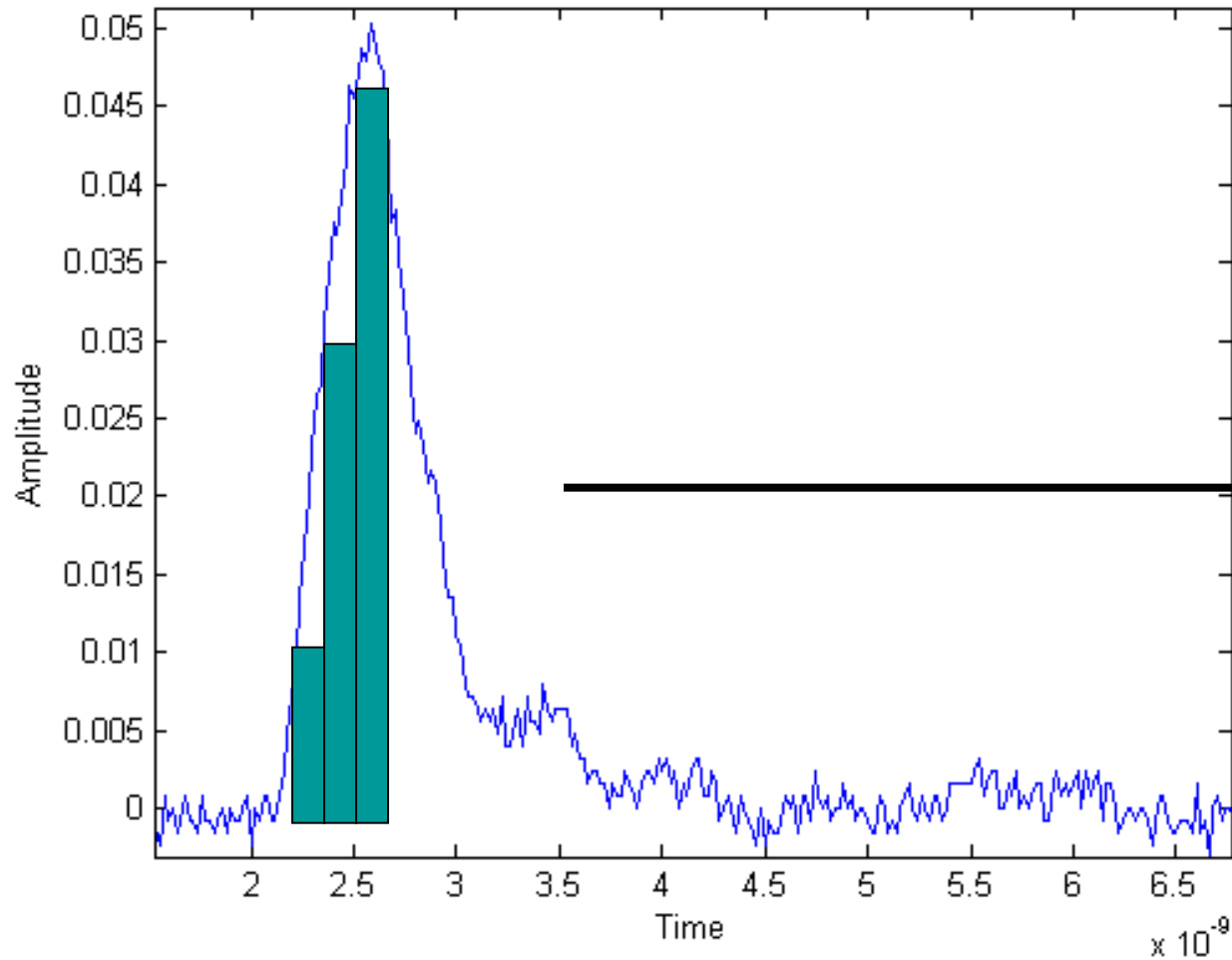


- 32 channels(100ps binning) or 8 channels (25ps binning)
- LVDS (differential) or LVTTL (single ended) inputs
- 40MHz time reference (LHC clock)
- Leading, trailing edge and time over threshold (for leading edge time corrections)
- Non triggered
- Triggered with programmable latency, window and overlapping triggers
- Buffering: 4 per channel, 256 per group of 8 channels, 256 readout fifo
- Token based readout with parallel, byte-wise or serial interface
- JTAG control, monitoring and test interface
- SEU error detection.
- Power consumption: 0.5W – 1.5W depending on operating mode.

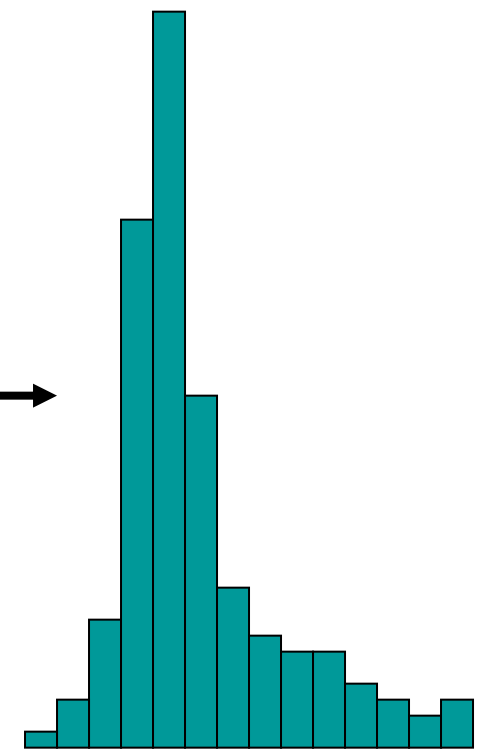
J. Christiansen CERN



Pulse Sampling



Sampling period, digitization (number of bits)



2 12 25 80 128 50 32 ...

Waveform analysis⁹⁶

Pulse Sampling

ADC: Number of bits

Quantization noise is $\text{LSB}/\sqrt{12}$

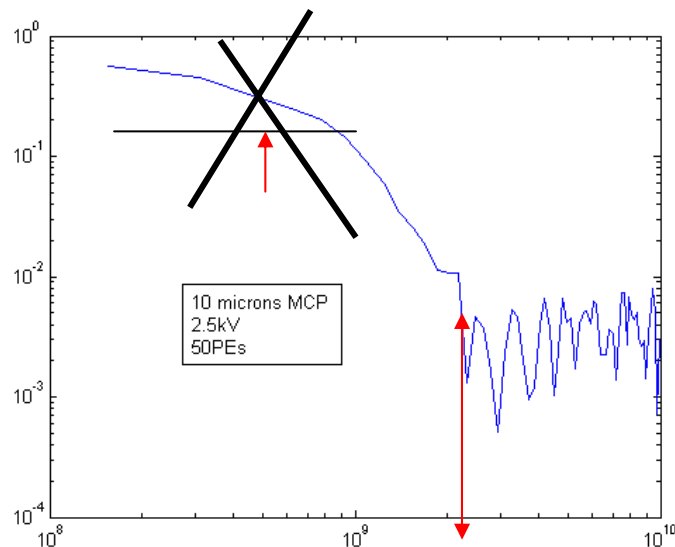
Signal noise should be significantly more than Q noise

X_{\max} Largest signal of interest :

$$\text{Nbit} = \log_2 (X_{\max} / \text{LSB})$$

Sample rate $1/\tau$

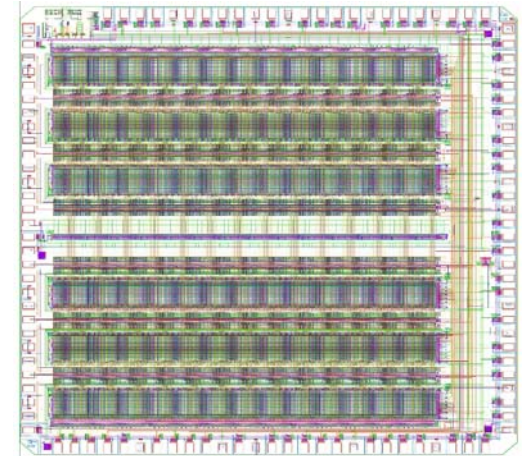
**$1/\tau$ above twice the Shannon-Nyquist frequency: the highest frequency above noise
NOT the 3dB cut-off:**



Example: PSEC3 6-channel Sampling ASIC specifications

10 GS/s sampling ASIC for Micro-Channel Plates Readout

Maximum sampling rate	15GS/s
Analog Bandwidth	2 GHz
Dynamic range	0.8V
Number of channels	6
Number of cells	256
Sampling window	adjustable 500ps-2ns
ADC Resolution	8-bit (12-bit implemented)
Crosstalk	1%
DC Input impedance	50 Ω internal (channels 0 and 1) 50 Ω internal (channels 2 and 3)
Clock	40 MHz
Conversion clock	1-2 GHz internal ring oscillator
Readout time	4 x 256 x 25ns=25.6 ms
Power	40mW/channel @ 1.2V
Process	IBM 8RF-DM (130nm CMOS)



Input analog bus laid out as a 50 Ω transmission line

RF design above 1 GHz

Devices behaviour are more and more geometry dependent

- **Controlled impedance 50 Ω paths**
- **Devices characterized by linear S (scatter) parameters**
- **Electromagnetic waves softwares**

Tools for Silicon, GaAs, RF transmission lines,

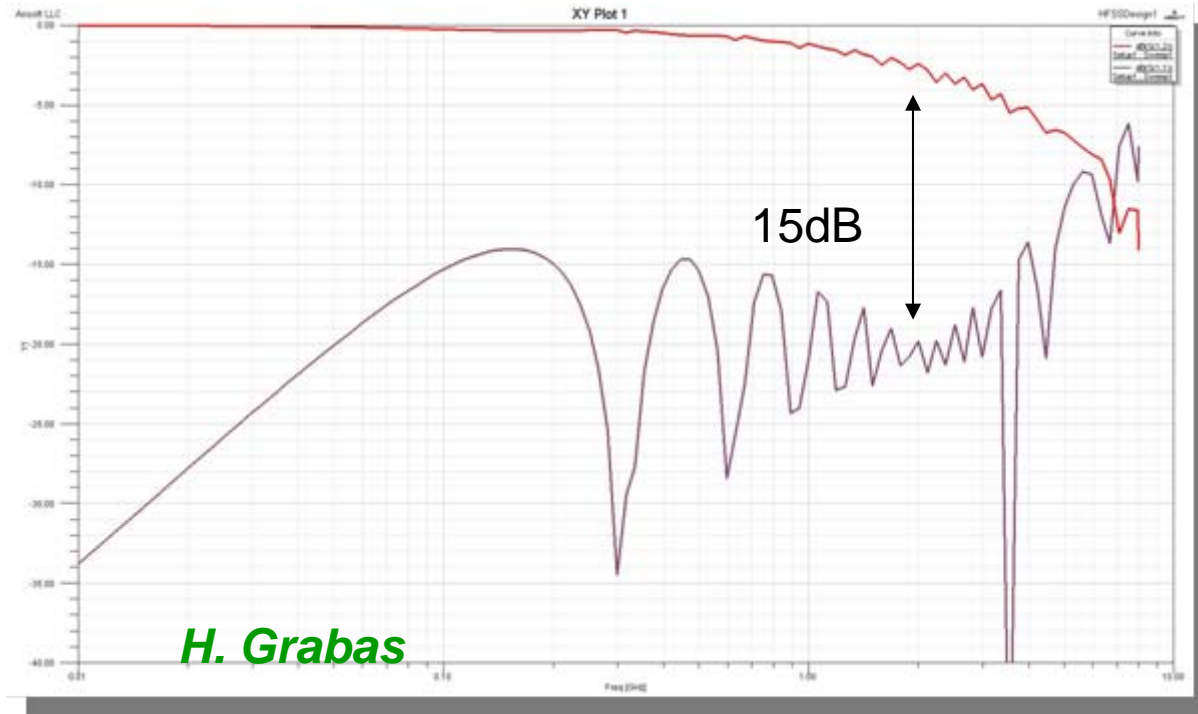
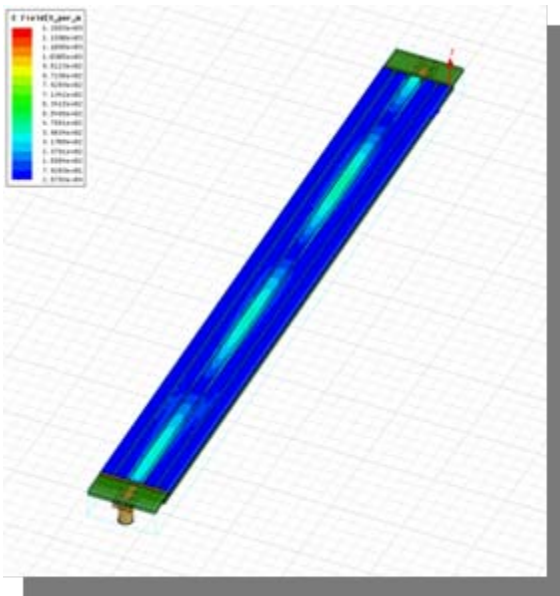
- **Network analysers**
- **Time Domain Reflectometry**
- **50 Ω Calibrated components**
- **RF software layout and simulation tools**

Agilent ADS

Ansoft HFSS

RF design

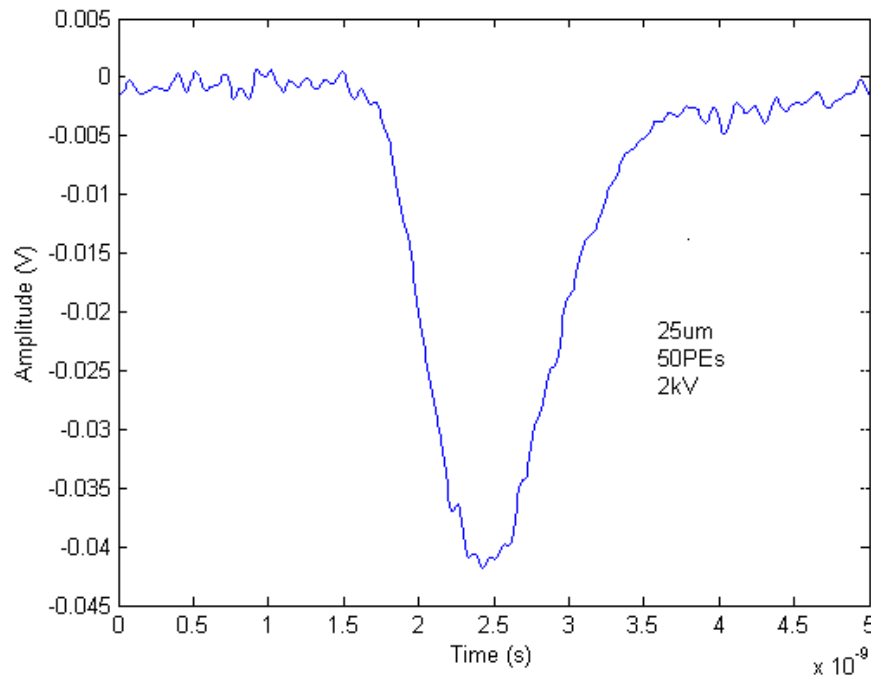
DC-10 GHz simulations of a large area (20 x 20 cm) Micro-Channel Plate based detector using Ansoft HFSS electromagnetic simulator



**Transmission line implemented
on glass for 2D Micro-Channel plate readout**

**Simulation shows that device is
functional up to 2.3 GHz at
15dB**

Processing of digital sampled data

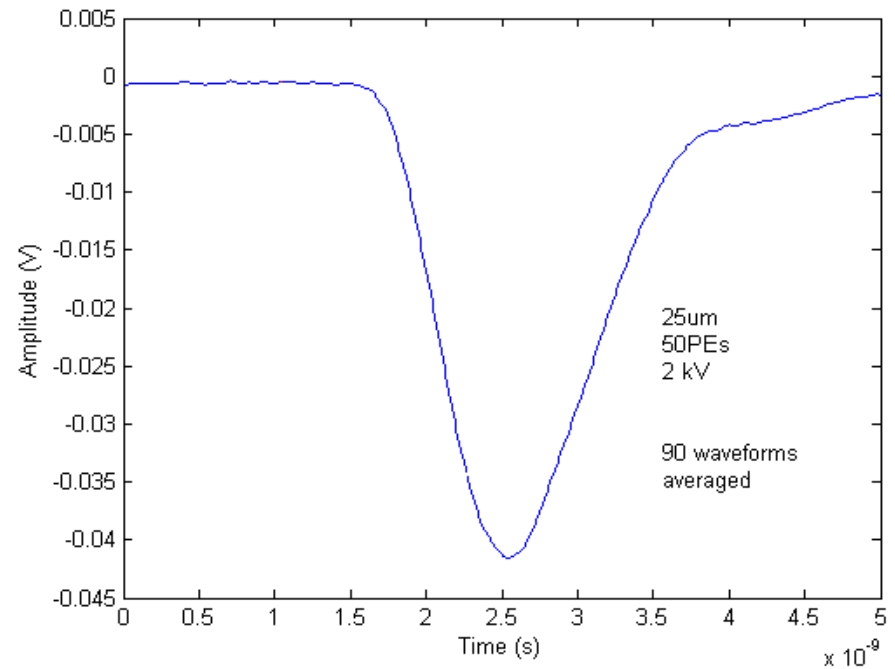
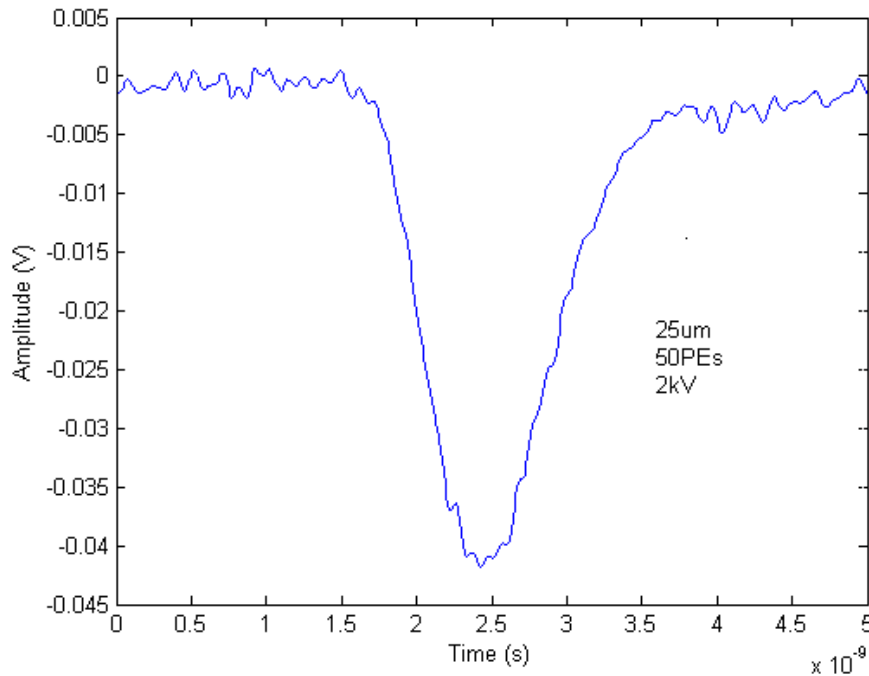


**Determine which information is useful in the waveform:
Rising edge, integral, maximum amplitude.**

For photo-detectors, usually **time and charge (integral of the current pulse)**

Pulse shaping can be done in digital if power and speed allow (ADC)

Fast timing: Processing of sampled data



Original MCP measured signal

Signal template (obtained by averaging 100 signals to remove noise)

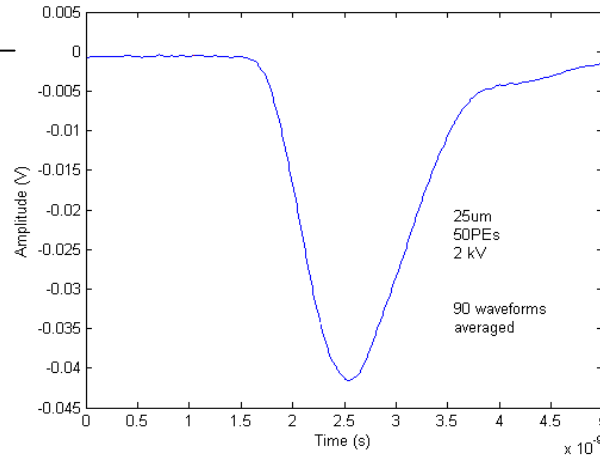
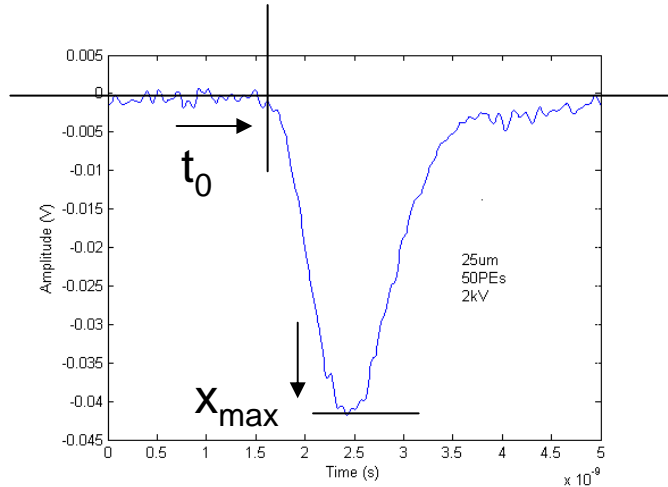
Example: Least squares algorithm:

Minimize
$$\chi^2 = \sum_{i=1}^N (\mathbf{x}_{\text{meas}_i} - \mathbf{x}_{\text{temp}_i})^2$$

to get accurate time and maximum amplitude

Processing of digital sampled data

Example: find pulse time and maximum amplitude



Solve:
$$\chi^2 = \sum_{i=1}^N (x_{\text{meas}_i} - x_{\text{temp}_i})^2, \quad \partial \chi^2 / \partial t_0 = 0, \quad \partial \chi^2 / \partial x_{\text{max}} = 0$$

Obtain t_0 and x_{max} :

$$a = \sum_i x_{\text{temp}_i}^2 \quad bp = \sum_i x'_{\text{temp}_i}^2 \quad b = \sum_i x_{\text{temp}_i}^2 \cdot x'_{\text{temp}_i}^2 \quad d = b^2 - a \cdot bp$$

$$mp = \sum_i x_{\text{meas}_i}^2 \cdot x_{\text{temp}_i}^2 \quad mp' = \sum_i x_{\text{meas}_i}^2 \cdot x'_{\text{temp}_i}^2$$

$$t_0 = 1 / d (mp' \cdot b - mp \cdot bp) \quad x_{\text{max}} = -1 / t_0 (mp' \cdot a / d + mp \cdot b / d)$$

Digital filtering

Signal as a sequence of numbers, compute weighted sums with a Digital Signal Processor.

- Finite Impulse Response: convolution with the sampled impulse response
- Infinite Impulse Response: recursive, use of the z-domain frequency response:

Analog

$$P(j\omega) / Q(j\omega) = \frac{\sum_n a_n j\omega^n}{\sum_m b_m j\omega^m} \quad j\omega \rightarrow \frac{2}{\tau} \frac{1 - z^{-1}}{1 + z^{-1}}$$

Digital

$$y_k = y(k\tau), \quad x_k = x(k\tau)$$

$$P(z) / Q(z) = \frac{\sum_i a_i z^{-i}}{\sum_j b_j z^{-j}} \quad y_k = \sum_j a_j y_{k-j} - \sum_j b_j x_{k-j}$$

Example: 1st order RC filter

Analog

$$H(j\omega) = \frac{1}{1 + RCj\omega}$$


$$y(t) = C \exp(-t / RC)$$

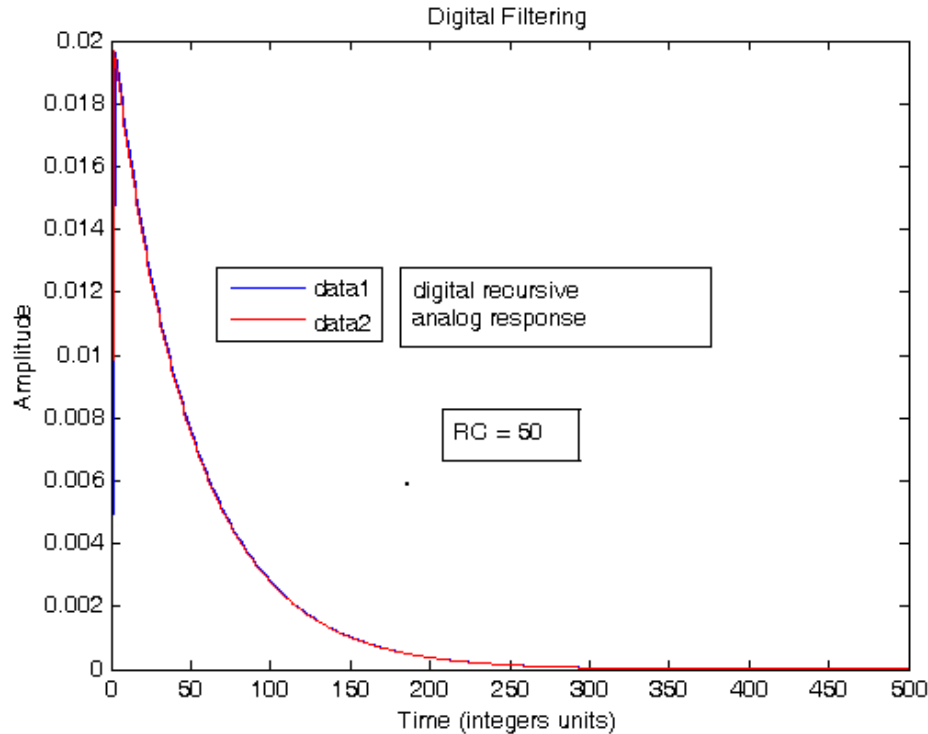
Digital recursive

$$P(z) / Q(z) = \frac{1 + z^{-1}}{(1 + a) + (1 - a)z^{-1}} \quad Y(k) = -\frac{1}{1 + a} [(1 - a) Y(k - 1) + X(k) + X(k - 1)]$$

$$a = RC / \tau$$

Digital filtering

Example: 1st order RC filter



Analog

$$H(j\omega) = \frac{1}{1 + RCj\omega}$$

$$y(t) = C \exp(-t / RC)$$

Digital recursive

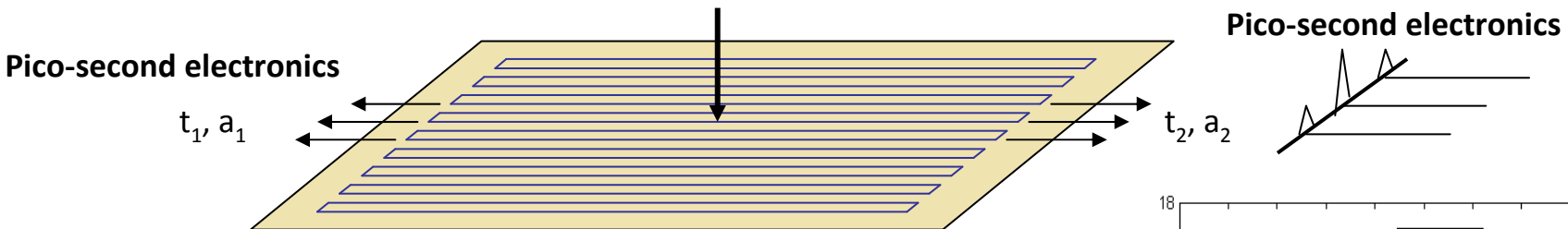
$$H(z) = \frac{1 + z^{-1}}{(1 + a) + (1 - a)z^{-1}}$$

$$y(k) = -\frac{1}{1 + a} [(1 - a) y(k - 1) + x(k) + x(k - 1)]$$

Pico-second timing and 2D position for large area detectors with delay lines

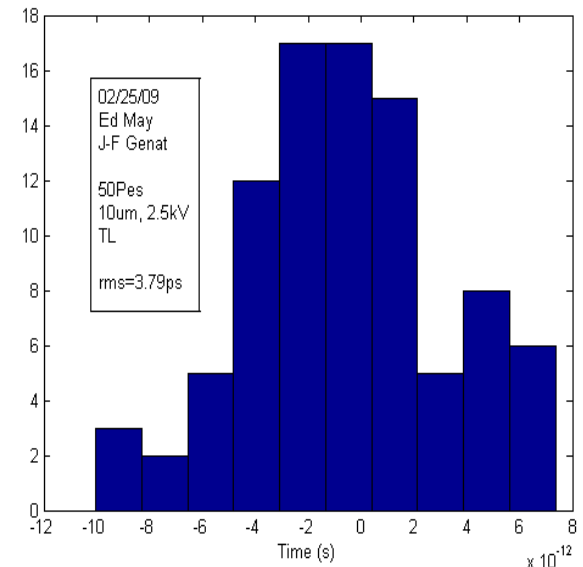
- Delay lines readout and pulse sampling provide
 - Fast timing (2-10ps)
 - One dimension with delay lines readout 100mm- 1mm
Transverse dimension can be obtained from centroids

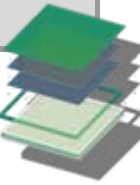
Less electronics channels for large area sensors



Timing extration with sampling and Digital Signal Processing
3.8 ps translates in 190 μm position resolution with 50 photo-electrons
5 x 5 cm² MCP

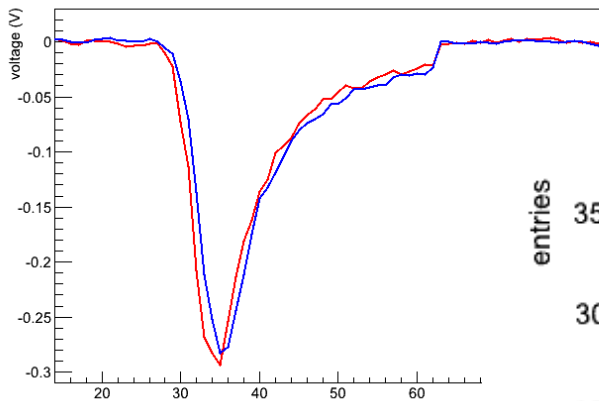
$$\begin{aligned} \frac{1}{2} (t_1 + t_2) &= \text{time} \\ v(t_1 - t_2) &= \text{longitudinal position} \\ \Sigma \alpha_i a_i / \Sigma \alpha_i &= \text{transverse position} \end{aligned}$$





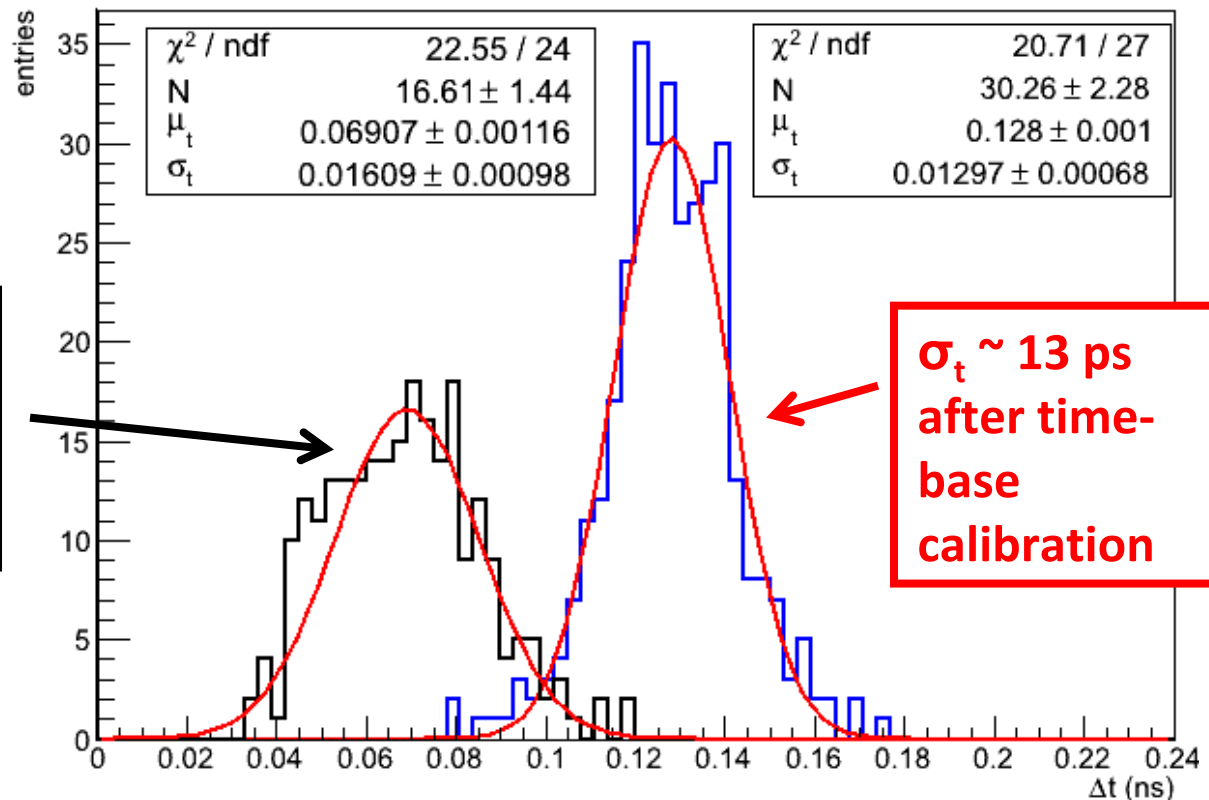
Example: Transmission Line-Micro-Channel Plates readout

Sample waveforms



$\sigma_t \sim 17$ ps
assuming
nominal 100ps
per cell

Stripline: $t_{\text{left}} - t_{\text{right}}$ (preliminary)



$\sigma_t \sim 13$ ps
after time-
base
calibration

E. Oberla

- **Introduction**
- **Contexts**
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- **Photodetectors**
 - **Vacuum**
 - **Solid state**
- **Photodetectors Electronics**
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 - **Technologies,**
 - **Photon counting**
 - **Amplitude, charge**
 - **Imaging**
 - **Timing**
 - **3D integration**
- **Conclusion**

3D Integration

Goal: increase the integration density

Interconnections: Two options: die to die

- 1 **Stack up several layers of different IC processes Interconnections.**
Through Silicon Vias (TSV) if more than 2 layers
Die can be tested



2-tier



2-tier w/TSV



Multi-tier hybrid w/TSV

- 2 **2D in a thinner process**

K. Torki

Limit of CMOS (10nm) is coming soon, option 1 will be mandatory
In addition, thin processes are *always* expensive. But 3D could be as well...

3D tools emerging:

- **Simulation**
- **Layout**
- **Extraction**

http://cmp.imag.fr/Spl-Session_3DIC/02_CMP.pdf

3D Imagers

AREA 3D INTEGRATED IMAGERS

■ Status: system architecture study of an **imaging system on a chip-stack**

- Integration of micro-optics layer:

- Ultra wide field of view
- Filters for hyperspectral imaging

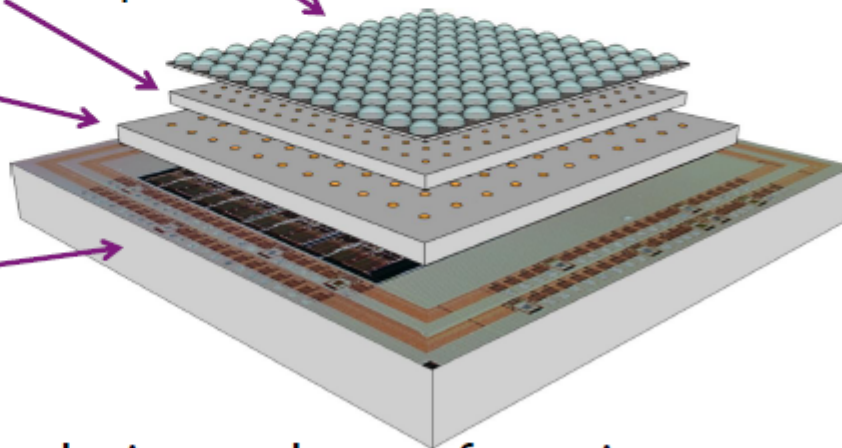
- Shared pixels = multiple pixels per bump

- Smart analog/digital read-out:

- Ultra high dynamic range
- ADC per group of pixels
- Variable resolution (active binning)

- Smart digital processing:

- 2D distributed group of processors
- Face recognition

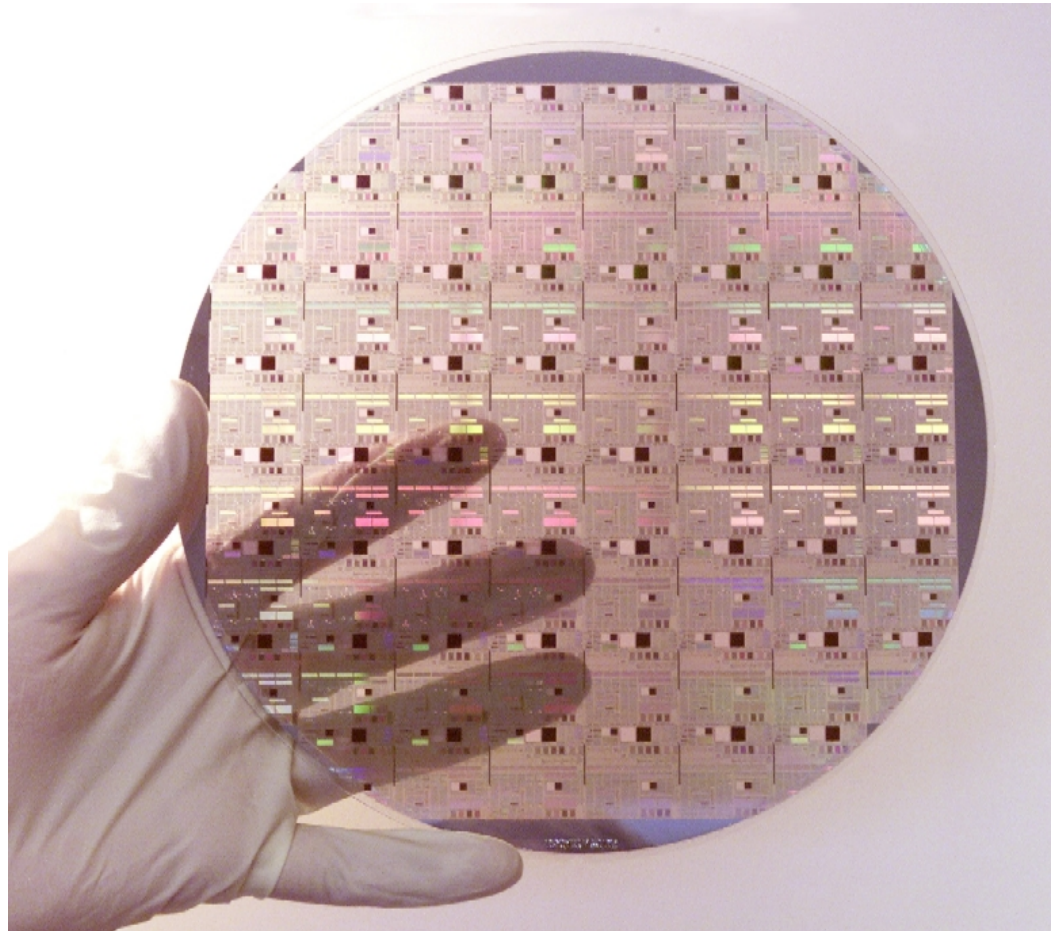


■ Next step: demonstrator design and manufacturing

3D Integration

- Shorter connections
Lower impedance
Less RC delays
Save power
- Higher density
Better heat
Smaller I/O pitch

**Area x Timing x Power =
Factor 15**



J.J Lu

**Wafer bonding for 3D integration
Cu on SiO₂ interconnect structures**

Applications

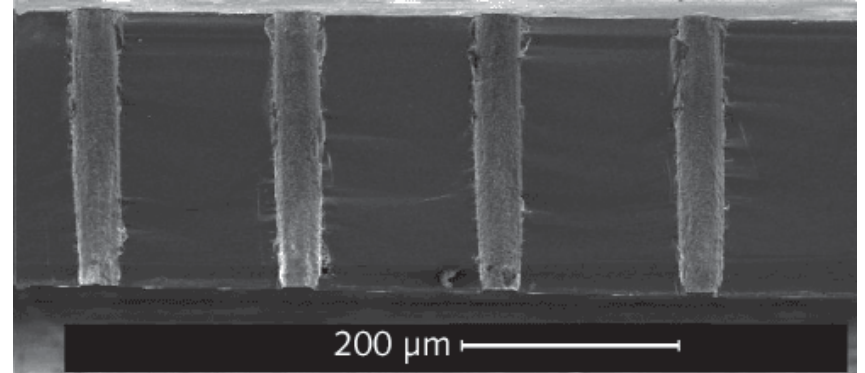
- **Memories, Memory on CPU**

IBM, Samsung

- **Pixellated photo-detectors:**

- Optics microlenses, filters,
- Pixels Photo-Detector,
- Electronics (analog + digital),
- Serial opto out

MIT Lincoln Labs, RTI, Ziptronix



Key feature:

**Through Silicon Via
(TSV)**

2-tier 3D process tools

- **PDK:** from CMC +
TSVs from Tezzaron

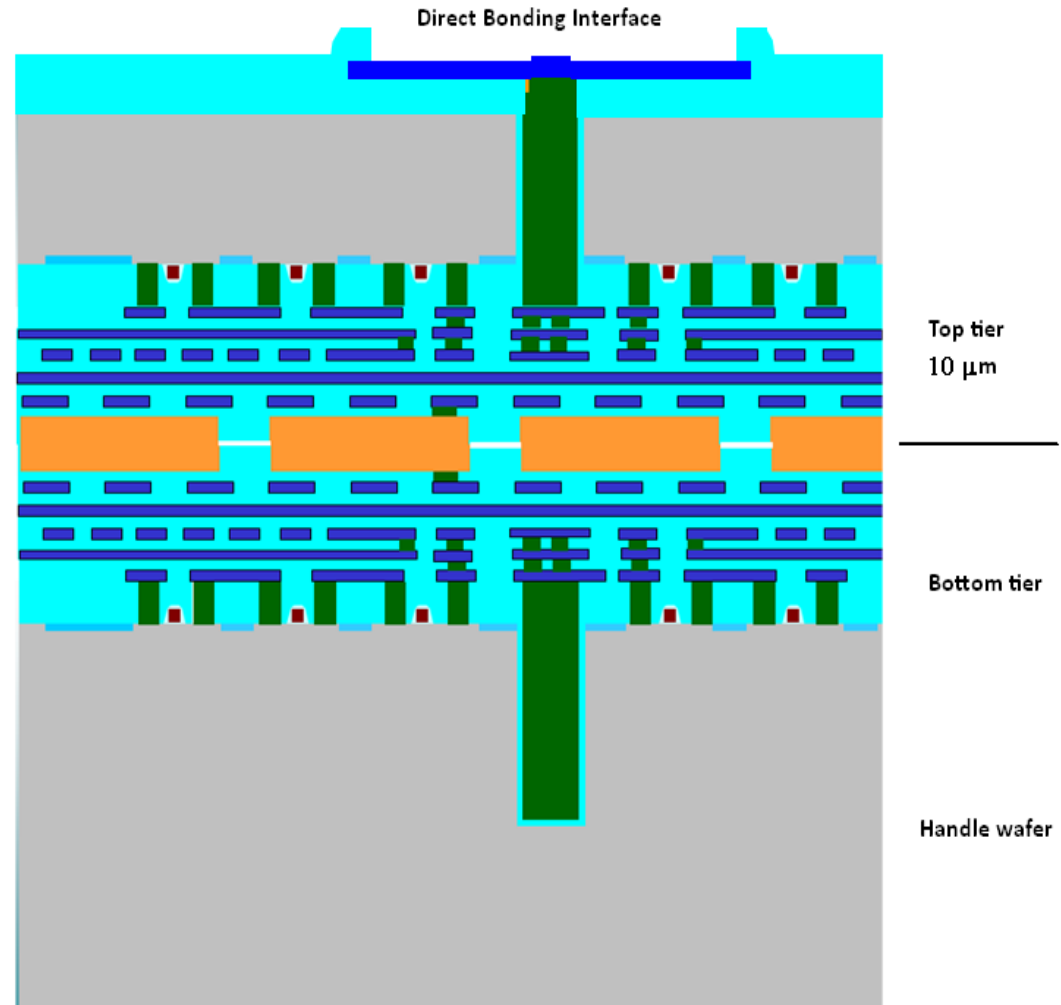
- **Libraries:** Core + I/O from ARM

- **Memory compiler:**
S/DPRAM and ROM from AI

- **3 D Utilities:**
Contributions development

- **Tutorial, User's setup**
Intallation easy

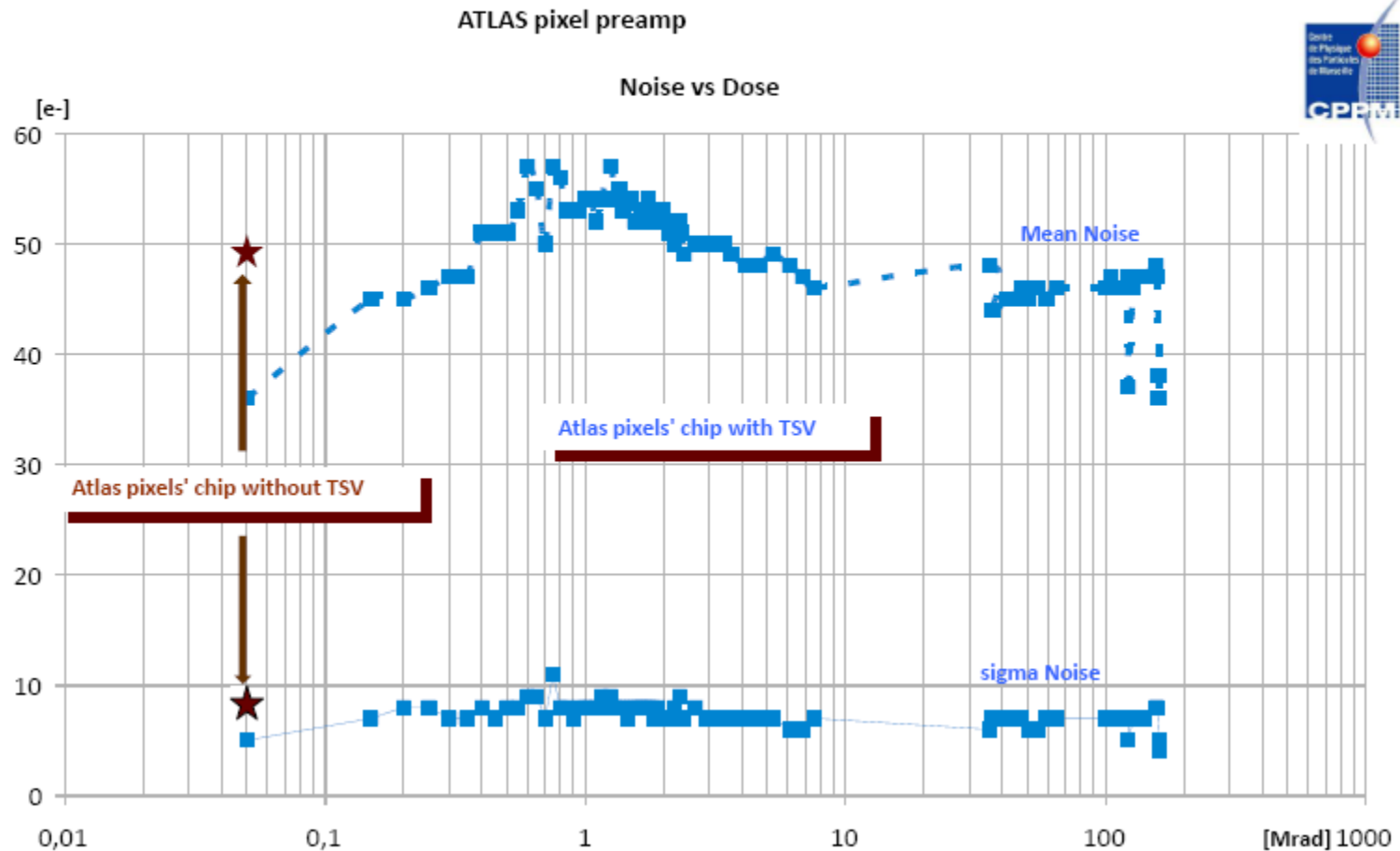
- **Support of Cadence CDB and OpenAccess databases**



K. Torki

3D process radiation hardness

FE-TC4-AE X-ray irradiation



A. Rozanov

CMC

Canada

CMP

France

Mosis FNAL

US

Tezzaron

Singapore

Access to 3D technology:

- **2-tier 130m CMOS**
- **Tezzaron, Globalfoundries**
- **Top tier exposing TSV**
- **Backside metal pads for wire bonding**
- **Design kit available**

Discussions with LETI, AMS

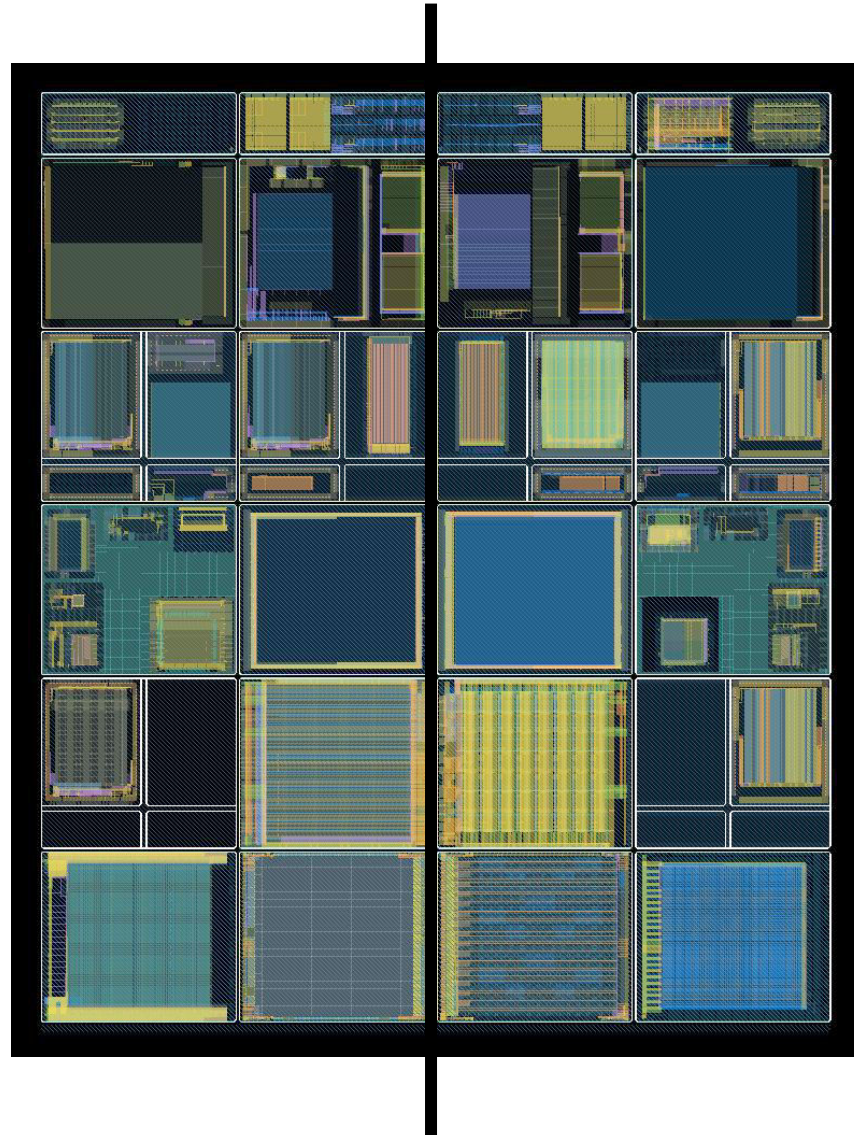
Talk to:

Kholdoun TORKI (CMP Grenoble, France)

<http://cmp.imag.fr/products/ic/?p=130nmFaStack>

1st MPW run

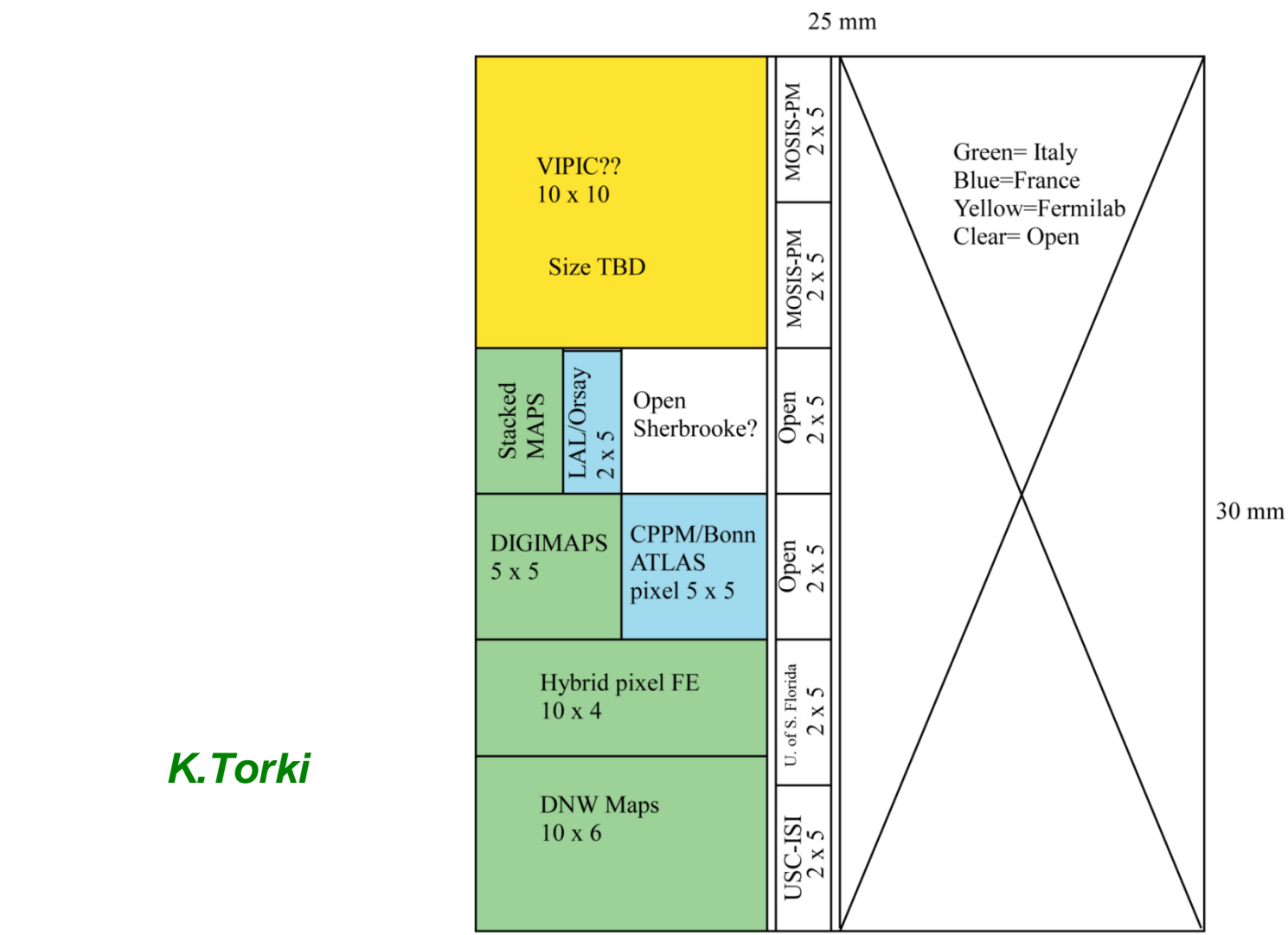
Fermilab



Top tier

Bottom tier

3D Integration CMP/MOSIS/CMC 1st MPW run



K.Torki

MPW run May 31st, 2011

3D Tools: Virtuoso Layout Editor with 3D layers

TSV →

Back Metal →

Back Pad →

DBI →

K. Torki

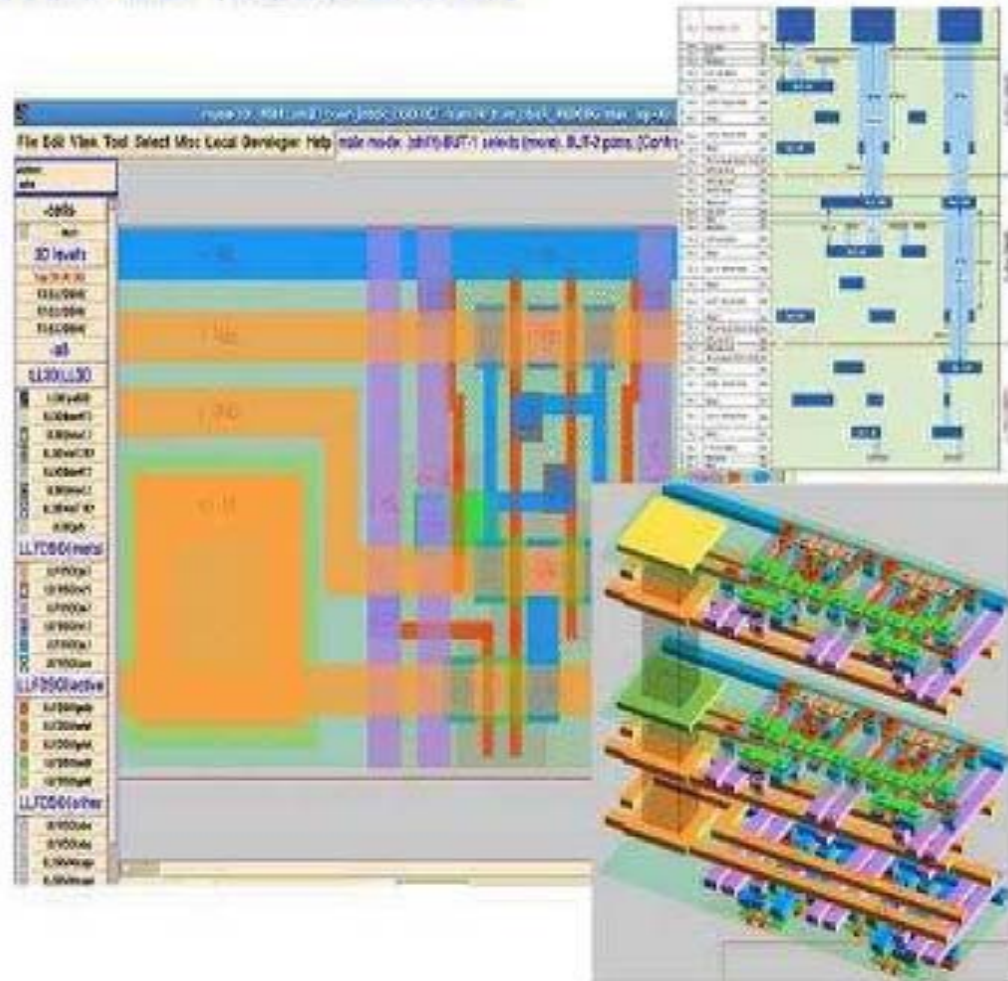
The screenshot shows the Virtuoso Layout Editor interface. The left panel displays a layer stack with the following layers and types:

Layer Name	Type
NO_FILL	drw
TSCSuperCnt	drw
TSCBackMet0	drw
TSCBackMet0	lbl
TSCBackMet1	drw
TSCBackMet1	lbl
TSCBPad	drw
SRAM_TSC	drw
PR_BNDRY	drw
NWELL	drw
DNWELL	drw
LDMOS_XTOR	mar
COMP	drw
POLY2	drw
POLY2	lbl
PPLUS	drw
NPLUS	drw
CNT	drw
MET1	drw
MET1	lbl
VIA1	drw
MET2	drw
MET2	lbl
VIA2	drw
MET3	drw
MET3	lbl
VIA3	drw
MET4	drw
MET4	lbl
VIA4	drw
MET5	drw
MET5	lbl
VIATOP	drw
METTOP	drw

The main window shows a 3D layout design. The top status bar displays coordinates (X: 12.500, Y: -4.115) and other parameters. The menu bar includes Tools, Design, Window, Create, Edit, Verify, Connectivity, Options, Routing, Assura, Calibre, and Help. The layout view shows a complex circuit design with multiple layers. Arrows point from the labels 'Calibre' and 'Assura' to the corresponding menu items. The bottom status bar shows mouse coordinates and actions: mouse L: mouseSingleSelectPt, M: leHiMousePopUp(), R: hiZoomAbsoluteScale(hiGetCurrentWi).

Tools for Tezzaron

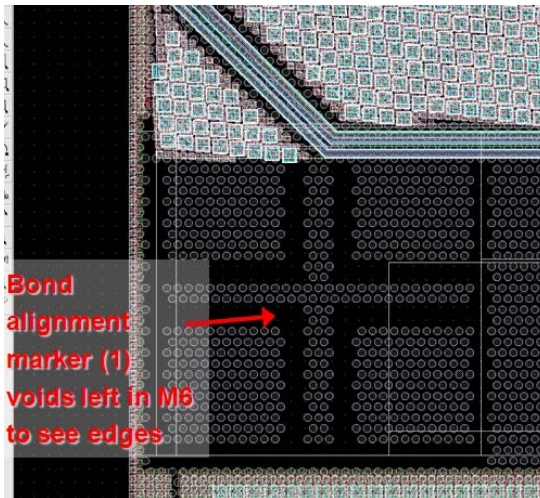
True 3D Mask Editor



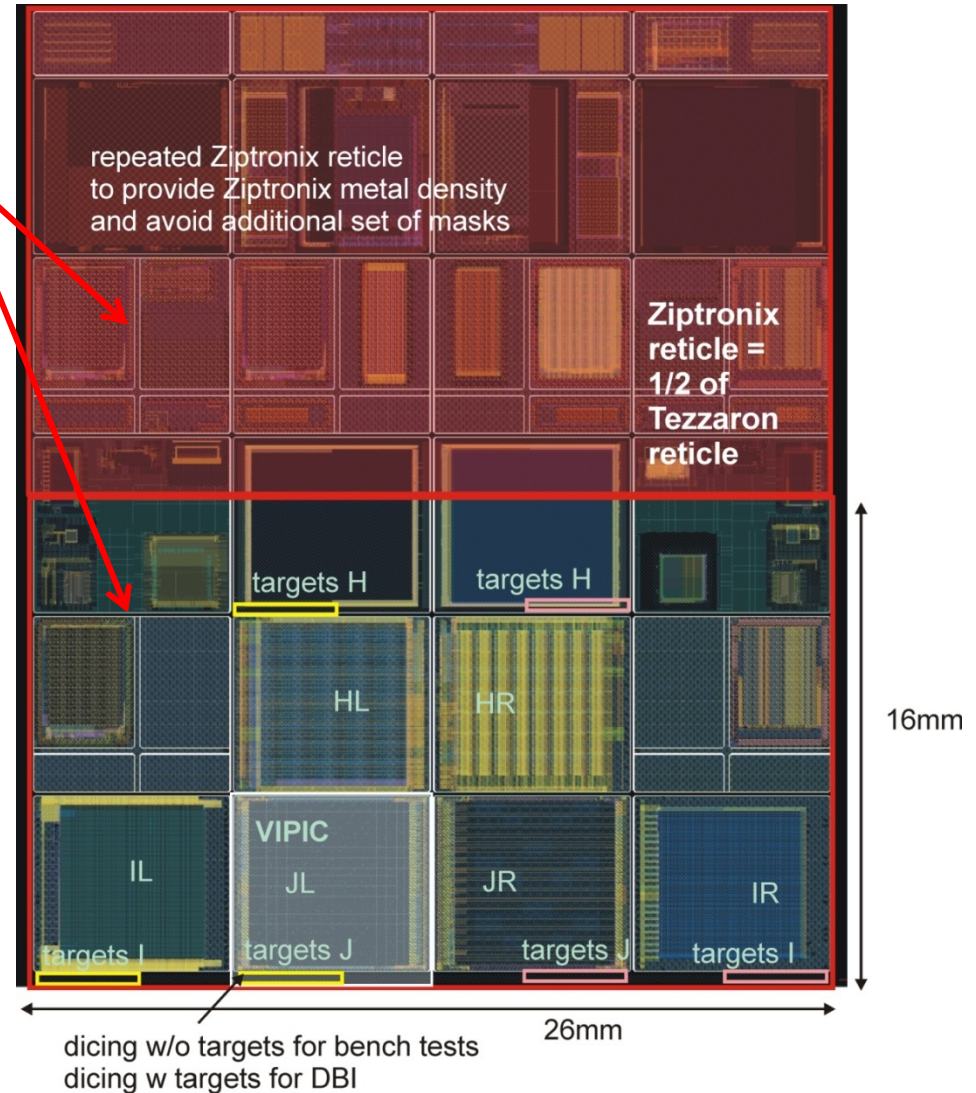
MicroMagix MAX 3D

Example: Some ROIC Wafer Issues

- Frame size for adding Ziptronix DBI bonding pads was smaller than Chartered frame – repeat bond pad mask twice on 3D frame to avoid extra mask cost.
- Space was limited for different alignment targets needed for deposition of seed/DBI post metal and DBI bonding.
- IR transparent bond alignment targets are needed on each ROIC and sensor (conflicts with M6 density requirement)



R. Yarema



Conclusion

Very promising developments open with **3D stacking** allowing to use the most suited technologies for each purpose

- Detection,
- Amplification and filtering,
- Digital processing

V
e
r

Deep Sub-Micron CMOS combined with **Silicon-Germanium** facilitate

- Low noise operation
- High level of integration

to get more and more powerful photo-detectors...

Thanks !

Extra slides

(Some) Photo-detectors

Vacuum

	Principle	Rise time	QE	Gain
• Photo-multipliers	Dynode chain	1-5 ns	25-35%	10^{6-7}
• Hybrid Photo Diodes	Electrons on Si	1-5ns	25-35%	10^{2-4}
• Hybrid APDs	Electrons on APDs			
• Micro-Channel Plates	Micro-pores	100ps	25%	10^6

Solid state

• PIN diodes	Photo-electric	50ps		
• Monolithic Active Pixel Sensors	Photo-electric	N/A		
• Charge Coupled Devices	Photo-electric	N/A	20% front	N/A
			80% back	N/A
• Avalanche Photo Diodes	Linear multiplication	2-5ns	30-70%	10^{1-3}
• Silicon Photo-Multipliers	Geiger avalanche	200ps	90%	10^6
• CdTe/CdZnTe	X-ray			

Large Area Picosecond Photo-Detectors

U-Chicago leaded

- Large (20 x 20 cm²) Micro-Channel Plate (MCP) based
- Glass window and tray
- Photo-cathode
- Double Chevron structure
- Atomic Layer Deposition (ALD) processed

Readout Electronics

- Giga-Hertz Waveform sampling
- Application Specific Integrated Circuits (ASIC) based
- 130nm CMOS technology

Potential applications:

High Energy Physics:

Medical Imaging:

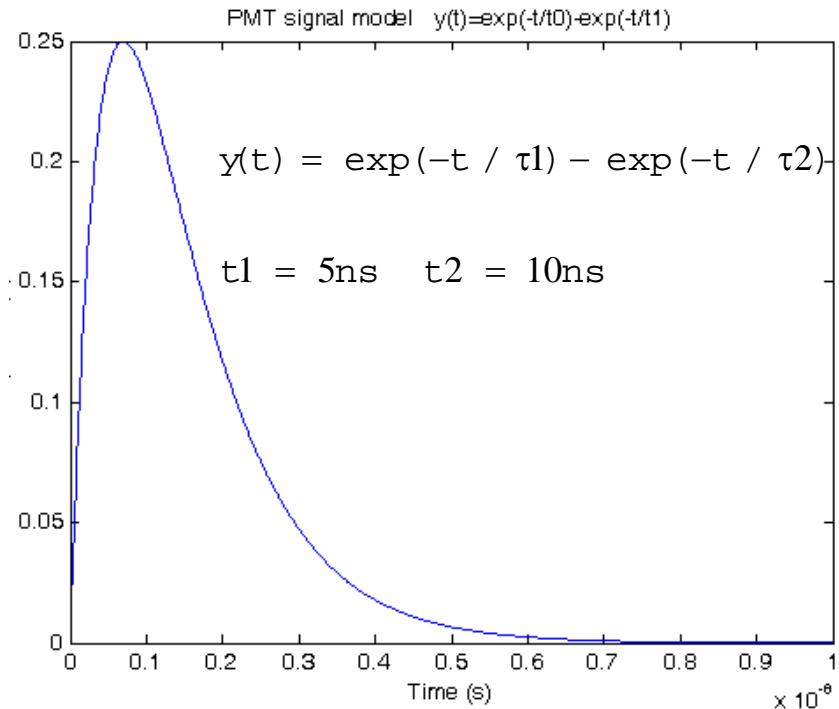
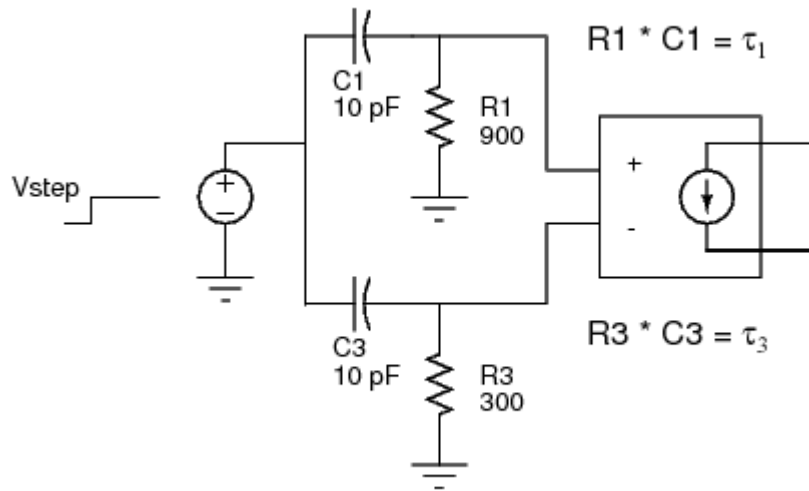
Security:

Detectors, new acceleration techniques

Positron Emission Tomography, dosimetry

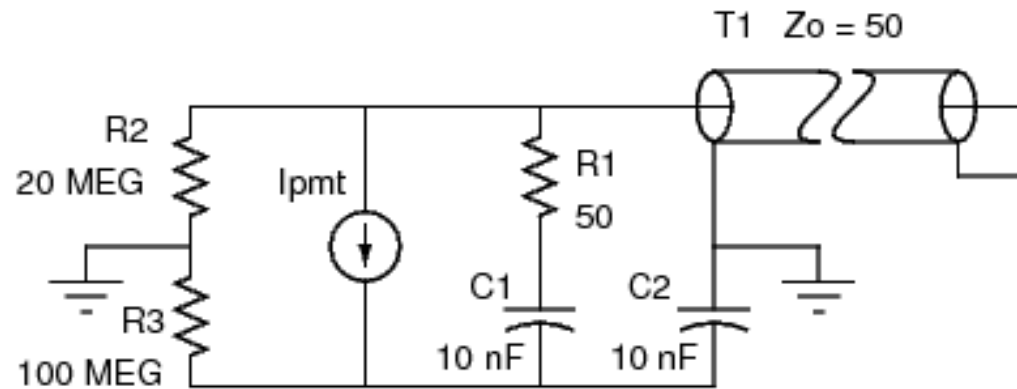
Airports, trucks

Signal simple Spice model



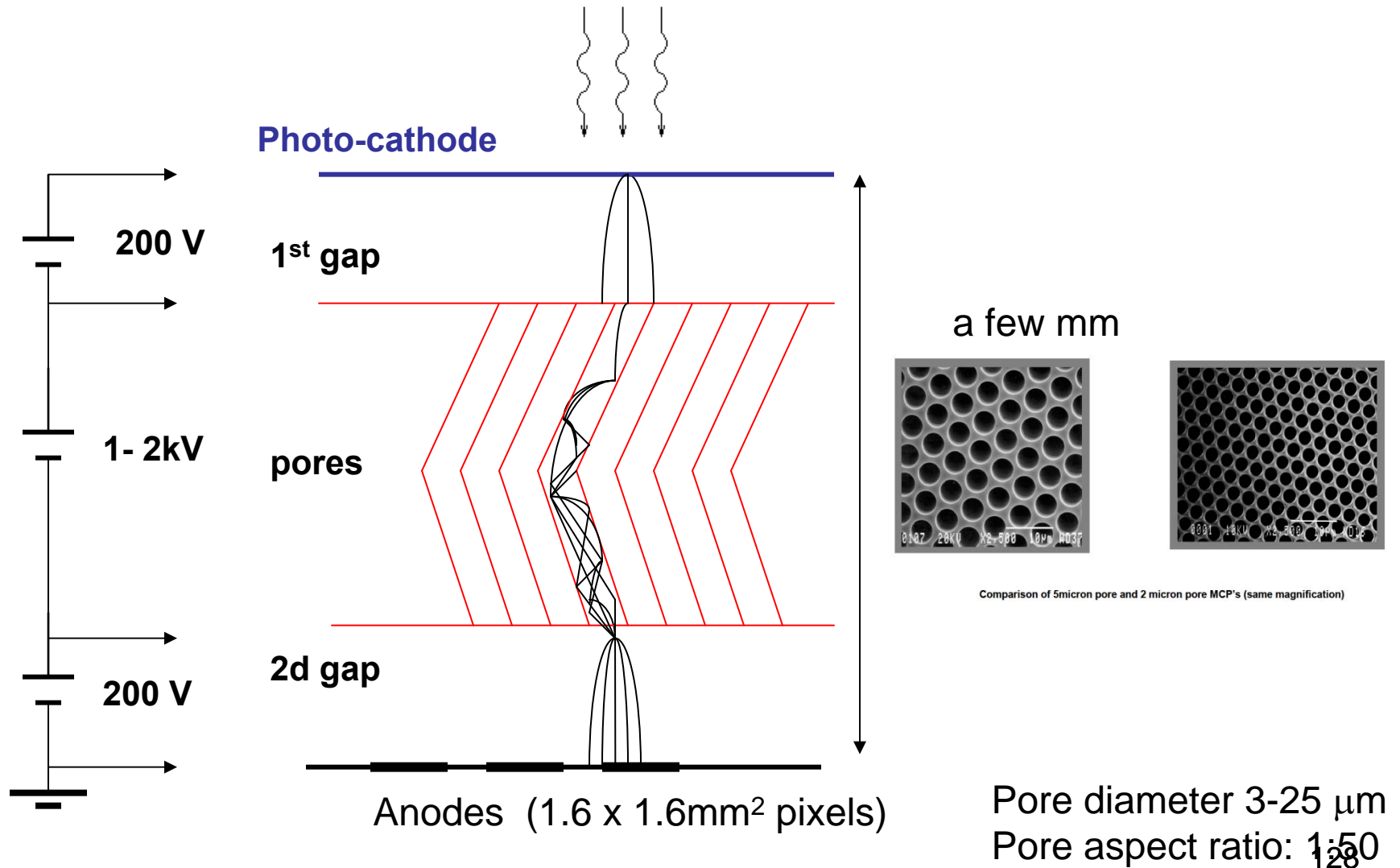
Spice detector model: difference of two exponentials

50 Ω Cable driving Spice model



SPICE Model of PMT Cable Driving Circuit

Micro-Channel Plate Detectors



Micro-Channel Plates

Optimization for timing

Reduce Transit time

The thinner, the best

Reduce pore size, primary and secondary gaps

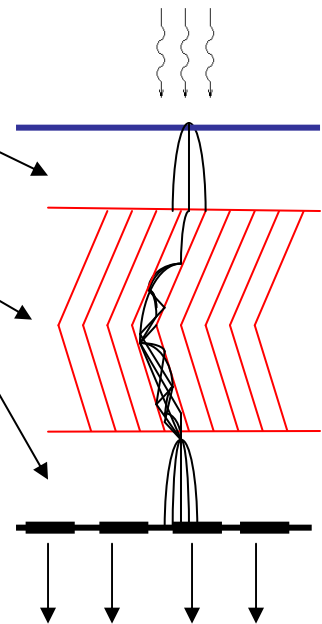
Avoid parasitic readout components

Connectors (!)

Parallel capacitances

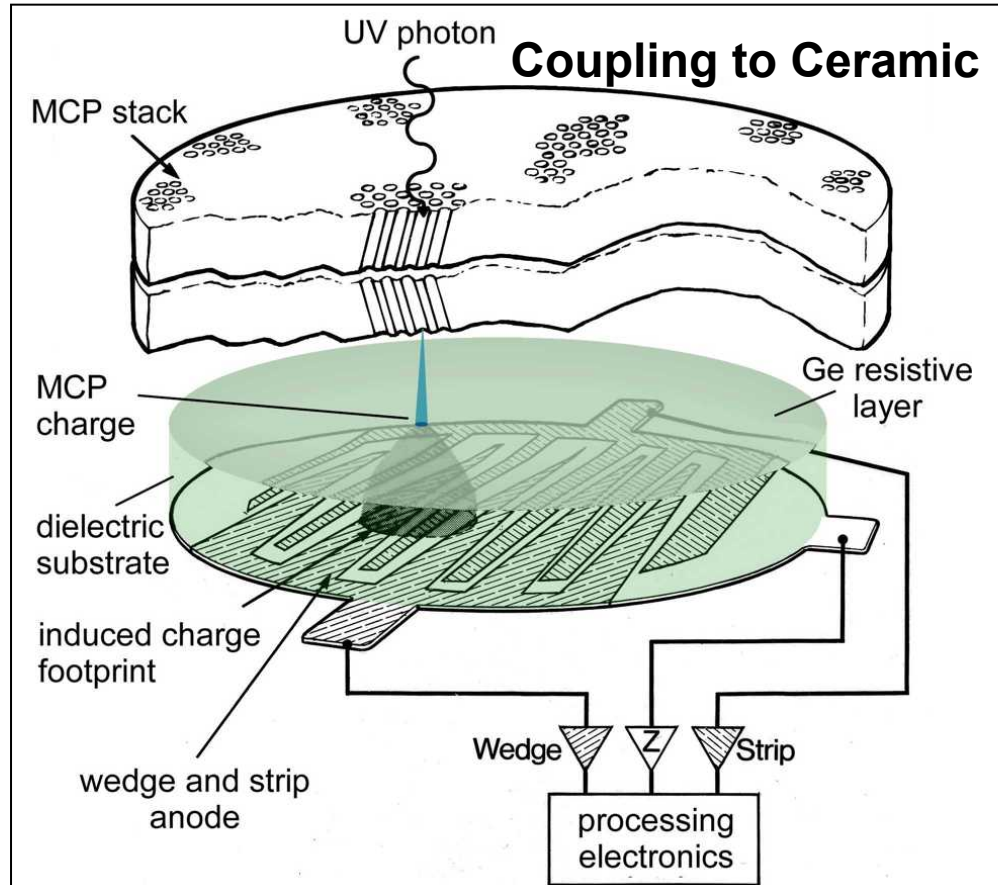
Series inductances

Reduce rise-time, consequently improve time resolution



Imaging Micro-Channel Plates Detectors

As imaging device...

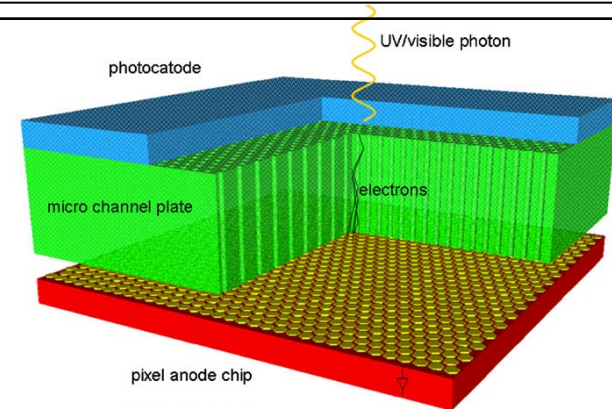
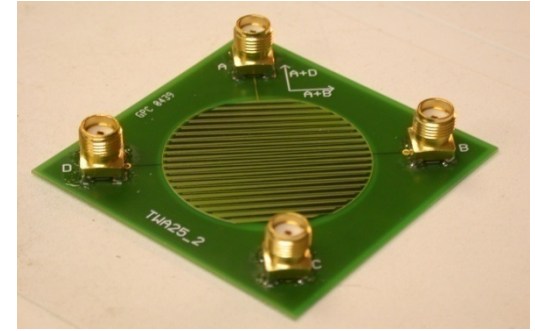


From J. Lapington, for WSO, Uni. Leicester, UK

Coupling to Board

Position: $10\mu\text{m}$ resolution

Time: 1ns



Coupling to ASIC: $3\mu\text{m}$

*From GLAST, Siegmund et al
NIM 591 2008*

Two-micron space resolution using analog charge division technique

R. Bellazzini et al. / Nuclear Instruments and Methods in Physics Research A 591 (2008) 125–128

High precision
analog measurements.

But
integration time=
200ns !

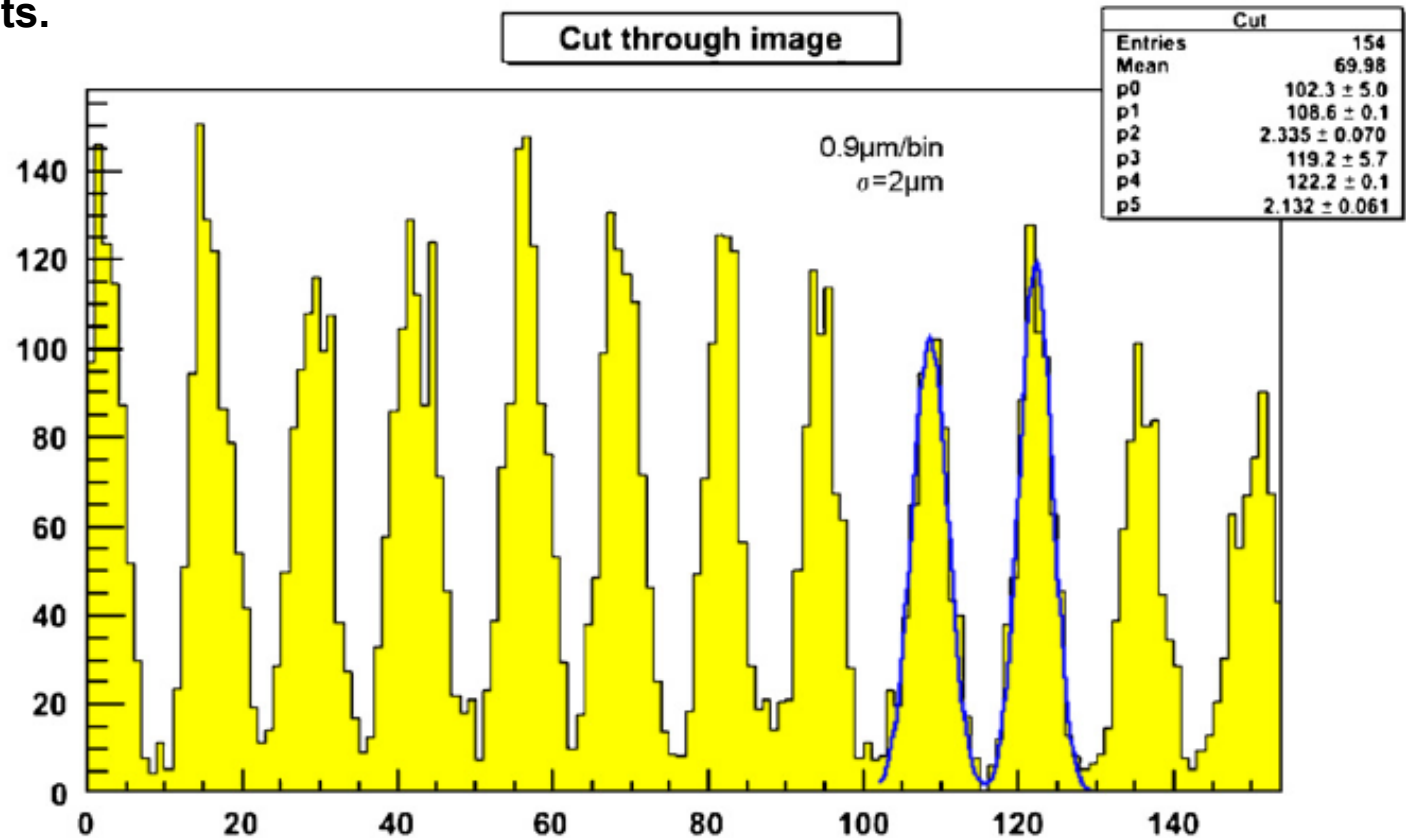


Fig. 4. A profile along a line cut across the MCP pores of Fig. 3. The spatial resolution of the readout is $\sim 2\mu\text{m}$ rms, capable of resolving every single MCP pore.

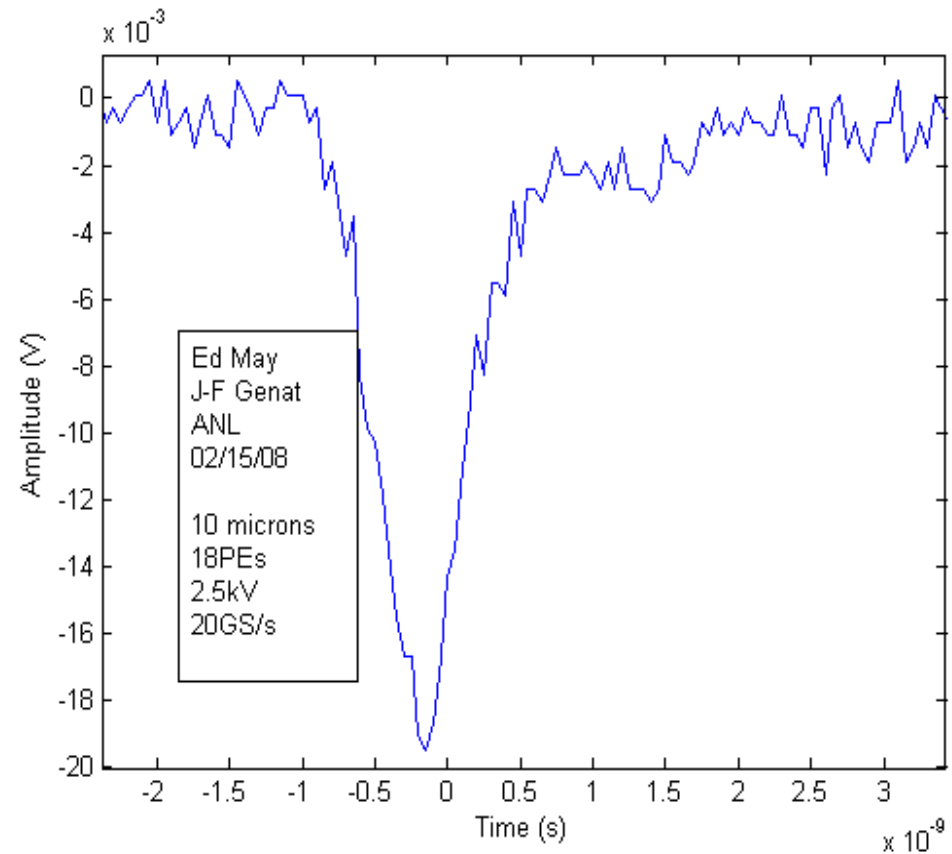
Micro-channel Plates Sampled Waveforms

- **Amplitudes (10 μ m, 2.5 kV)**

18 Photo-Electrons	20 mV
50 Photo-Electrons	35 mV
158 Photo-Electrons	78 mV

- **Rise times**

25μm	600ps
10μm	550ps

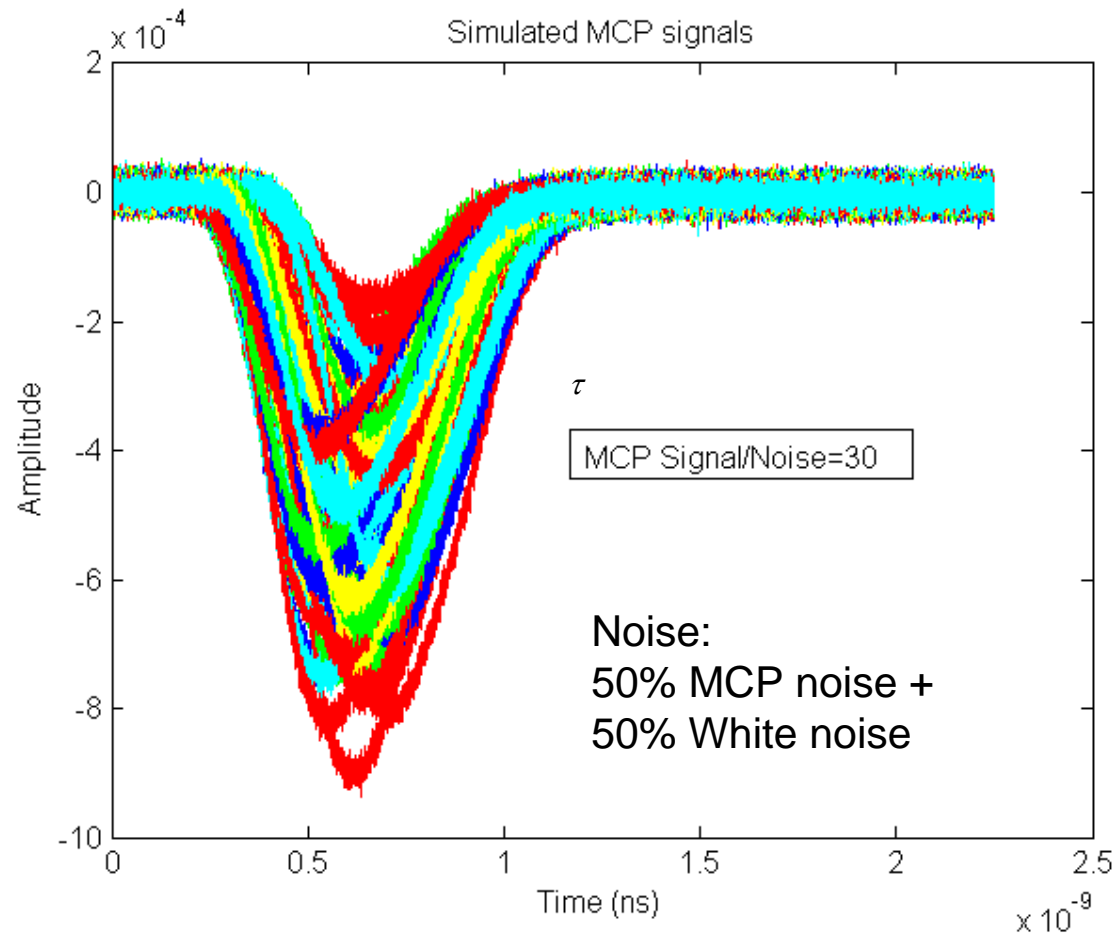


Synthesized signals for simulations

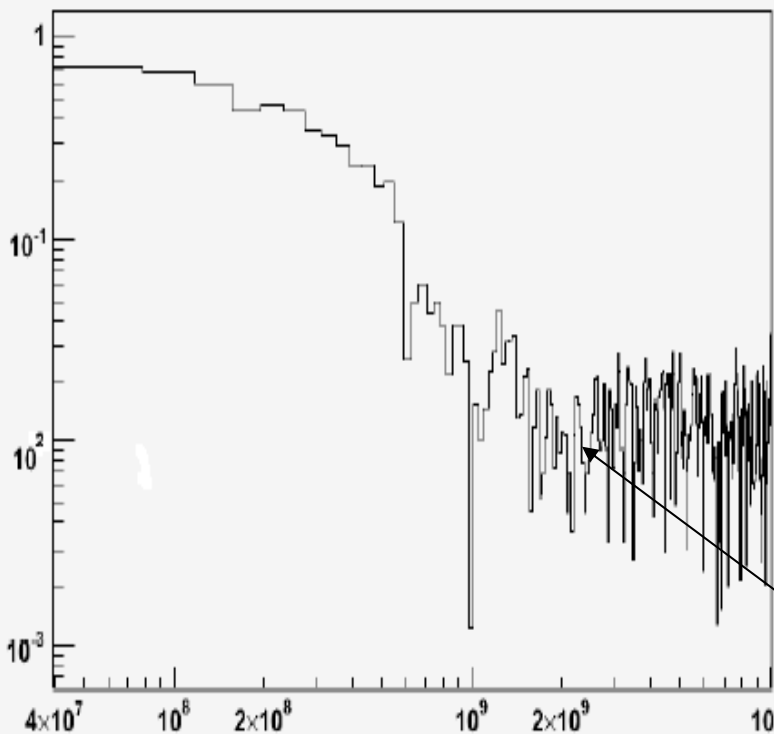
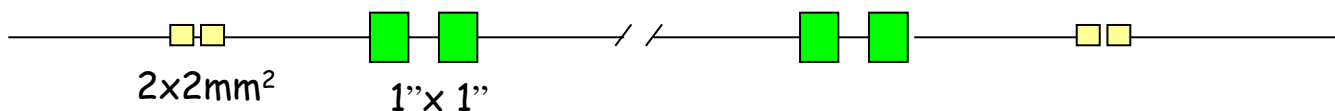


MCP signals: $(t/\tau) \exp(-t/\tau) \otimes (t/\tau) \exp(-t/\tau)$

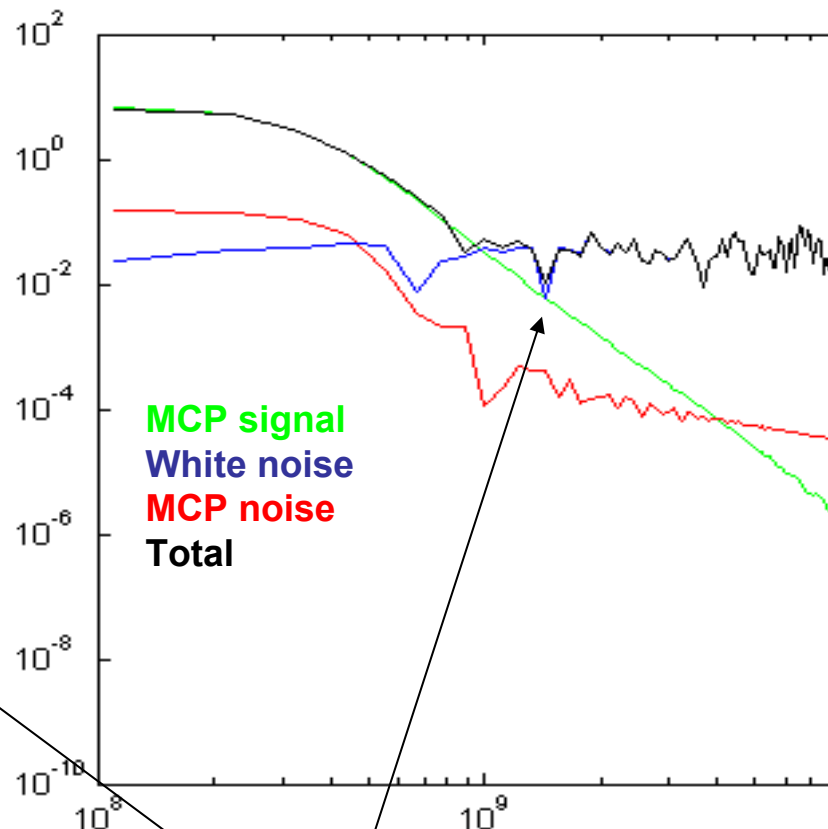
τ is tuned to a 280ps rise-time



MCP Signals spectra



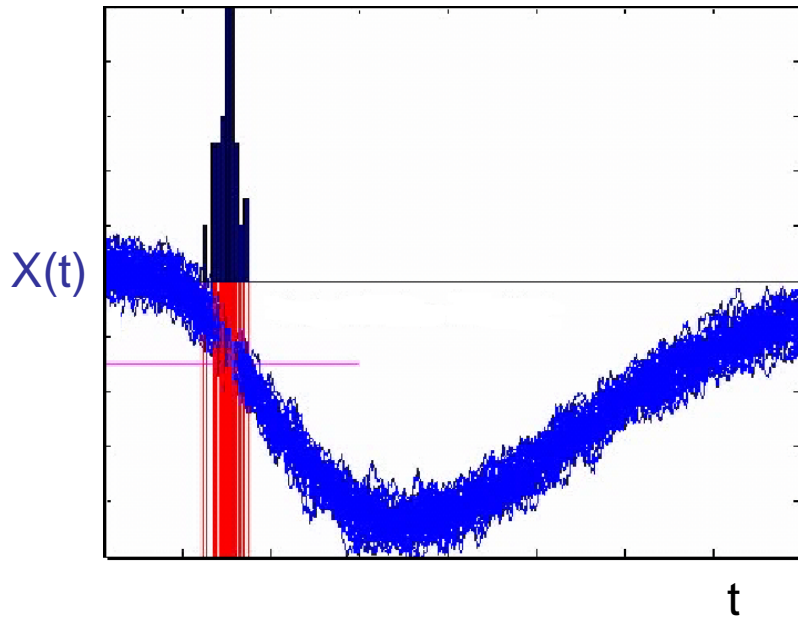
Measured (FNAL T979 Beam-Tests)



Simulated

Same noise corner at 1.2 GHz

Single Threshold: Noise and Slope



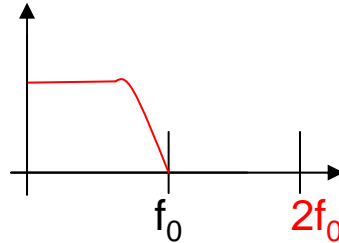
- $rms_{noise} = \sigma_x$

- $\sigma_t = \sigma_x / \frac{dx(t)}{dt}$

Single threshold: Time spread proportional to amplitude noise and inverse to slope

Pulse sampling and Waveform analysis

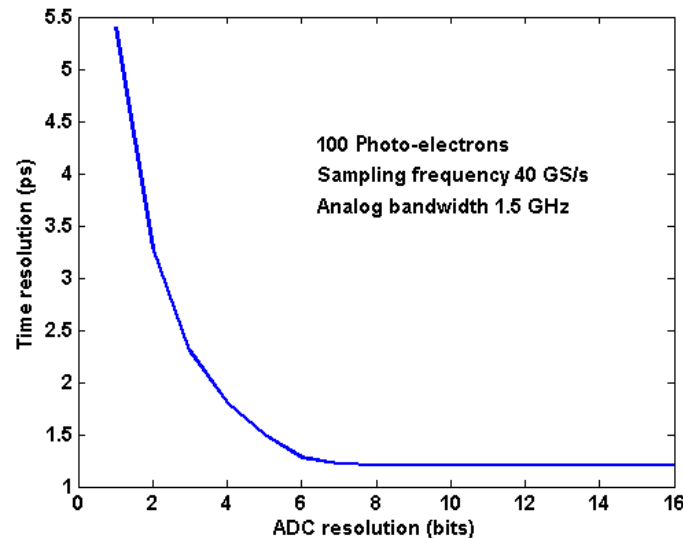
- Sampling frequency: Set at twice the largest frequency in the signal spectrum



- Digitization: Evaluate what is needed from signals properties:

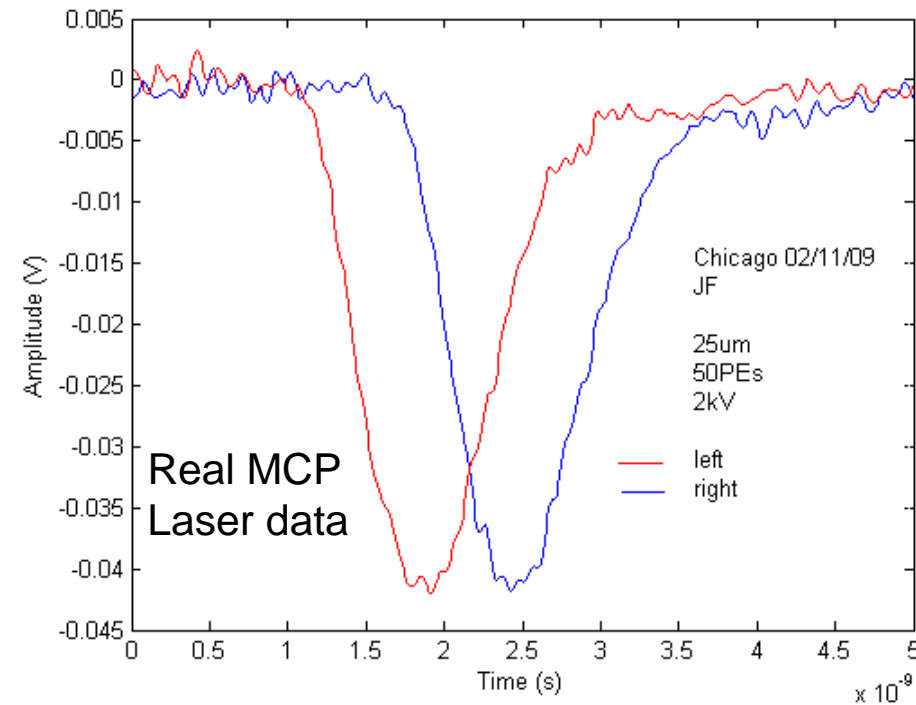
Example:

MCP signals



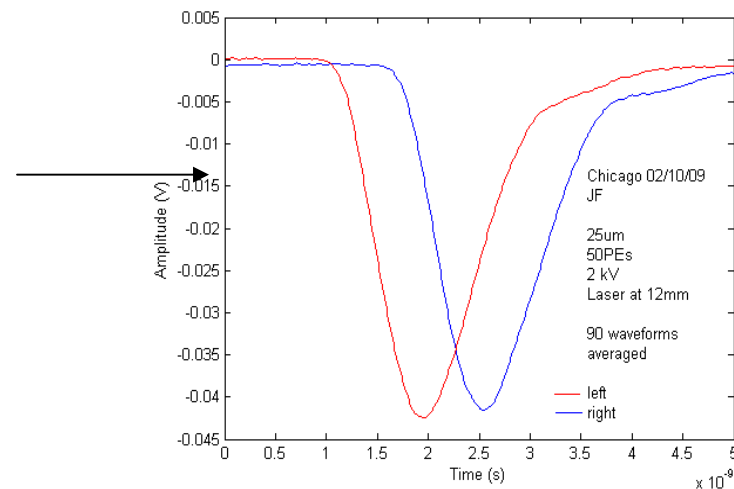
Sampled pulses analysis

Many techniques



B. Cleland and E. Stern, BNL

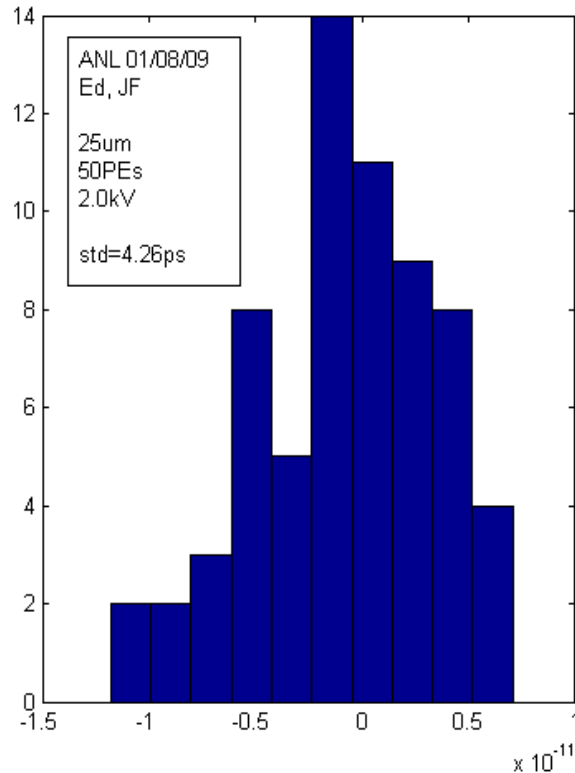
Signal Template



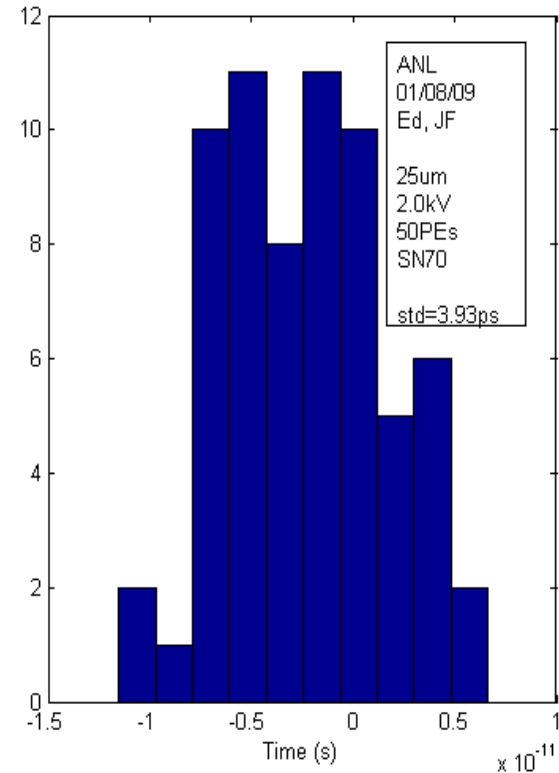
- Extract precise time and amplitude from minimization of χ^2 evaluated wrt a template deduced iteratively from the measurements, at the two ends of the T-line.
- With T-lines, the two ends are highly correlated, so, MCP noise is removed.

Iterative template

At T-lines ends



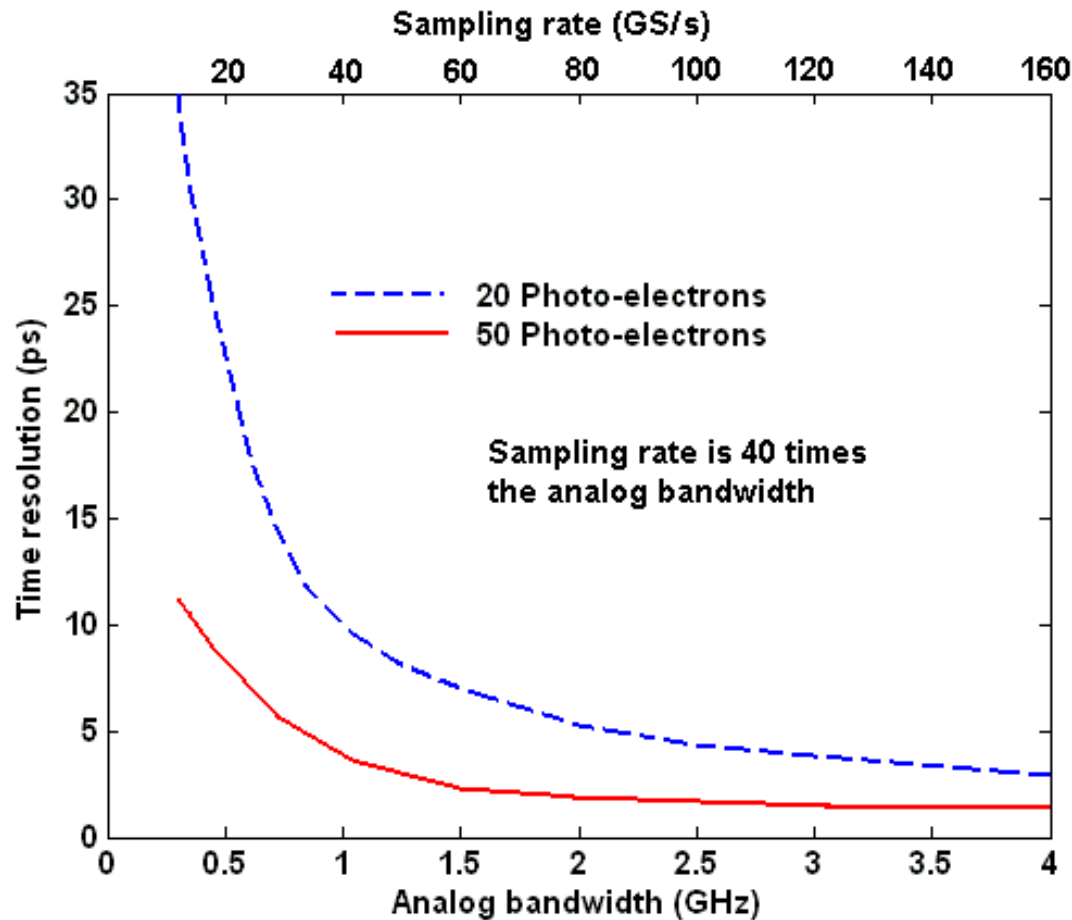
Template from average
std= 4.26ps



Template iterative
std=3.93

Pulse sampling

Timing resolution vs Sampling rate (simulation)

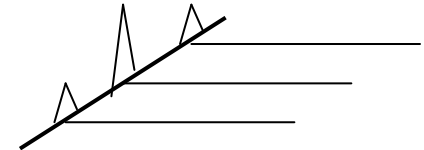


Timing resolution vs Sampling rate / Analog bandwidth

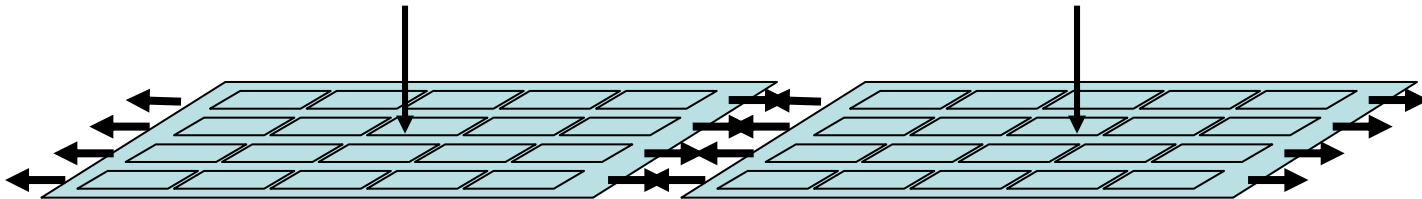
Pulse sampling benefits

Pulse sampling and waveform analysis:

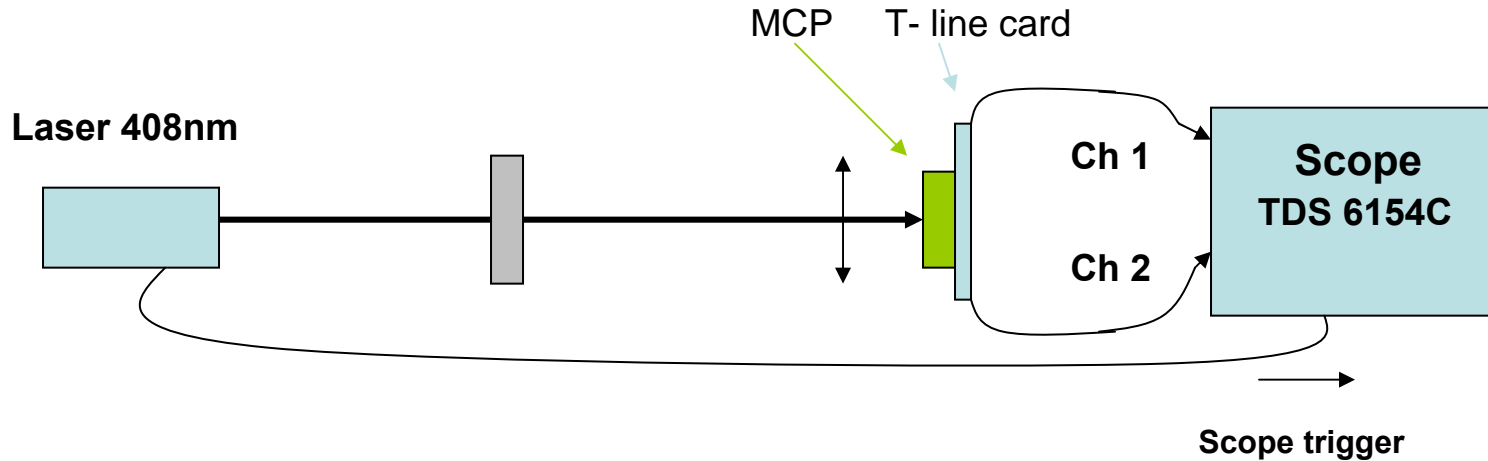
- Picosecond timing with fast detectors
- Charge: centroids for 2D readout
- Resolve double pulse



For large area detectors read with delay lines in series



Position sensing using fast timing

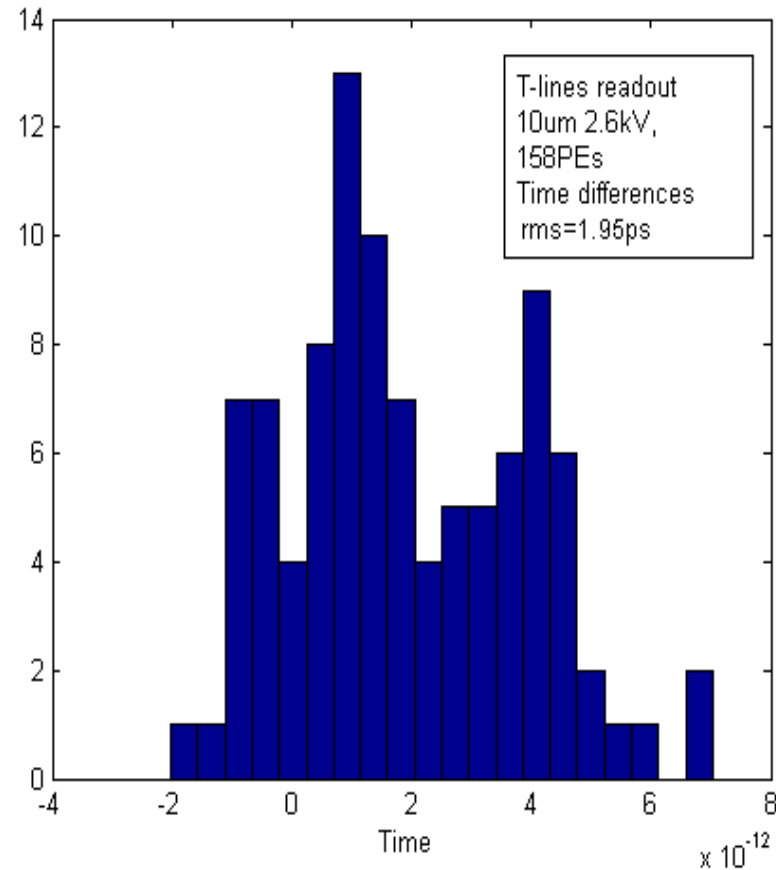


- Edward May, Argonne:

Laser test bench calibrated with the single PE response of a Quantacon (single photon sensitive) PMT.

- 25/10um pores MCP on transmission lines card
- Scope triggered by the (somewhat jittery) laser signal
- Record two delay lines ends from the same trigger
- Tek 6154C scope at 20 Gs/s

Results



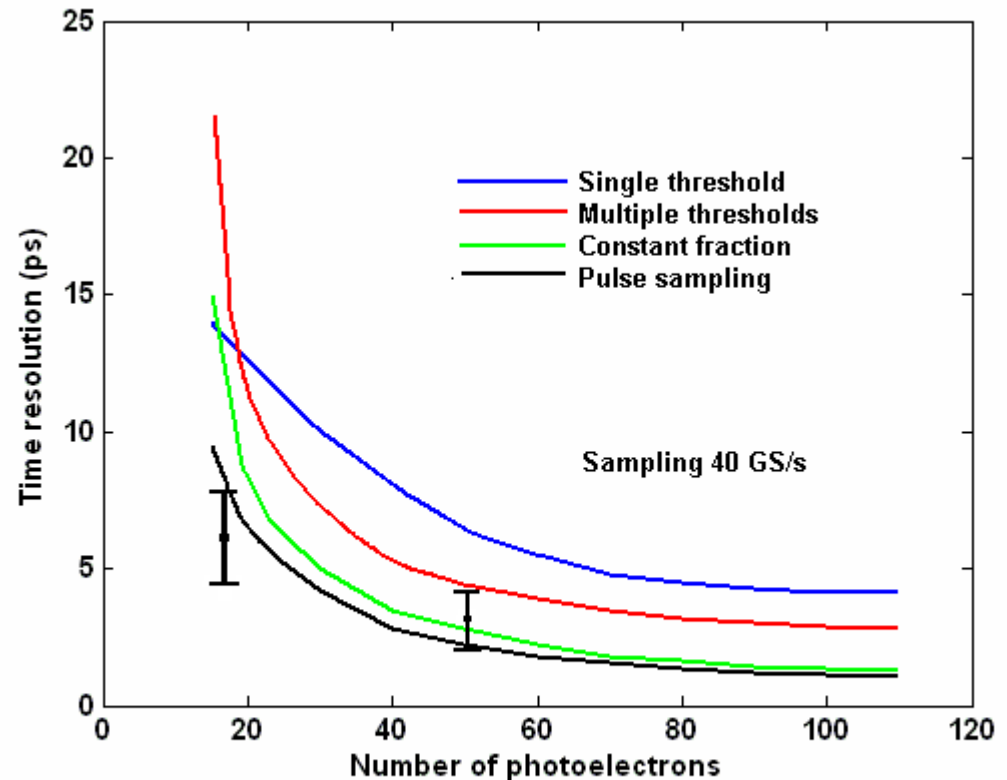
Position resolution (velocity=8.25ps/mm) :	50PEs	4.26ps	213μm
	158PEs	1.95ps	97μm

Measurements vs simulation

50PEs rms=3.82ps vs 2.5ps (simulation)

18PEs rms = 6.05ps vs 7ps (simulation)

Measurements
do not match exactly
since MCP noise
is partly removed
(T-lines ends correlated)



Position Resolution at 158PEs

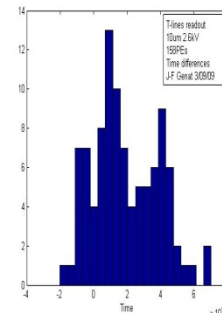
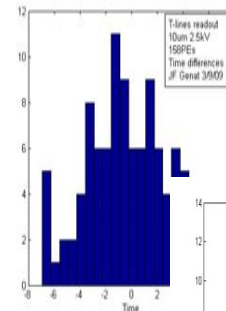
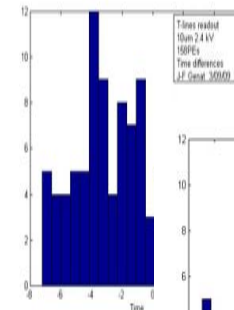
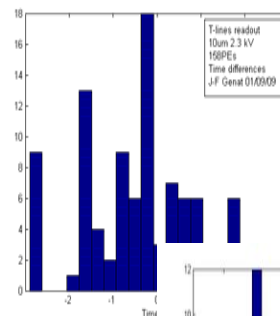
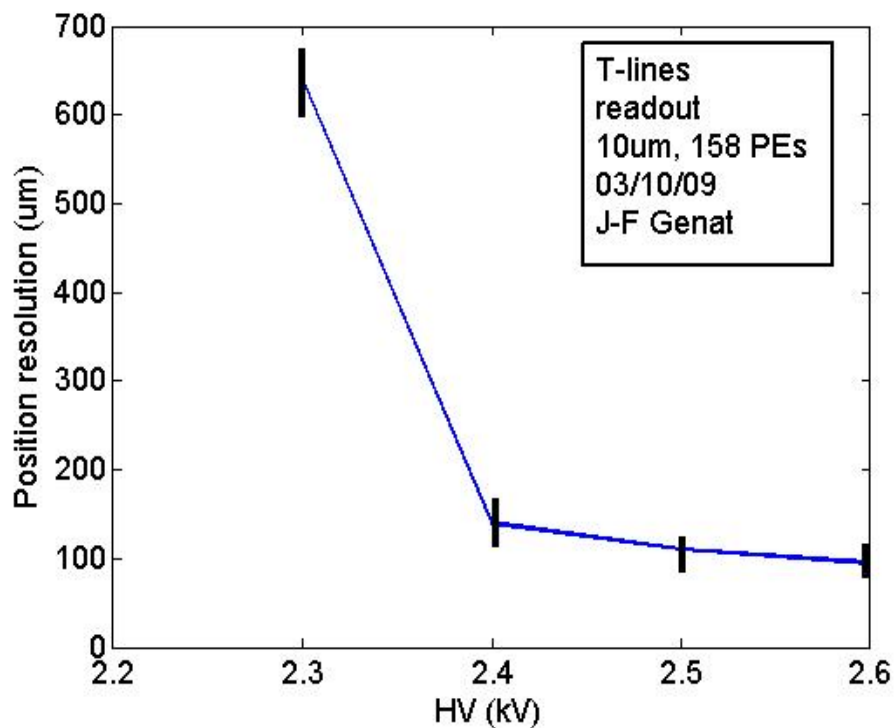
158 PEs

HV = 2.3 kV
Std 12.8ps
640 μ m

HV = 2.4 kV
2.8ps
140 μ m

2.5 kV
2.2 ps
110 μ m

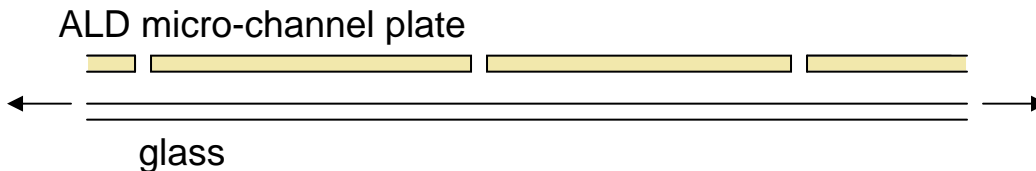
2.6 kV
1.95 ps
97 μ m



Transmission lines as anodes

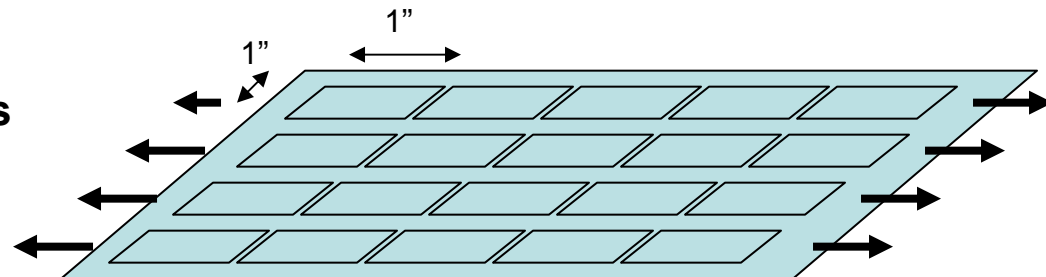
- Present Photonis MCPs:
Pixellated anodes, pitch of 1.6 x 1.6 mm
 - Atomic Layer Deposition (ALD) detectors
 - Waveform sampling with fast sampling chips
- Integration of lines as anodes in vacuum for large area sensors
- Plates of 1" x 1" in ALD process
- Modules of 8 " x 8 " ?
- One vacuum vessel (glass)

Henry Frisch, (U-Chicago)
W. Hau, M. Pellin (ANL)



Check in vacuum
T-lines coupled to Micro-Channel Plates
(impedance, velocity)

B. Adams, K Attenkoffer, ANL



MCPs: Best position resolution

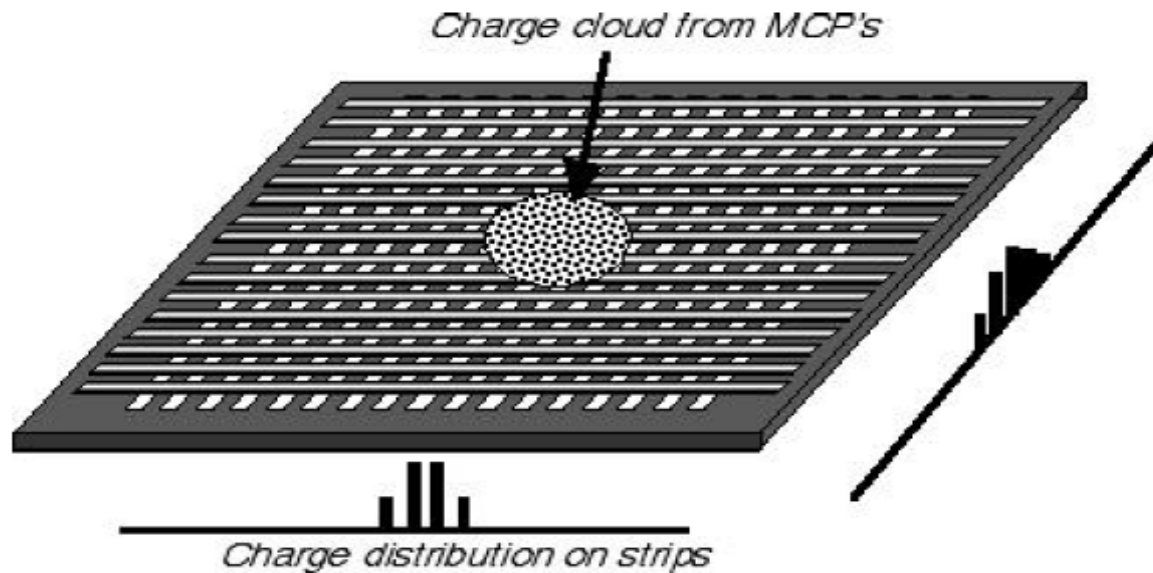


Figure 1. Schematic of the cross strip anode showing the MCP charge cloud, and charge distribution on the cross strips.

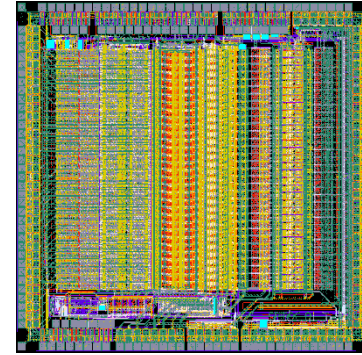
A few microns position resolution using **analog weighted sums**

O. Siegmund, A. Tremsin (SSL Berkeley)

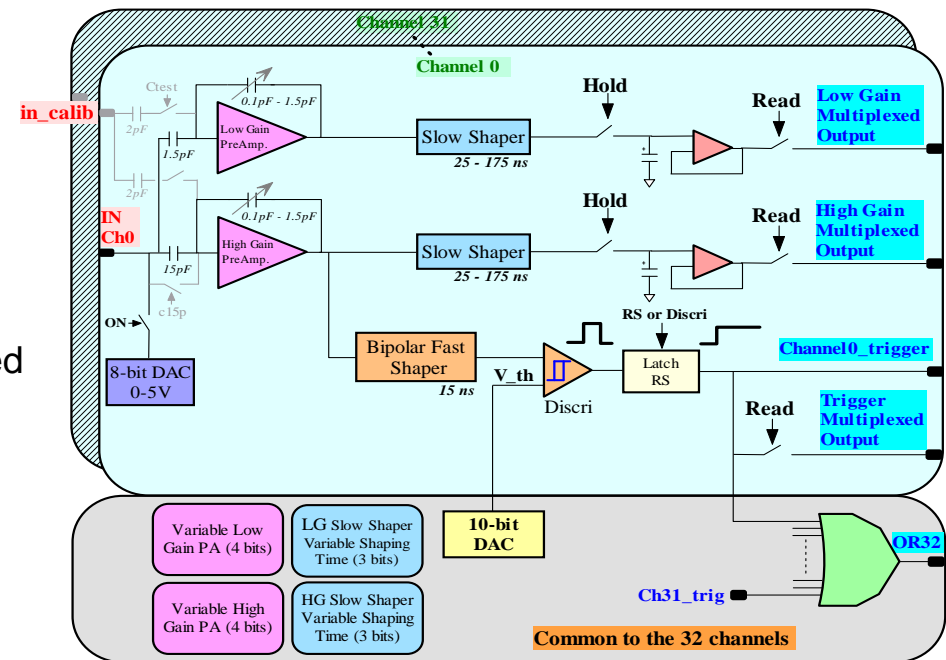
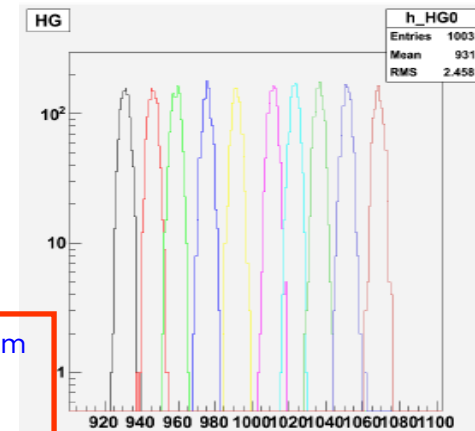
Silicon PMs Readout: SPIROC

350nm
Silicon-Germanium

- **32-Channel ASIC for Silicon PM readout**
Includes 32 x 16-deep analog memories and ADCs
- **Internal input 8-bit DAC** (0-5V) for individual SiPM gain adjustment
- **Energy measurement : 14 bits**
 - 2 gains (1-10) 1 pe \rightarrow 2000 pe
 - Variable shaping time from 25ns to 175ns
 - pe/noise ratio : 11
 - 2 Multiplexed outputs for low gain and high gain
- **Trigger output**
 - pe/noise ratio on trigger channel : 24
 - Fast shaper : ~ 10 ns
 - Trigger on 1/3 pe (50fC)
 - 32 trigger outputs
 - OR 32 output
 - **Trigger latch** for each channel and multiplexed output
- Individually addressable calibration injection capacitance
- **Embedded features**
Power pulsing, bandgap, 10-bit DAC

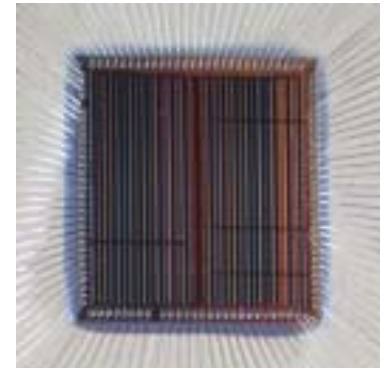
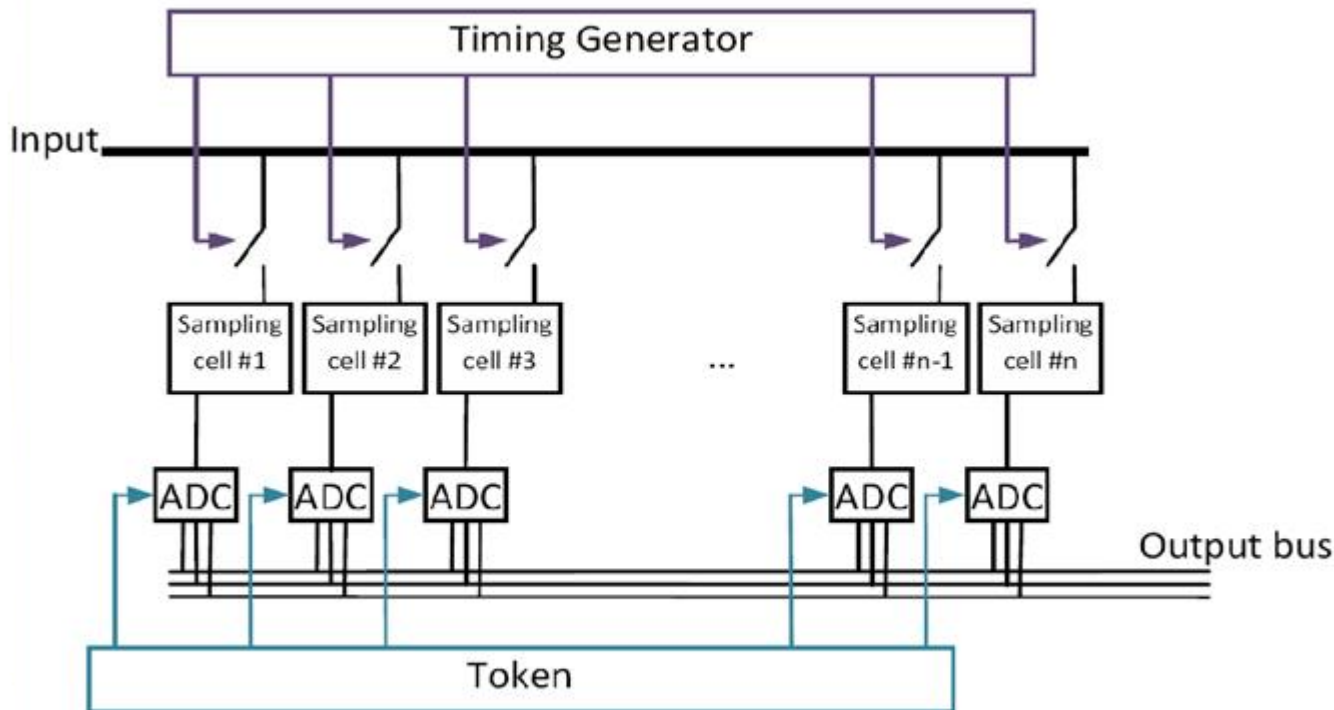


Fabricated in SiGe AMS 0.35 μ m
Delivered in December 2009
Chip area: 17 mm²



Switched Capacitor Arrays (SCA)

- Sampling capacitors: 50-100 fF, input bus 200-1k Ω
- Analog bandwidth = $1/2\pi RC = 1-10\text{GHz}$
- Dynamic range 10-13 bits limited by noise and voltage droop before readout
- Timing generator using voltage controlled delay elements of 50-500ps
- Depth can be very large (64k) if bandwidth is not constrained
- Very low power (readout dominated)
- Used in fast oscilloscopes



15 GS/s 130nm CMOS