PV-lab
IMT NEUCHATEL

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Amorphous Silicon Based Microchannel Plates

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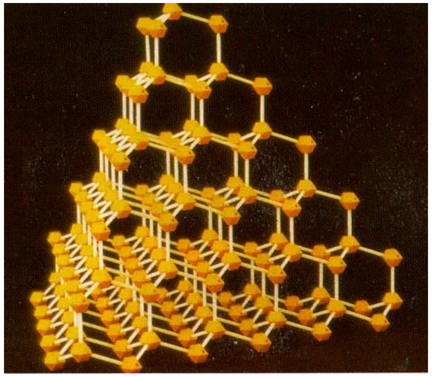
Outline

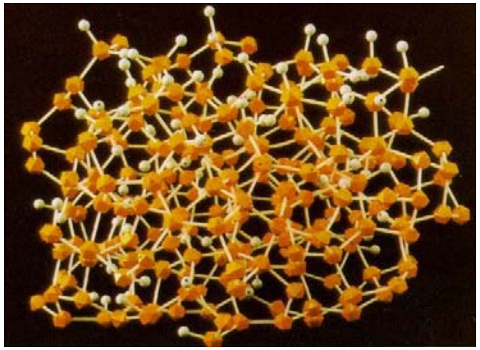
- Introduction to hydrogenated amorphous silicon (a-Si:H)
- a-Si:H microchannel plate (AMCP) advantages
- AMCP fabrication process
- AMCP characterization with EBIC technique
- Results and conclusions

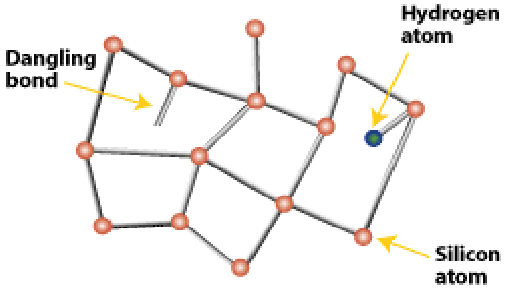
Hydrogenated amorphous silicon (a-Si:H)

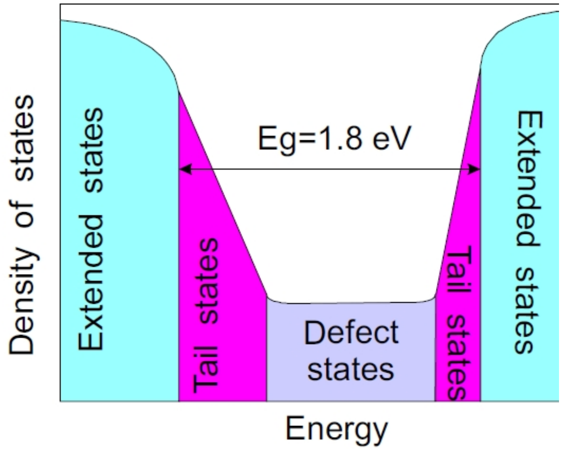
crystalline silicon (c-Si)



hydrogenated amorphous silicon (a-Si:H)





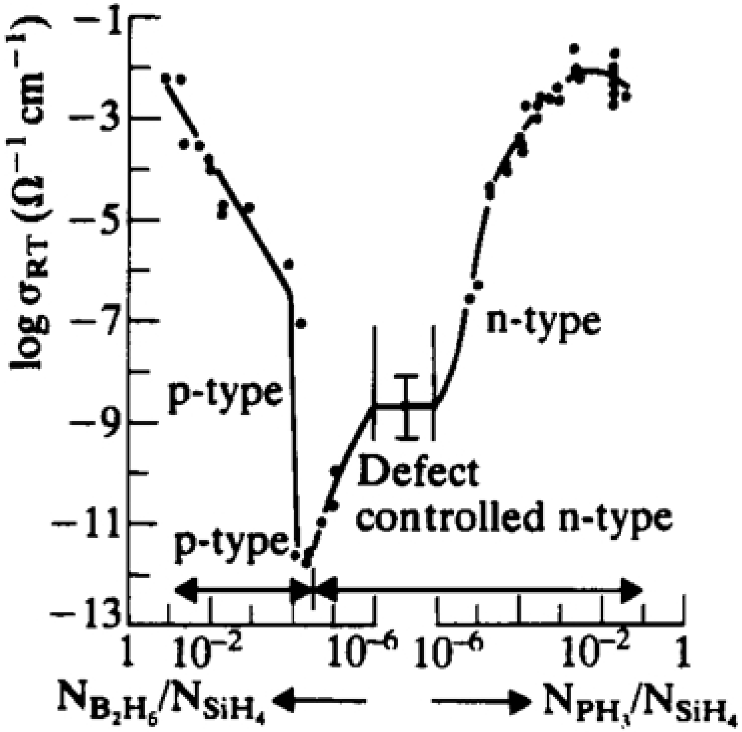


- tetrahedral structure conserved at short range, disorder at long range
- 2-20% of hydrogen reduces the dangling bonds down to ≈ 10^{16} cm^{-3}
- $E_{g,a\text{-}Si:H}$ = 1.8 eV vs. $E_{g,c\text{-}Si}$ = 1.1 eV

a-Si:H conductivity

Electrical properties	c-Si	a-Si:H
Drift mobility [$cm^2 \cdot V^{-1} \cdot s^{-1}$] electrons (holes)	1350 (450)	≈ 1 ($3 \cdot 10^{-3}$)
Conductivity [$\Omega^{-1} \cdot cm^{-1}$]	≈ 10^{-10} - 10^{-7}	≈ 10^{-10} - 10^{-12}

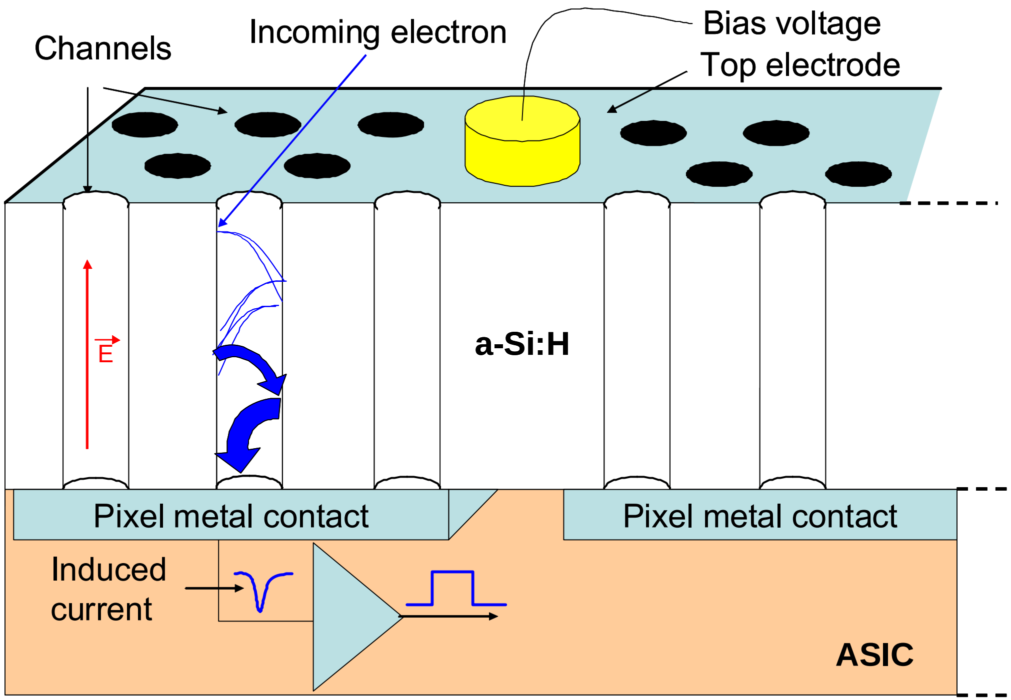
a-Si:H conductivity changes with either phosphorous or boron doping



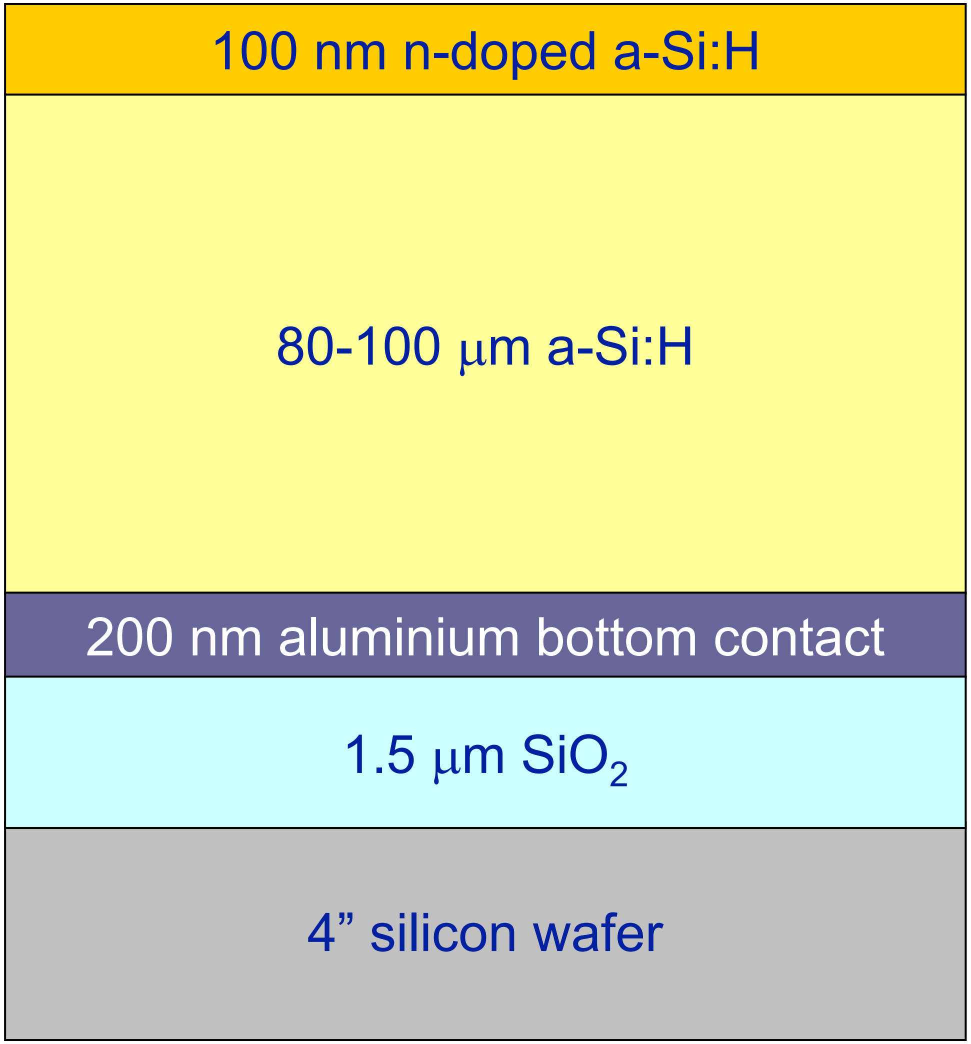
Spear, Phil. Mag. 33 (1976)

Advantages of AMCP

1. no need for "strip resistance" and "insulating" layers (intrinsic a-Si:H $\sigma_{dark} = 10^{-10} - 10^{-12}\ \Omega^{-1}\cdot cm^{-1}$)
2. use of the c-Si micromachining technologies
3. possibility of a vertical integration on Application Specific Integrated Circuit (ASIC):
   a-Si:H Tdep < 250 ºC



AMCP realization



Plasma-enhanced chemical vapor deposition (PE-CVD)

f = 70 MHz

T_{dep} = 225 ºC

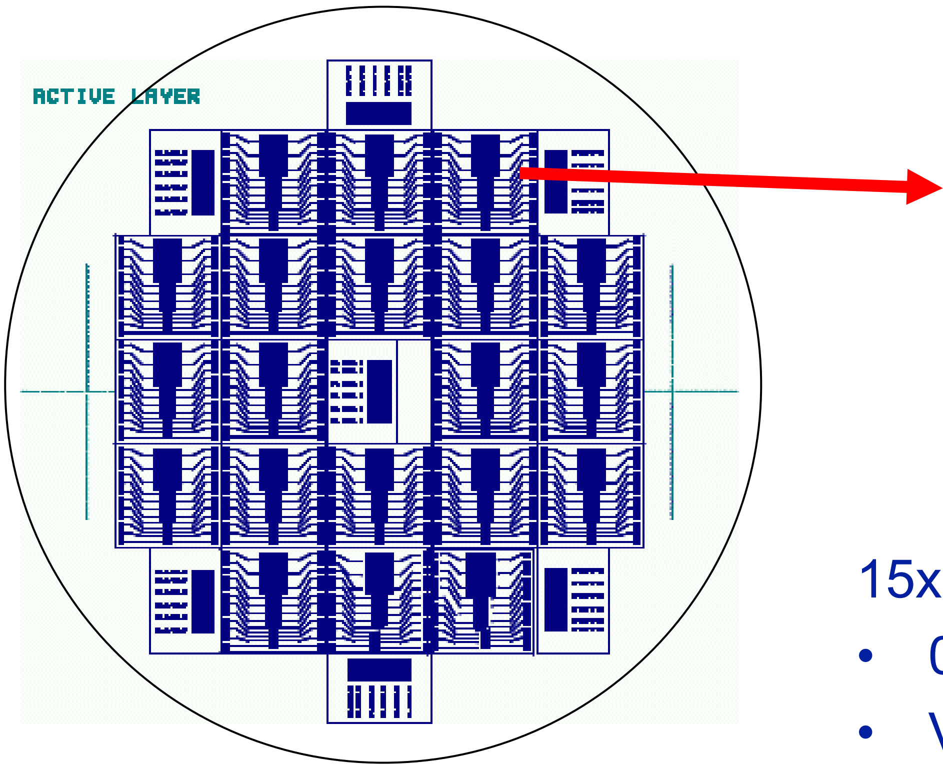
[SiH4]/[H2] ≈ 3.7

deposition rate ≈ 1.5 nm/s

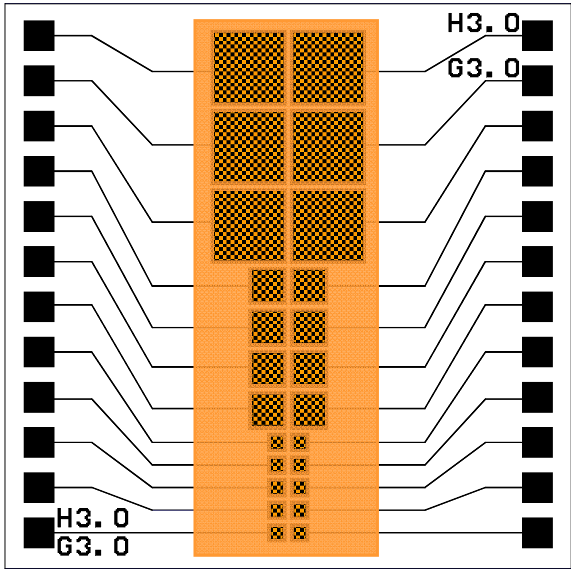
evaporation or sputtering

thermal oxidation

AMCP test prototypes



4” oxidized Si wafer

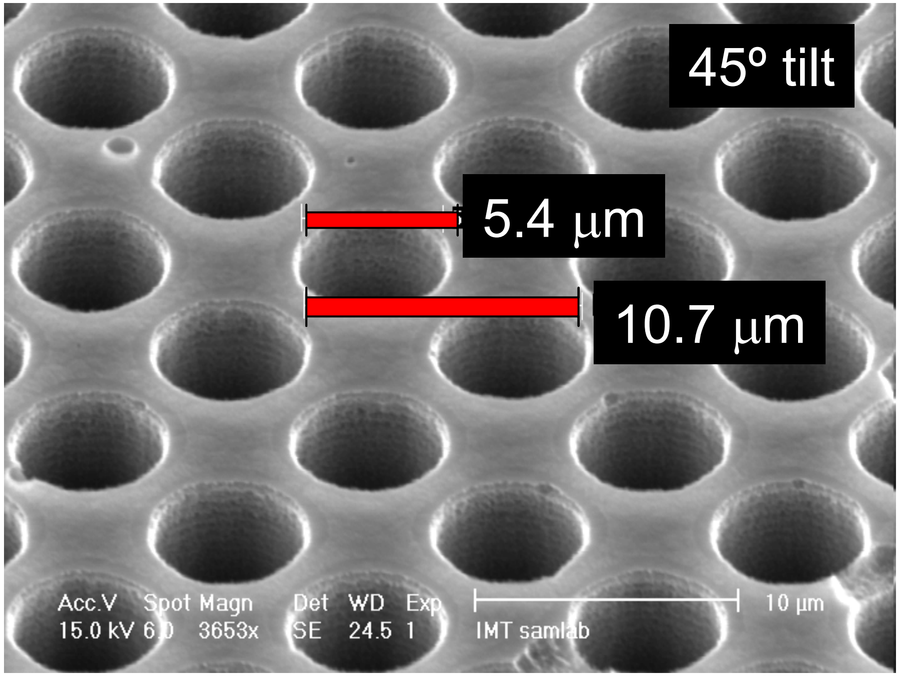


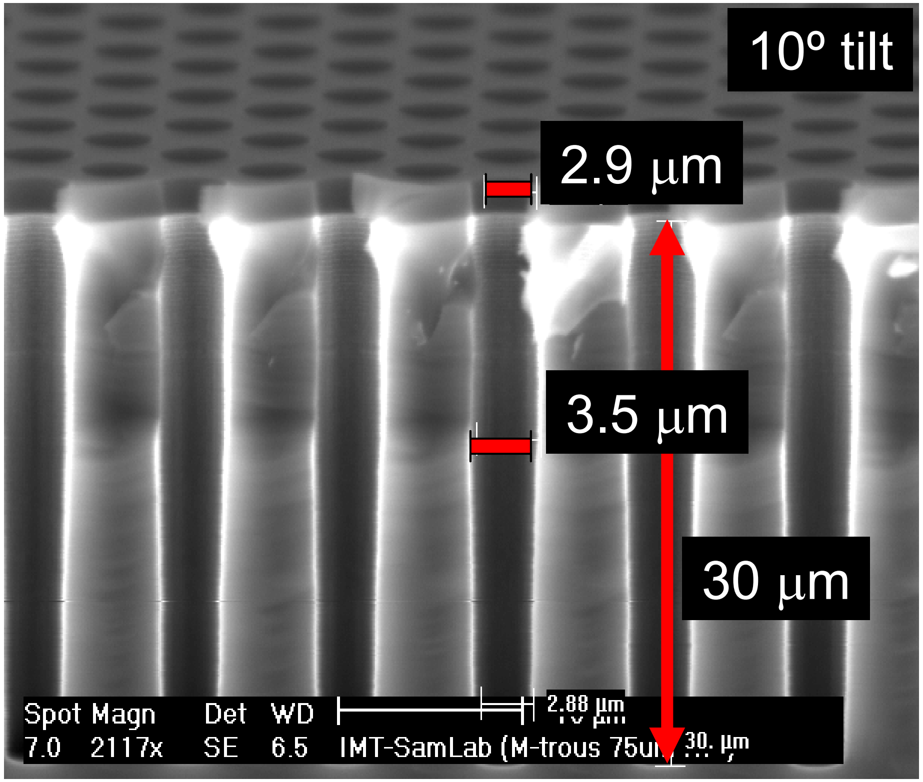
15x15 mm^2 reticules with 16 pixels

- 0.5 x 0.5 – 2 x 2 mm^2 pixels
- Various channel diameters:
  2 – 6 µm in diameter
- Various channel gaps:
  2 – 4 µm

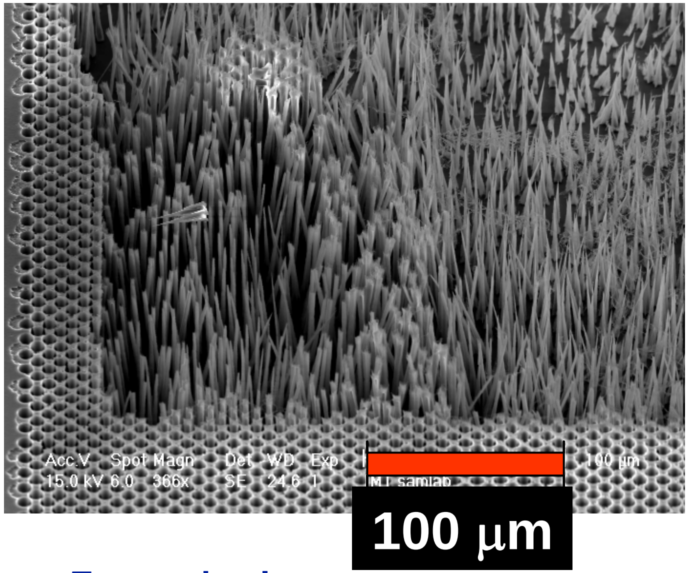
Deep Reactive Ion Etching (DRIE)

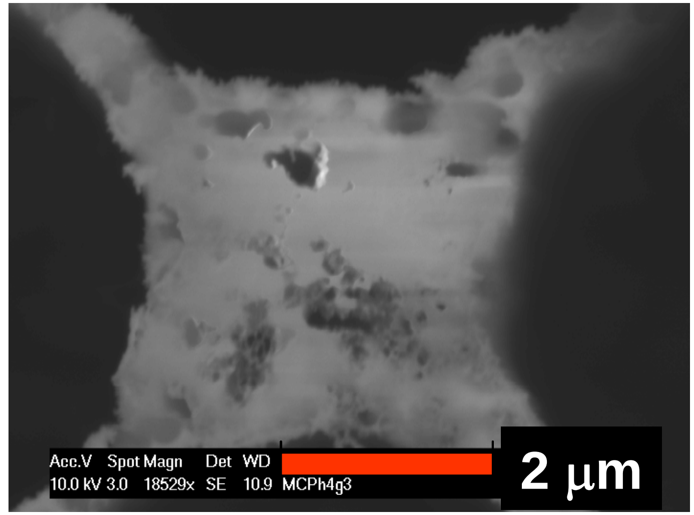
Performing alternate steps of etching and passivation





Issues of first AMCP generation

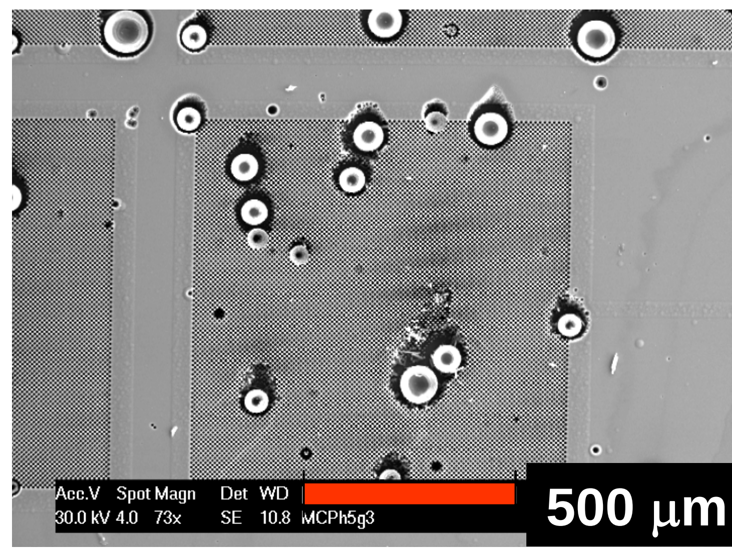




- 6 µm holes
- 3 µm gap
- degraded top surface with high resistivity

- 5 µm holes
- 2.5 µm gap
- Collapse of amorphous silicon layer

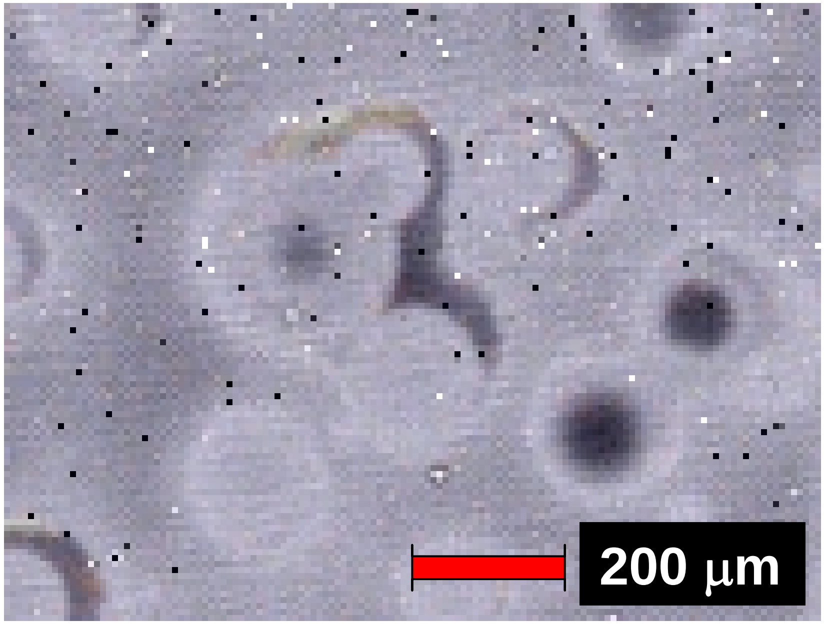
- big columnar defects
- possible stresses in the layer and/or due to DRIE



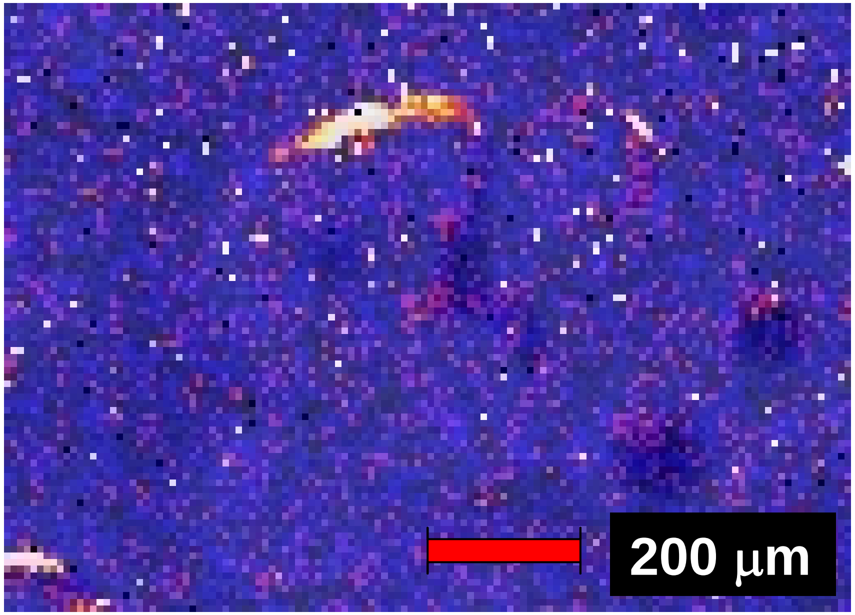
AMCP leakage current

1. No blocking contacts and defective structure (~ μA)
2. Lock-in thermography measurement reveals localized areas with high leakage currents
3. Bias voltage is limited to **-340 V**

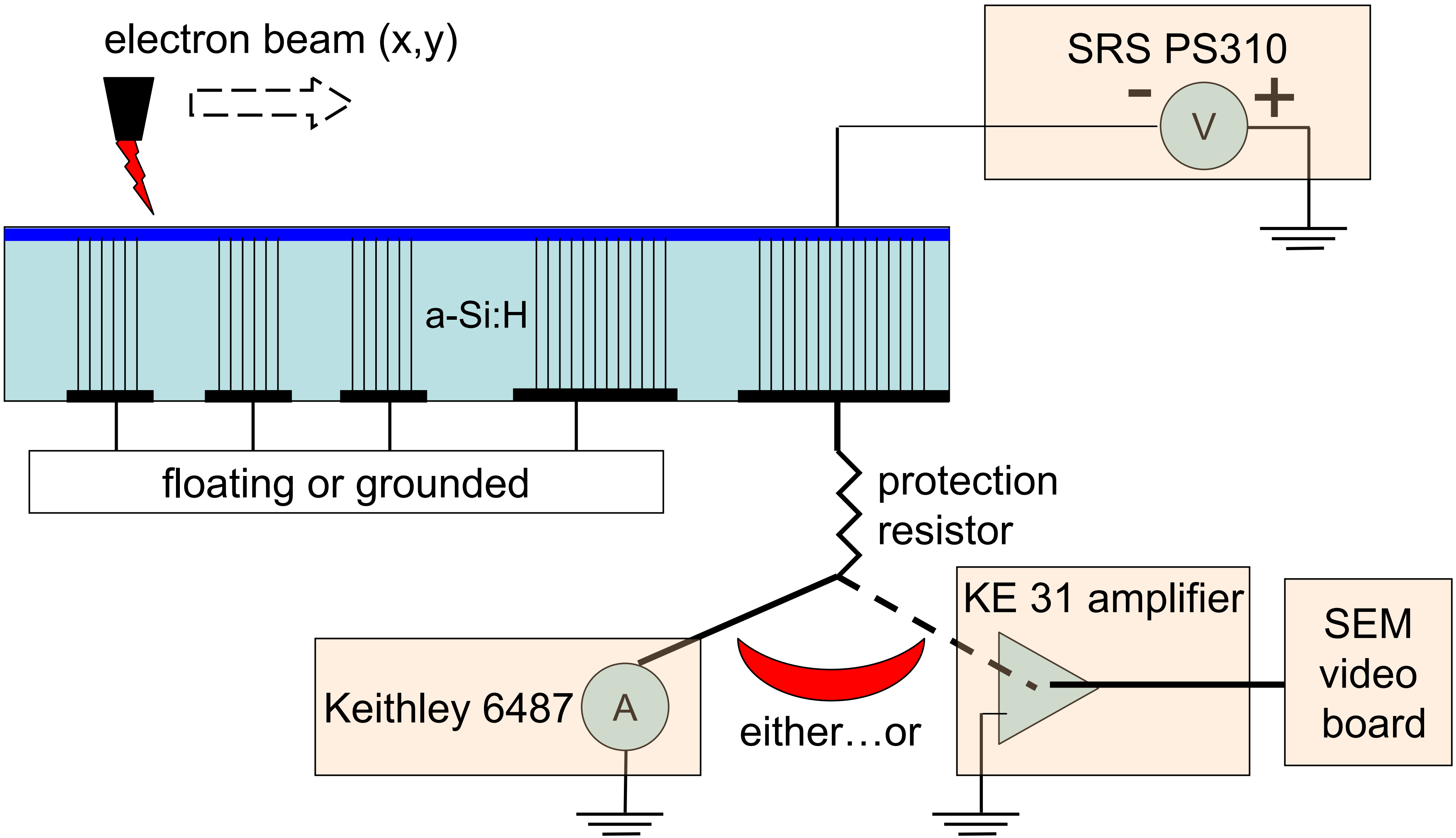
Optical microscope



Lock-in thermography

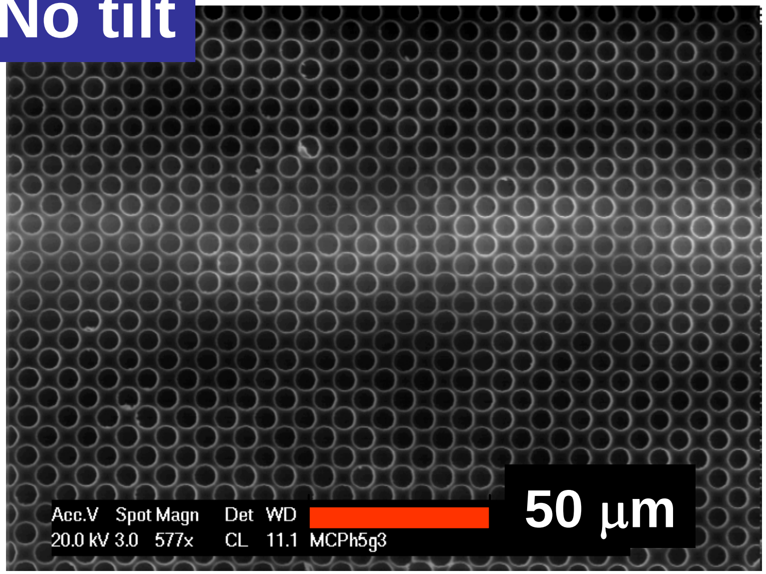


AMCP characterization with EBIC technique

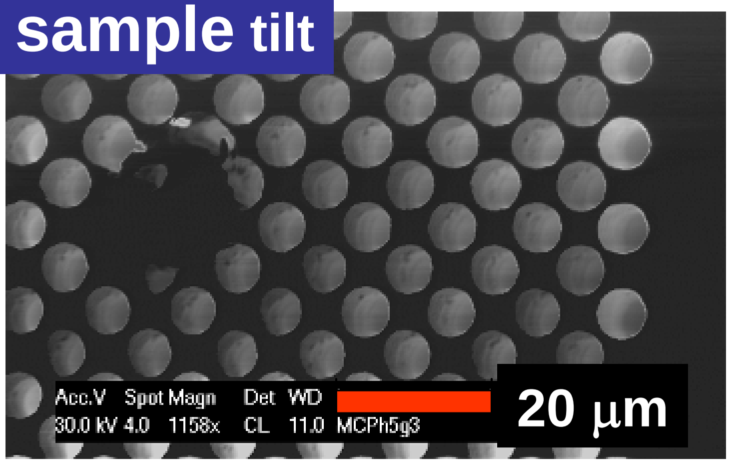


EBIC maps: tilting effect

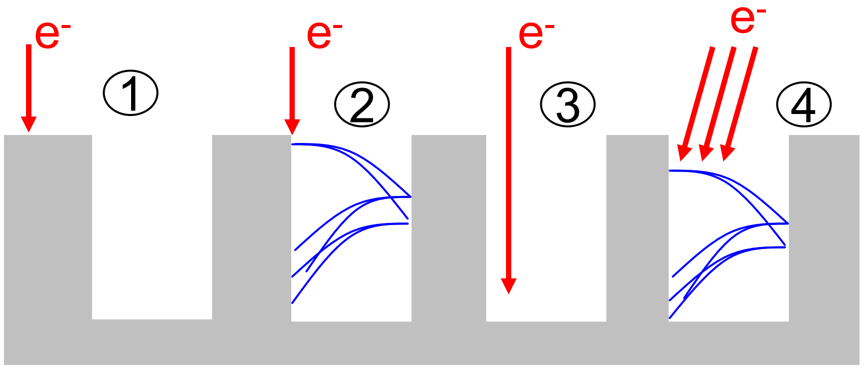
No tilt



10º sample tilt

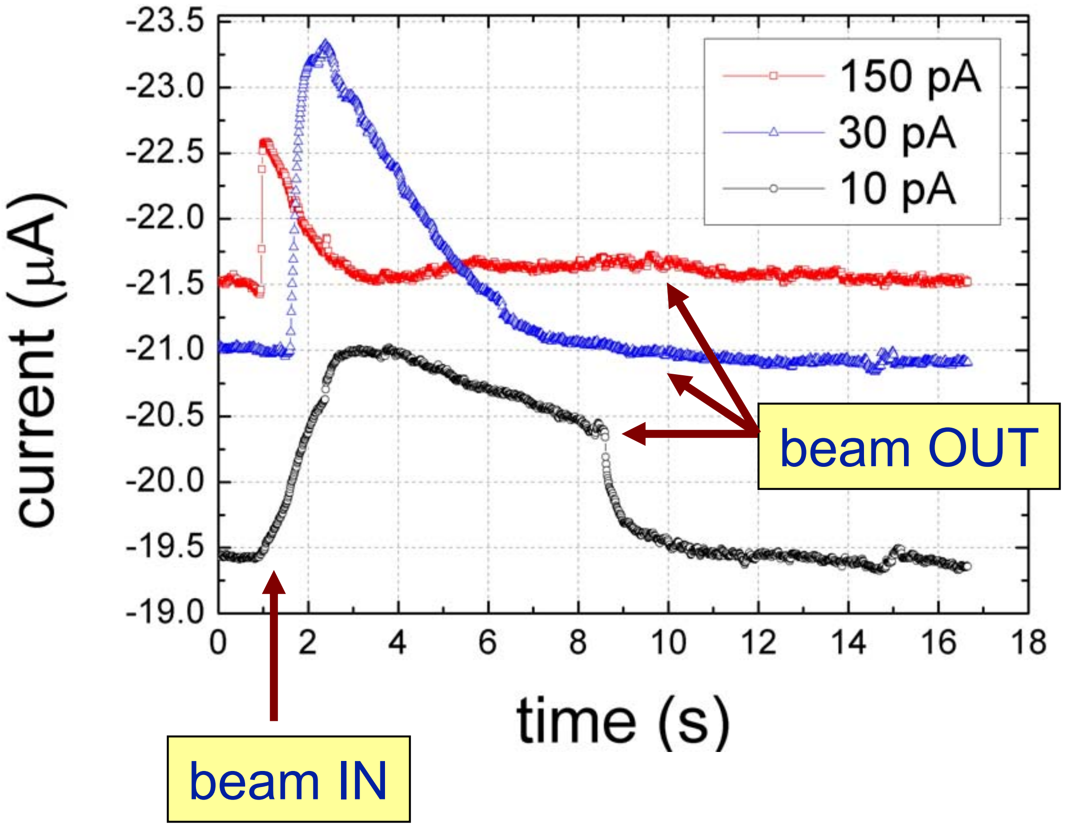


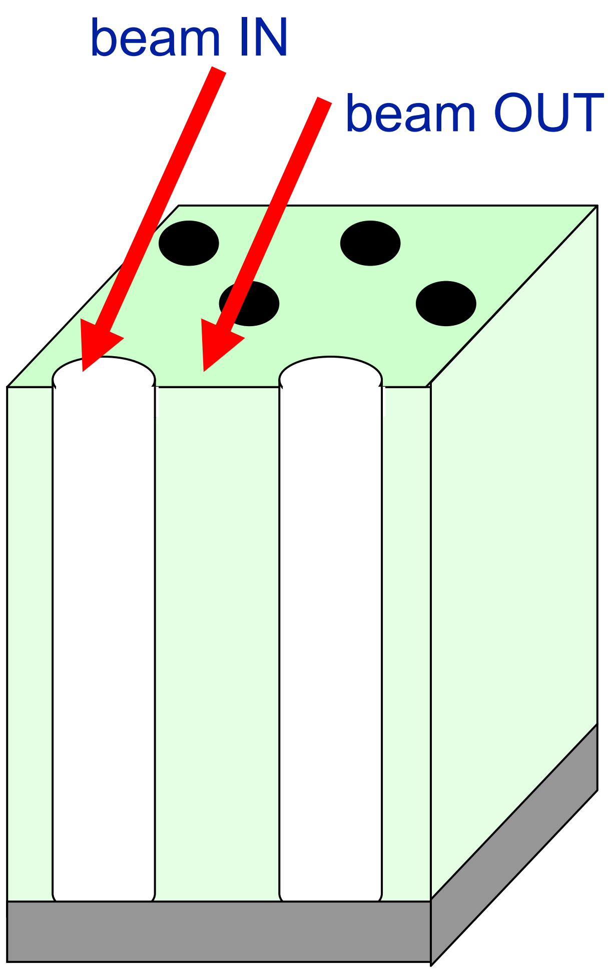
First proof of amplification mechanism !



Current amplification vs. beam current

15º tilt, 5 keV: 10 pA, 30 pA and 150 pA

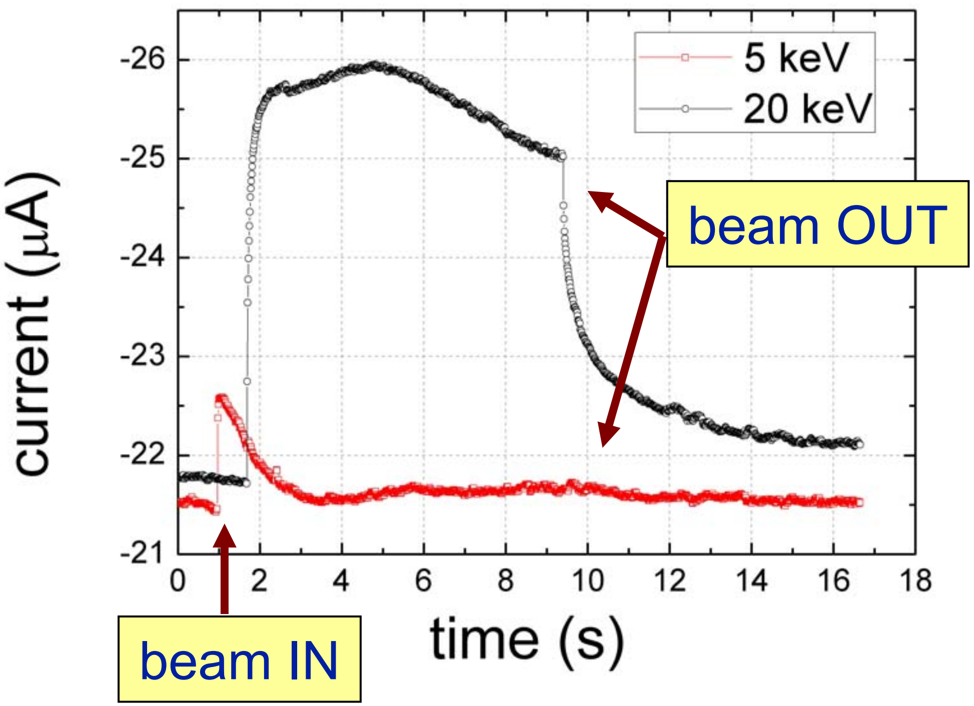


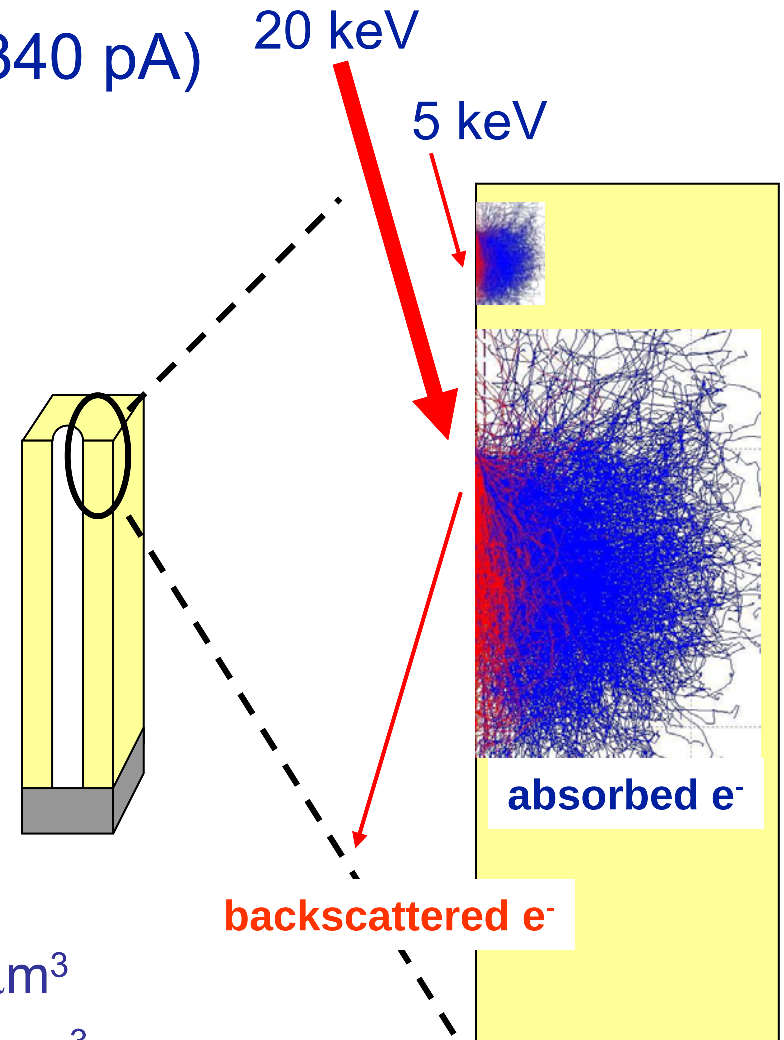


Further proof of amplification mechanism !

Current amplification vs. beam energy

15º tilt, 5 keV (150 pA) vs. 20 keV (340 pA)



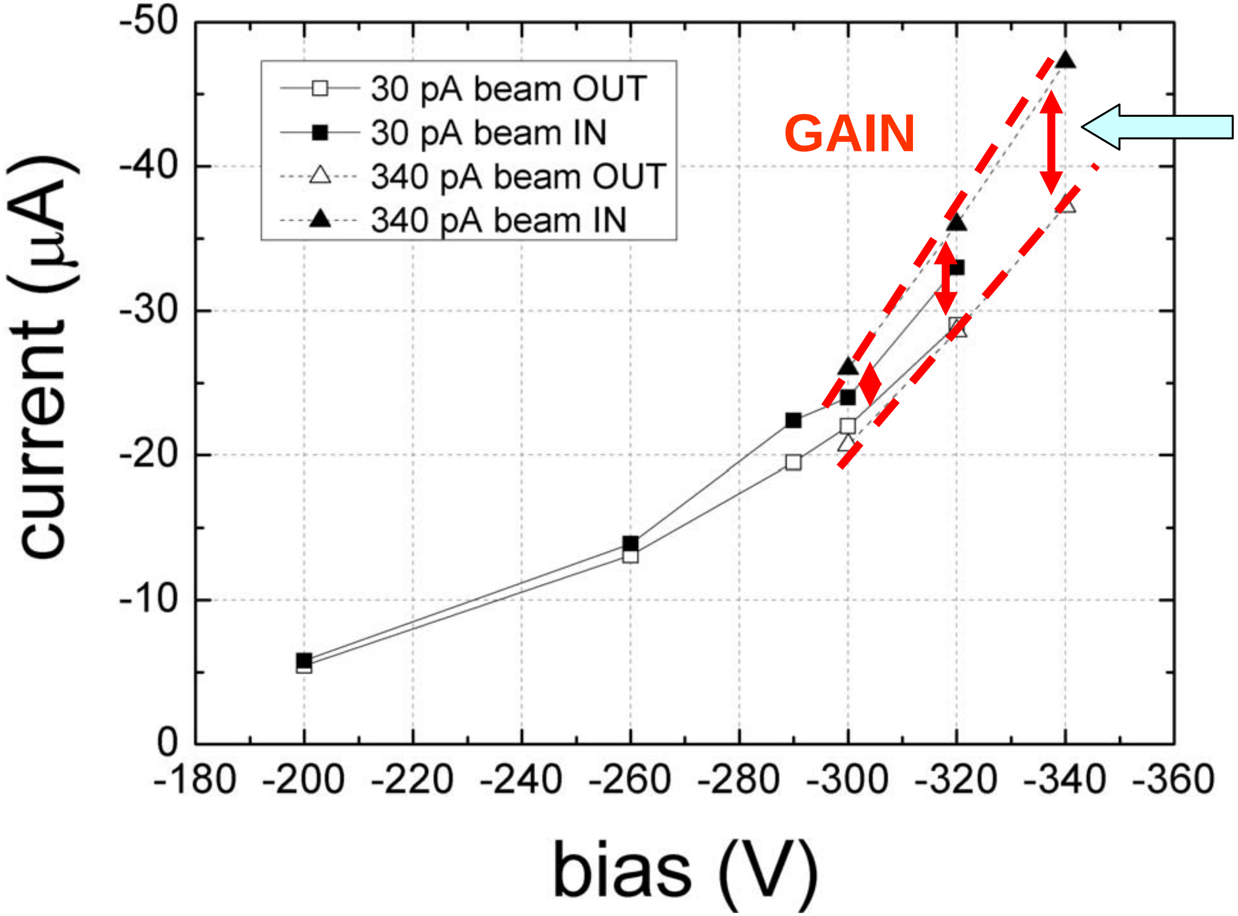


CASINO v2.42 simulations:

20 keV ≈ $2 \cdot 10^{12}$ e^-/h^+ s^{-1} within 50 μm^3

5 keV ≈ $2 \cdot 10^{11}$ e^-/h^+ s^{-1} within 0.03 μm^3

Current amplification vs. bias voltage



higher gain is expected at **higher bias voltage** and **pulse operation mode** !

Summary

1. First a-Si:H microchannel plates (AMCP) were realized, even though the fabrication process needs to be improved.

2. First proof of the amplification mechanism is given by using EBIC technique.

3. Gain needs to be confirmed by further tests at higher bias voltage and in pulse operation mode.

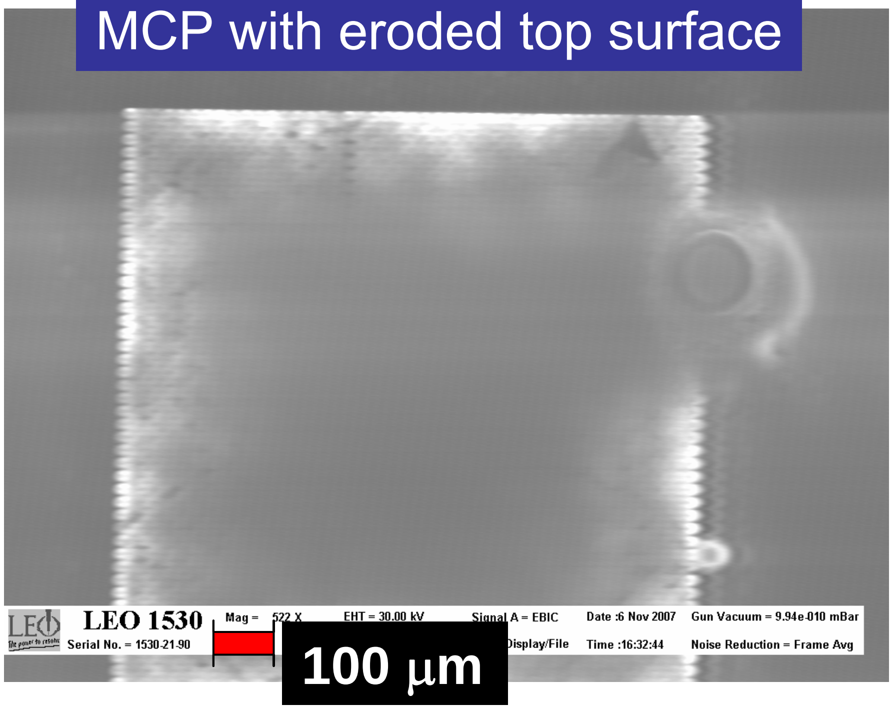
4. AMCP can be vertically integrated on top of an Application Specific Integrated Circuit as monolithic detector.

Thank you for your attention

EBIC maps: effect of top surface erosion

Erosion → loss of top contact integrity → uneven spread of bias voltage

MCP with eroded top surface



MCP with good quality top surface