COMPET- Characterization of a High Resolution and High Sensitivity Pre-Clinical PET Scanner with 3D Event Reconstruction

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COMPET - Facts

- 4-8cm bore opening (adjustable) with 8cm axial view
- very high sensitivity (16%)
- high resolution (sub-millimeter)
- 3D event reconstruction
- no inter module and inter crystal gap
- High data throughput FPGA/ethernet readout (~Mevents/sec)
- Backend computer farm for data taking and image reconstruction
- MRI compatibility
COMPET: POI Measurement Concept

Number of detector elements: 1080
Classical scanner with similar resolution and sensitivity: 20000 - 30000

See also AxPET (this session)
The AX-PET demonstrator—Design, construction and characterization
doi:10.1016/j.nima.2011.06.059
Readout Scheme

Analog preamplifier
Discriminator
Virtex 5
Readout FPGA
Virtex 5
Trigger FPGA
Embedded system
HV supply
Switch Network
Computer Farm

600 LYSO channels, 480 WLS
PreAmp

# channels: 10
# cards: ~150

70mm
FFC input

90mm

TOT  LVDS

LVDS output
Readout Scheme: FPGA

- **Fast Digitizer**
  - 1Gs sampling rate
  - Continuously sampling
  - No external trigger needed!

- **Parameterization Filter**
  - Extract time and amplitude information
  - TDC/QDC

- **Event Builder**
  - Incremented with each global coincidence
  - All events tagged with global event number

- **Ethernet**
  - 1Gb/s link
  - UDP data packets
Clock Distribution / Trigger / Reset

Trigger → Clock Out

Clock In, LVDS → Reset+Trigger bus, LVDS → Clock Out

Readout → Clock In, LVDS

Clock
Readout Software Design

- UDP receiver
- Raw Data memory (queue)
- Decoder and event sorter
- Event builder
- Event Data (HDF5/binary)
- Event analyser (find POI)
- POI Data (HDF5)
- Hit Data memory (queue)
- Control data display
- Slow data

Data flows:
- UDP receiver to Raw Data memory (queue)
- Raw Data memory (queue) to Decoder and event sorter
- Event builder to Hit Data memory (queue)
- Event analyser (find POI) to POI Data (HDF5)
- POI Data (HDF5) to Slow data

TCP connections:
- UDP receiver to Raw Data memory (queue)
- Slow data to Event analyser (find POI)
Readout Software Design

• 4 independent threads:
  – UDP receiver
  – Decoder: Decodes and sorts the hits to events
  – Event generator: build HDF5 tables consisting of the same event number
  – Event analyser: clusters the event data, finds corresponding WLS+LYSO data, finds the POI.

• Thread safety:
  – Mutexes/condition variables for access to queues (FIFOs) and slot memory.

• Maximal coincidence rate/computer with test pulser: 200 kcps
Trigger Scheme

• 2 Trigger to be implemented:
  – Synchronous trigger in real time through direct links: implemented, working
  
  – Asynchronous trigger through Ethernet (UDP/IP) 50% implemented
ETHERNET/UDP Trigger

Readout cards (x20)

Late running counter

Trigger FIFO

Send out data

Trigger 0 times

UDP

Issue trigger 1 times

Late running counter

UDP

Bottleneck: Network capacity, FIFO sizes

Good to scale, uses only standard network components
First Module Test Results: One Layer + Tagger

Setup:
10 LYSO crystals
12 WLS
Tagger
60MBq F-18 source

Tagger rate: 6.2 kcps
LYSO rate (10 channels): 1.3 Mcps
Trigger/readout rate: 500 cps
Assembly of the First Layer

- 12 WLS
- 10 LYSO
- Connected to COMPET readout
Intrinsic Spectra (LYSO)

Peaks at: 202keV, 303keV
Coincidence LYSO Spectra

Energy resolution (@511keV): 13% (FWHM), zero point calibration with intrinsic spectrum
Analysis

- For each hit in a LYSO crystal search for WLS hits.
- A WLS cluster consists of at least 2 adjacent WLS.
- Compute the center of gravity for the cluster with the largest integrated signal.
Cluster Size Distribution, E > 400 keV

[Bar chart showing the distribution of cluster sizes with E > 400 keV, with peaks around cluster sizes of 2 and 4.]
Results: Hit Map
Results: Hit Map

FWHM: 2.5 mm
~ source size
Source 2: Weak Na-22

FWHM: 1.8 mm
~ source size
Summary

• A high resolution + high sensitivity scanner is being implemented
• Readout scheme (ToT + FPGA-QDC + trigger + readout software) works.
  Bottleneck: Write speed to disk. Maximal rate/computer: 200kcps
• One half-layer assembled.
Backup: Simulations
Simulations: Setup

- Gate v5.0.0p01
- Readout based on hits
- List Mode output (ROOT)
- trigger condition:
  - **Total** deposed energy in 2 modules $> 450$ keV

Simulation of back-to-back gamma rays (511 keV) and $^{18}$F in water.
Detector Sensitivity Simulation

• Source for sensitivity simulations: back to back gammas (511 keV)
• 5 layers, 4 modules
• Diameter: 50 mm, Length: 72 mm
• 3D event reconstruction: 3 cases assumed:
Detector Sensitivity

All events (multiple scatters)

Single scatters

Photoelectric

06.07.2011

COMPET workshop Jan 2011

Michael Rissi, Universitetet i Oslo
Central Point Source Resolution

<table>
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<th>σ(DOI) [mm]</th>
<th>FWHM_x [mm]</th>
<th>FWHM_y [mm]</th>
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<tr>
<td>0.8</td>
<td>1.18</td>
<td>1.22</td>
</tr>
</tbody>
</table>

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