Development of EUV CMOS APS for EUI onboard Solar Orbiter

Talk outline

-I- Introduction / Motivation
-II- Introduction to EUI onboard Solar Orbiter
-III- EUV detector development activities:
- APSOLUTE: Si APS CMOS back illuminated
- BOLD: AlGaN hybrid imager back illuminated

-IV- Summary & Conclusion

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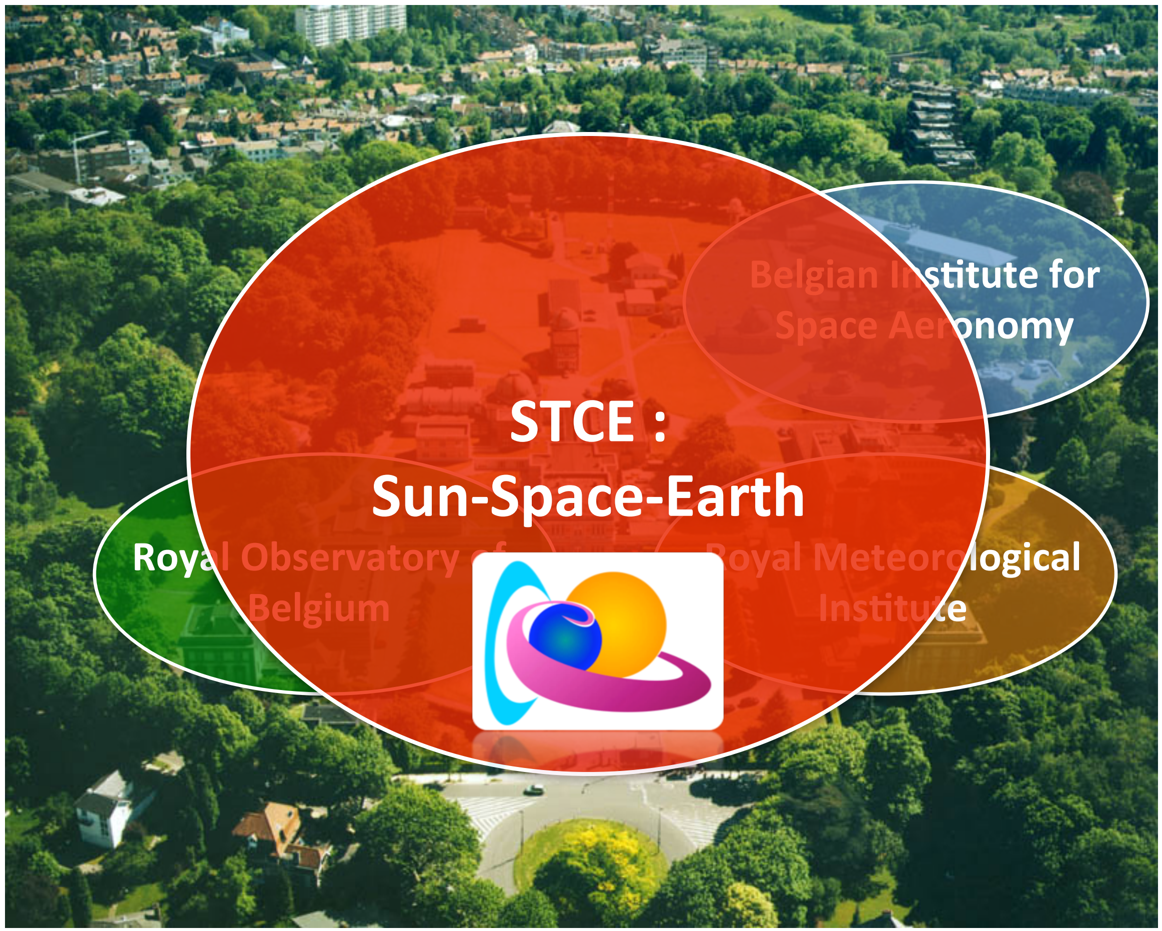
– 1 – Solar-Terrestrial Center of Excellence (STCE) – 2 – Royal Observatory of Belgium (ROB)

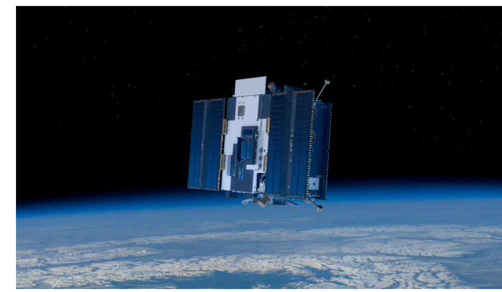
The Solar-Terrestrial Centre of Excellence (STCE)



Mission : Motivation

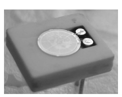
Development of advanced technologies components (to meet EUV Solar Physics requirements) :

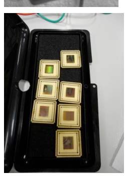
- Development of new challenging UV detectors (→ VUV radiometer),
- EUV APS CMOS imagers (→ EUV Telescopes),
- EUV optical Filters and UV Leds,
- Signal processing (incl. compression, JPEG2000 Virtex 5).

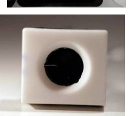


PROBA2, launched 2nd Nov 2009

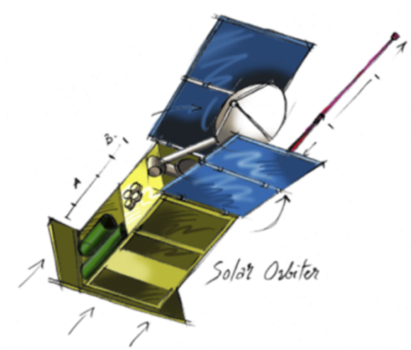
Past, present and future technological programmes :





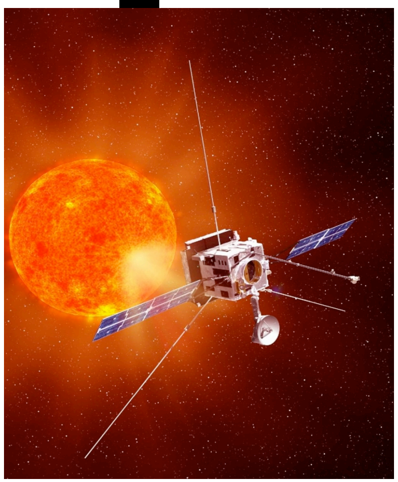


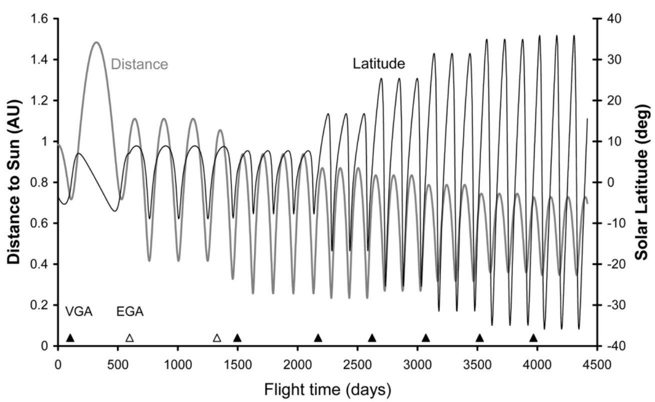
- LYRA : 12 solar radiometers (1st UV diamond detector in space),
- SWAP : Solar EUV telescope (1st EUV CMOS for solar physics),
- BOLD : R&T for EUV imaging sensor (specs, modelling, tests),
- EUI : Specification, testing, calibration, radiation of its imaging sensors,
- LYRA2 (Space Situational Awareness: cBN, AlN, AlGaN detectors).

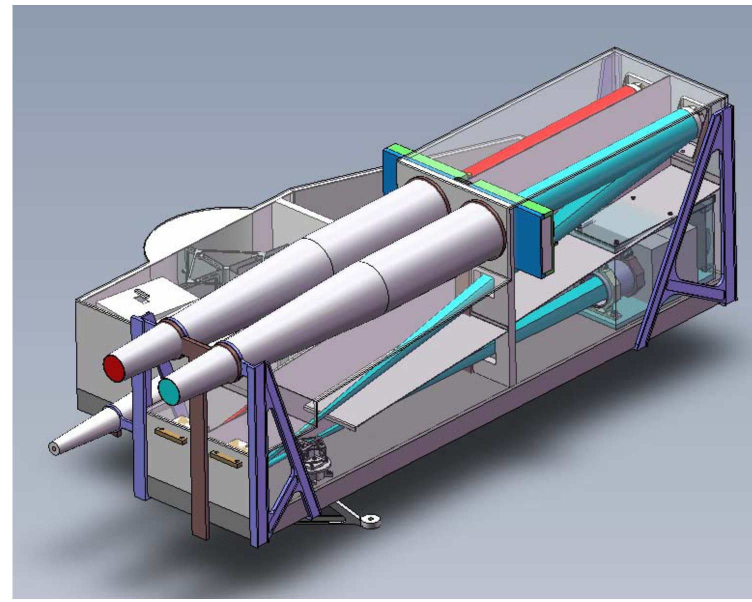


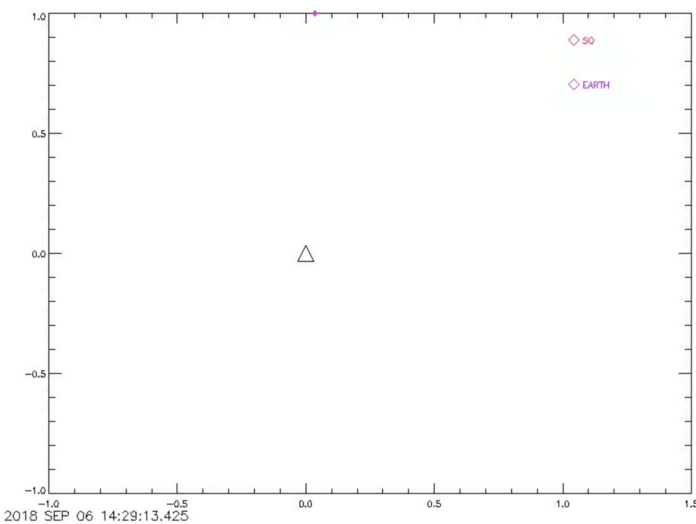
Solar Orbiter, to be launched 2017

Solar Orbiter and EUI









EUI : Extreme Ultraviolet Imager telescopes

- 2 HRI wavelengths: 17.4 nm, Ly-a (121.6nm)
- 1 FSI wavelengths : 17.4 and 30.4 nm (dual passband)

EUV detectors development activities

-1- APSOLUTE – Si CMOS APS

-2- BOLD – AlGaN 2D arrays

Consortium :

Prototype development: the APSOLUTE project

- **'APSOLUTE':** APS Optimized for Low-noise and Ultraviolet Tests and Experiments

  ➔ detector prototype developed and tested by end 2011 to confirm detector baseline and reach TRL5 qualification status (low noise and EUV sensitivity).
- **Partners:**
  - ROB/CSL : Specification + EUV radiometric characterization
  - CMOSIS : Design + Technology development
- **Requirements:**
  - Sensitivity: minimum 50% QE in 10nm < λ < 40 nm
  - Read noise: < 5e$^-$ RMS with a target of 1e$^-$ RMS after CDS with cool down to -40°C
  - Radiation hardness: > 70 krad (Si) with SEL and SEU tolerance, and operable after 1 Mrad (Si). High proton/neutron immunity.
  - Saturation (FWC): 80ke$^-$
  - On-chip functionalities: Random Access (RA),…
  - Vacuum compatibility and cleanliness,
  - Low power consumption (<500mW).

Prototype development: APSOLUTE

- **Concept:**

Two image sensors are designed:

- APSOLUTE64K: 256x256 sensor, containing 16 test pixel variants, organized in blocks of 64x64 pixels.
- APSOLUTE1M: 1024x1024 sensor, containing the “best guess pixel” variant.

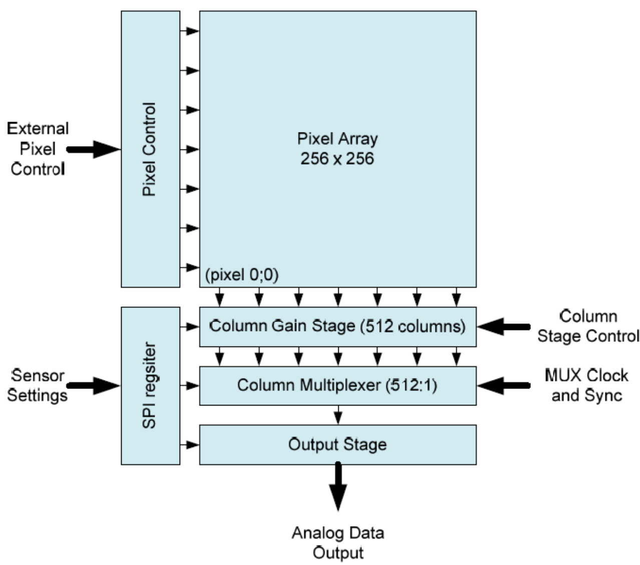


FIGURE 1 – APSOLUTE64K BLOCK DIAGRAM

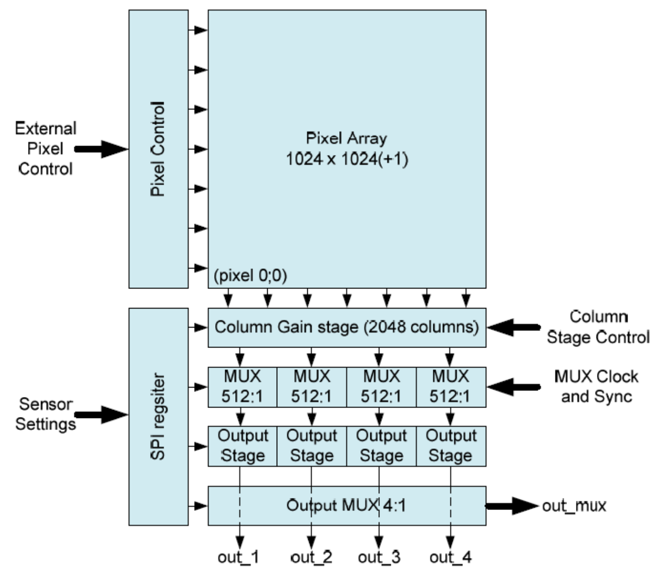
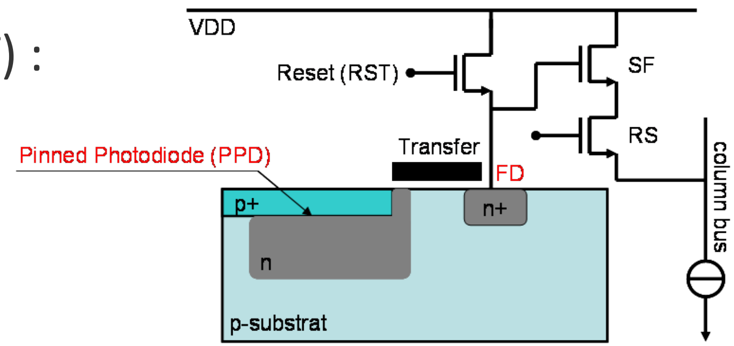


FIGURE 2 – APSOLUTE64K BLOCK DIAGRAM

Courtesy of CMOSIS

APSOLUTE: 1st front side prototypes

- Pixel design available (based on 4T) :



dualFD_5T **1**	dualFD_5T_TXv4 **2**	dualFD_5T_TXv5 **3**	dualFD_5T_SF **4**
dualFD_5T_TXv1 **5**	dualFD_5T_TXv2 **6**	dualFD_5T_TXv3 **7**	dualFD_7T **8**
dualTX_6T **9 (1MV2)**	dualTX_6T_TXv1 **10**	dualTX_6T_TXv2 **11**	dualTX_6T_TXv3 **12**
dualTX_8T **13 (1MV1)**	dualTX_8T_TXv1 **14**	dualTX_8T_TXv2 **15**	dualTX_8T_TXv3 **16**

#1-7 single SF, single TX

#8 double SF, single TX

#9-12 Single SF, double TX

#13-16 double SF, double TX

Remark:
- Pixel 8 not working
- Pixels 13 to 16 have a low FWC (<30ke-) and a noise level of ~8e-; too low dynamic range

Prototype development: APSOLUTE

- **Approach:**
  - Test chip (Monolithic) on SOI (SOITEC) material, 0.18μm technology (TS)
  - 10 μm pixel pitch pinned photodiode (PPD) based on 4T pixel design
  - Thinned for back-side illumination (EUV sensitivity)
  - Dual pixel read out

Backside thinning – SOI wafer

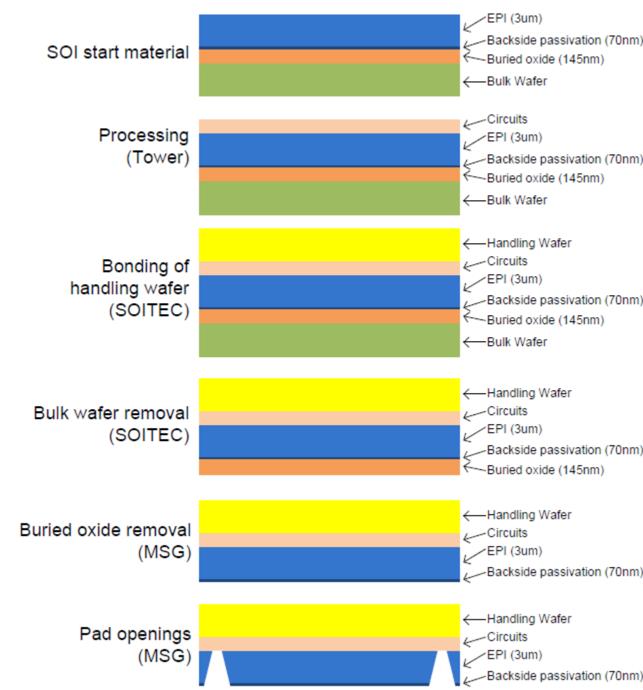


FIGURE 14 – PROCESS FROM STARTMATERIAL TO BACKSIDE THINNED WAFER

Noise and HDR : 2 columns gain amplifiers

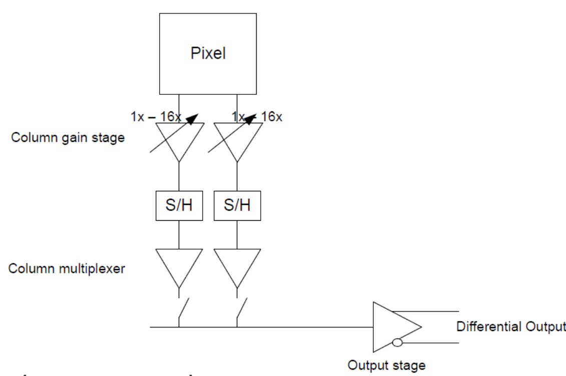


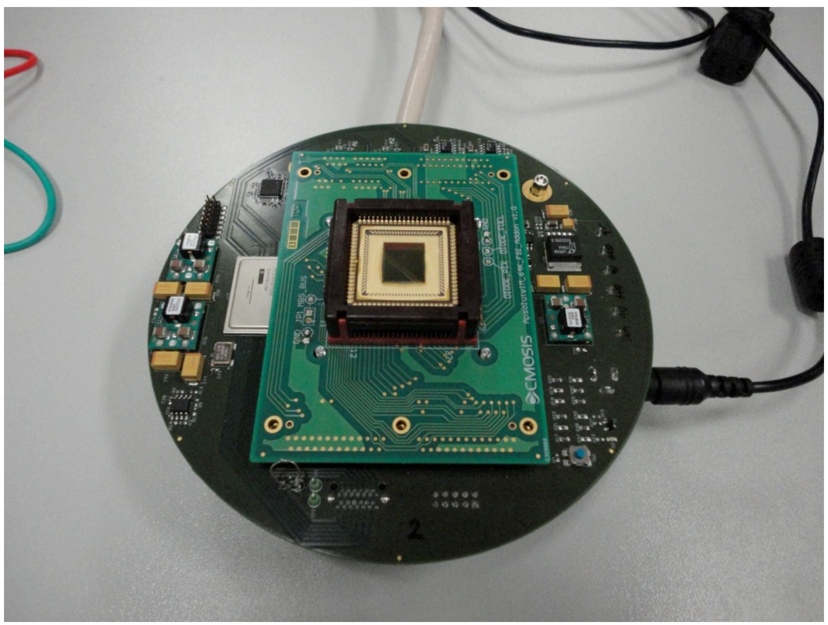
FIGURE 8 – ANALOG PATH ARCHITECTURE

- Programmable column gain path (1x up to 16x)
- Programmable output gain (1x; 2x; 4x)

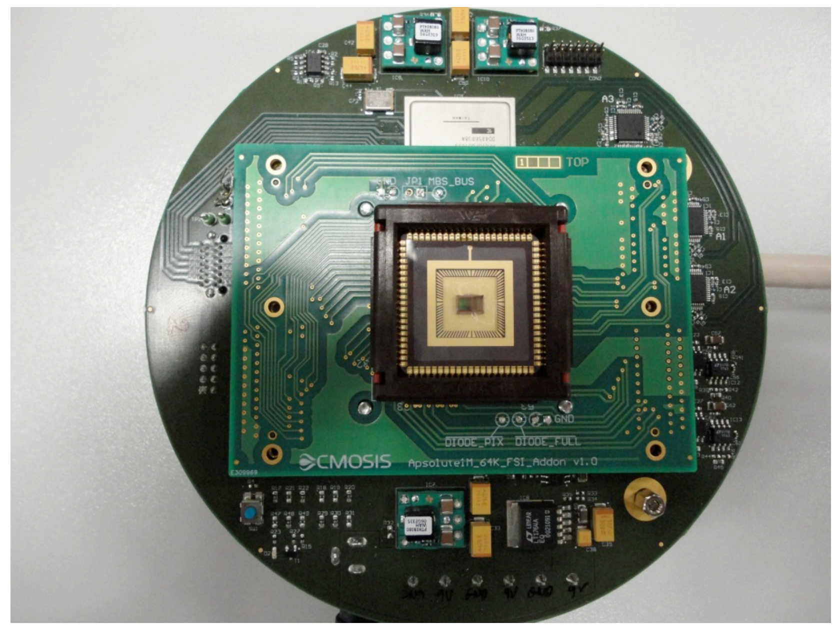
Courtesy of CMOSIS

APSOLUTE: 1st front side prototypes

- 256x256 and 1kx1K imagers (Si, 10 µm pitch)
- 16 pixels variants, 2 gains path per pixel (HG; LG)

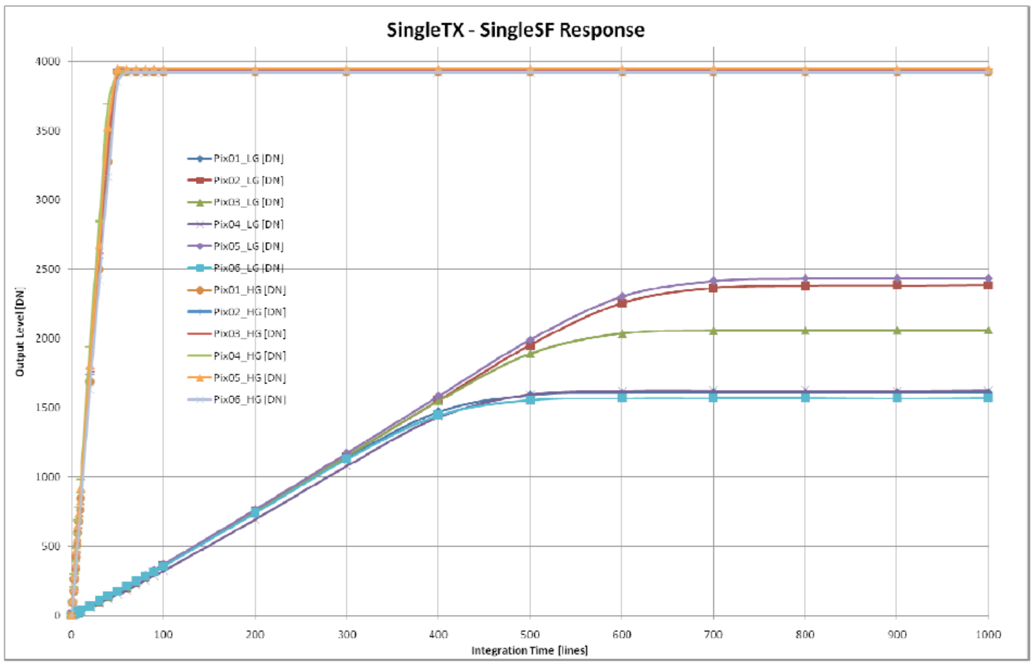


1kx1k



256x256

APSOLUTE: Dual gain operation (#1→#6)



Linear at low light level

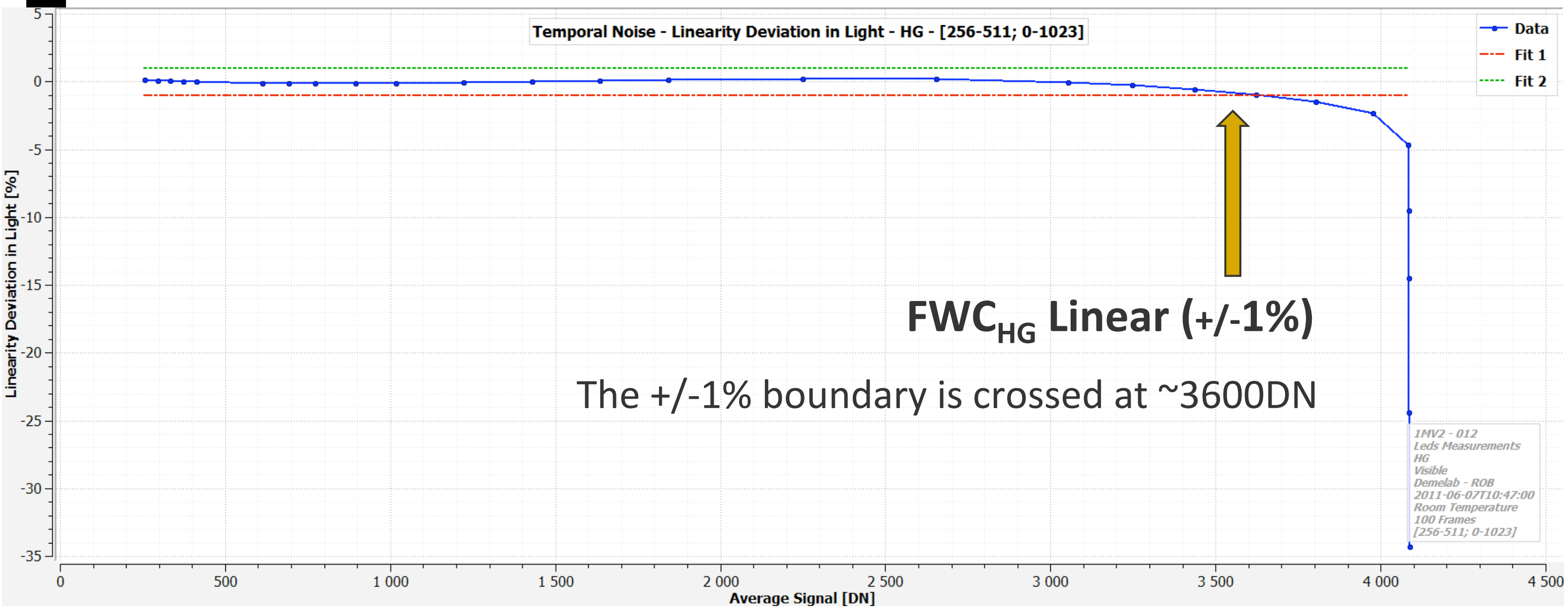
<u>Example:</u>
Pixel #1-6 same photodiode size (# TX shape, size)
- #1 and 4 normal TX low FWC
- #6 larger normal TX low FWC
- #5 smaller normal TX high FWC

- #2-3 U shape TX
(3 has larger U shape TX → lower FWC)

- High Gain Columns set to 3.25x gain
- Low Gain Columns set to 1.13x gain

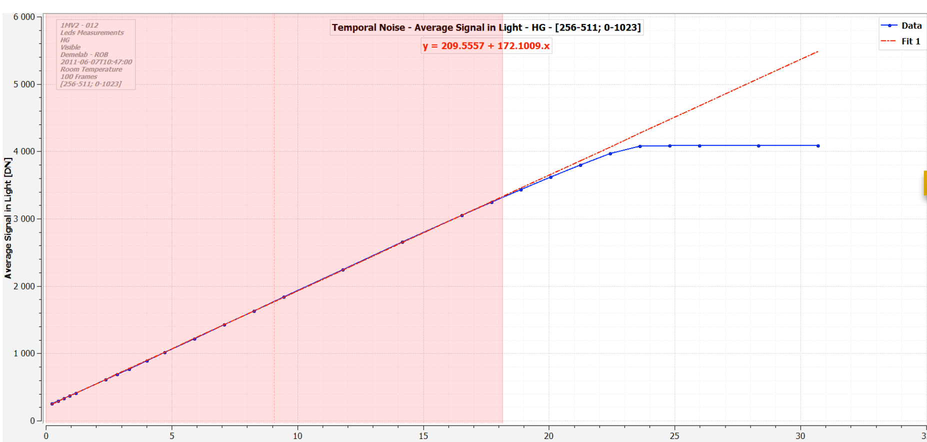
Courtesy of CMOSIS

First results: Linearity error vs Signal output



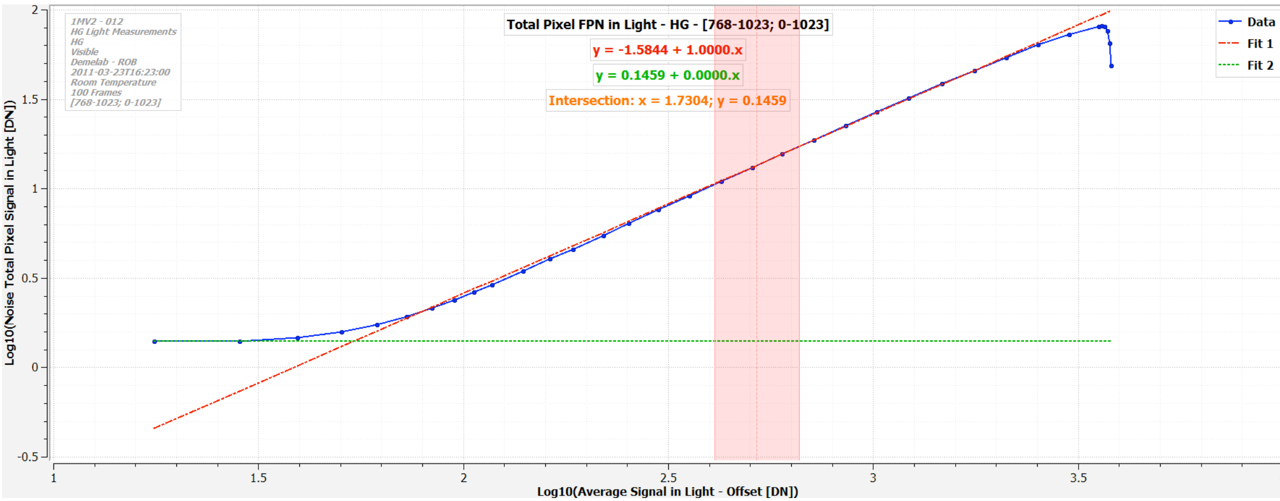
FWC_{HG} Linear (+/-1%)

The +/-1% boundary is crossed at ~3600DN

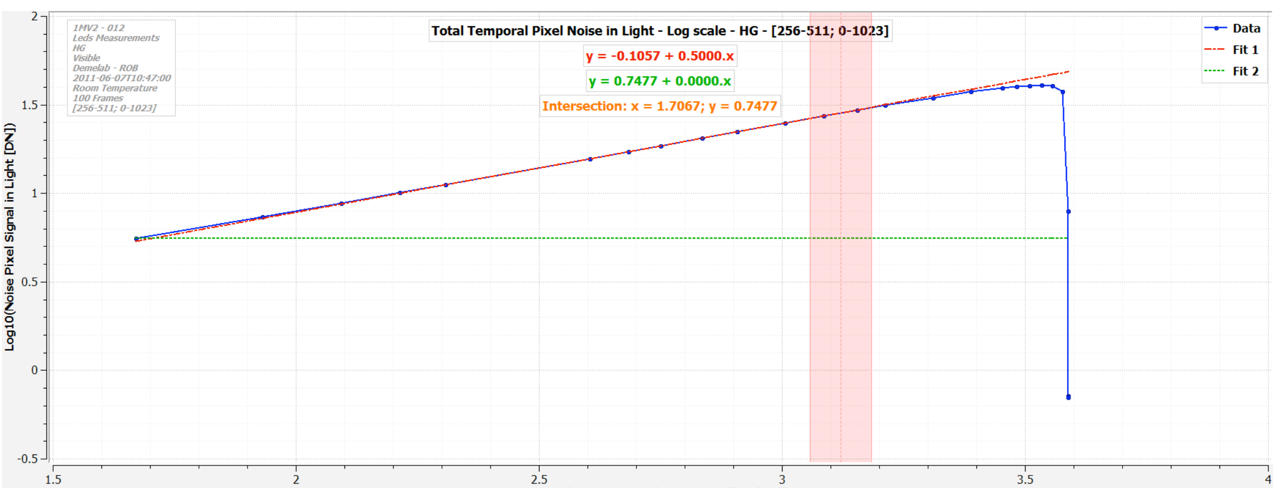


For single TX, single SF variants:
- #2 and 3 behave the most linear

FPN (DSNU, PRNU, offset pixel) & PTC



→ Column, row, pixel offset

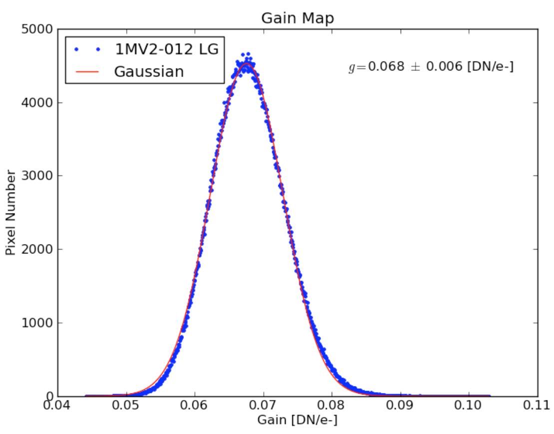


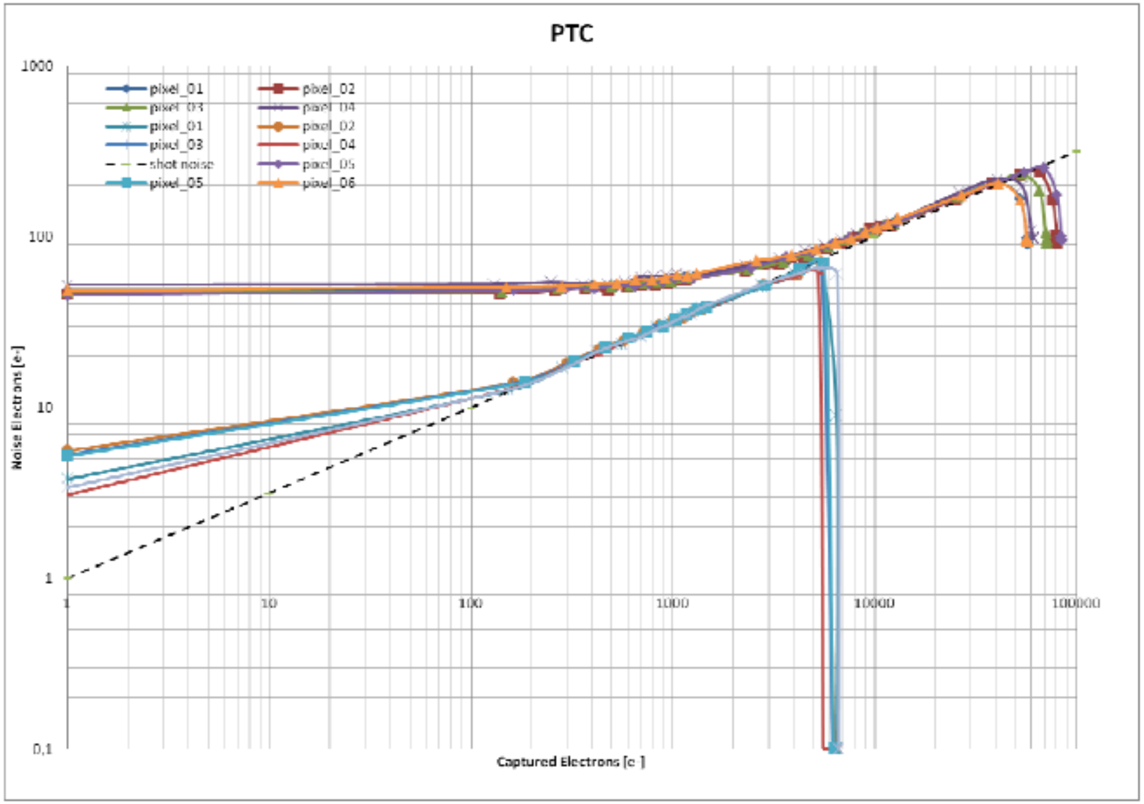
Photon Transfer Curve (PTC) for HG and LG

APSOLUTE: 1st results (256x256)

Photon Transfer Curve : PTC

Conversion gain map





Single TX, Single SF (pixels #01-06)

High gain → 5 ke-

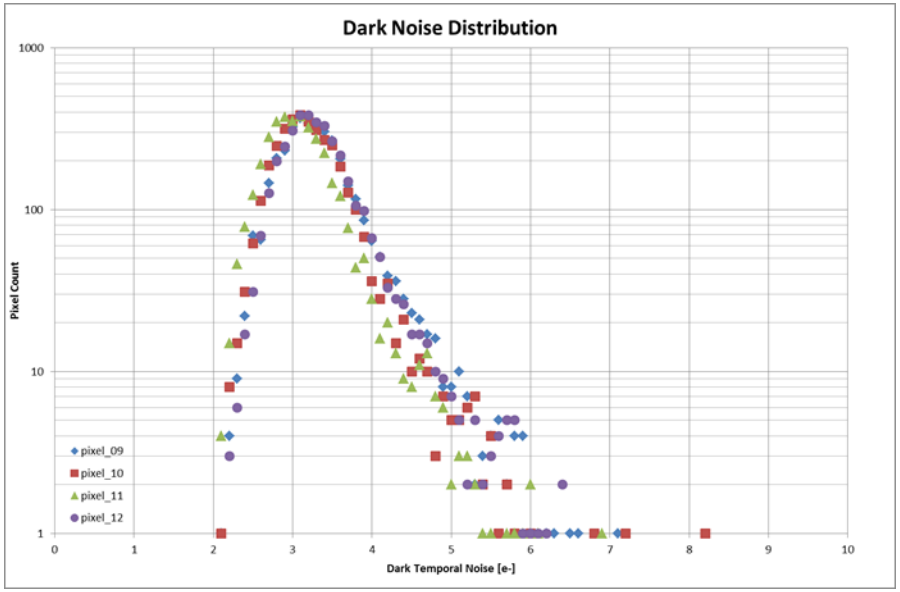
Low gain →5 to 60-99ke-

Courtesy of CMOSIS

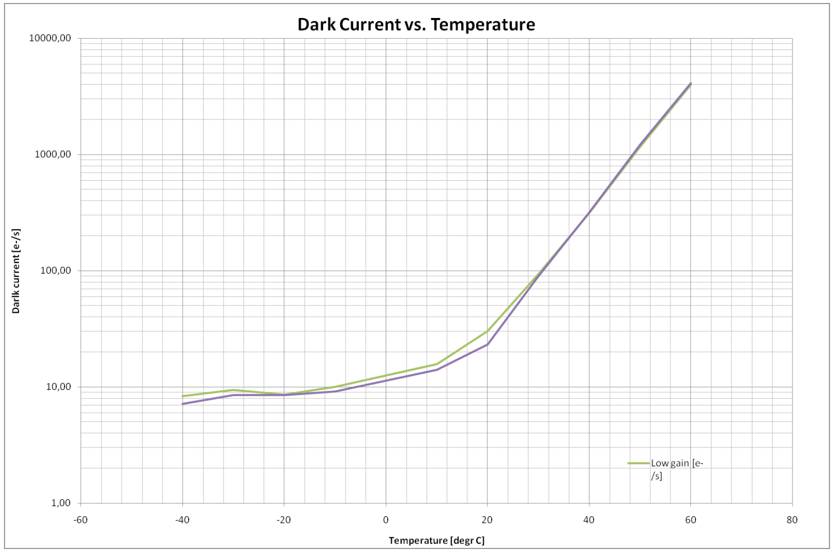
Dark signal and noise distribution

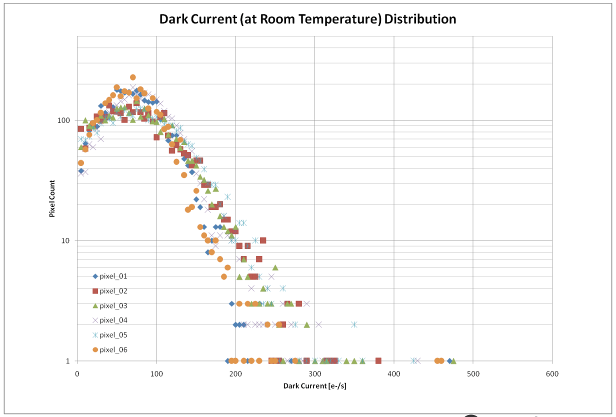
Dark current vs T° (-40°,+60°C)

Dark noise distribution



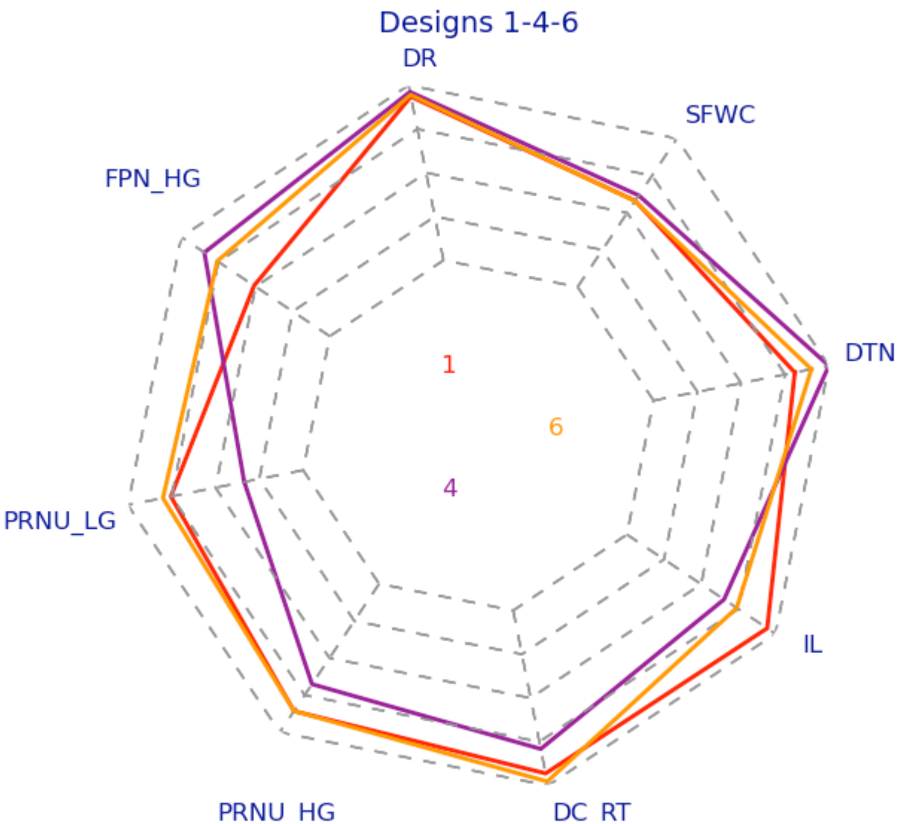
Dual TX, Single SF
(pixels 09-12)

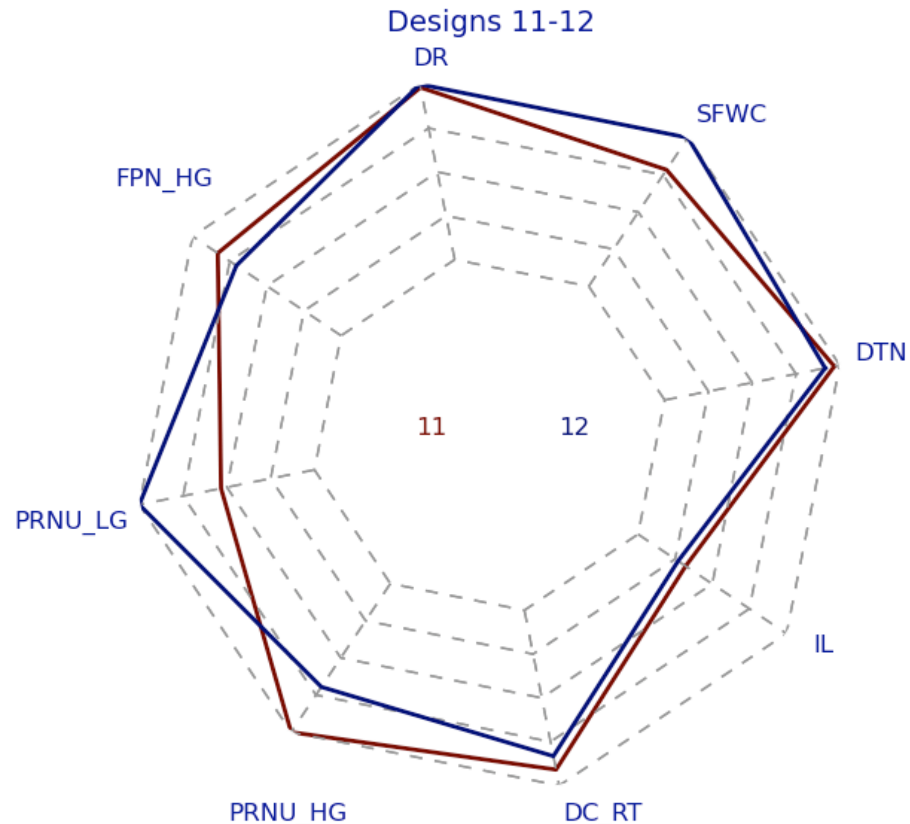




Courtesy of CMOSIS

APSOLUTE: 1st results (#1 to #12)

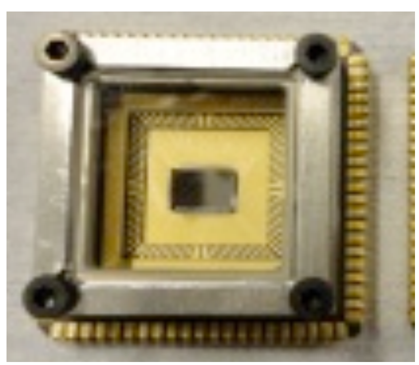




→ To define the best criteria for the selection of the FM pixel design

From Front side to Back side illumination

- SOI Wafer processing & thinning finished
  Steps:
  - Buried Oxide Removal (+ removal of 250nm and 400nm Si → (E)UV QE improvement
  - Backside Implant: TBD if required (to reduce the dark current)
  - Pad Opening
  - Packaging
- Packaged BSI devices



Backside thinning – SOI wafer

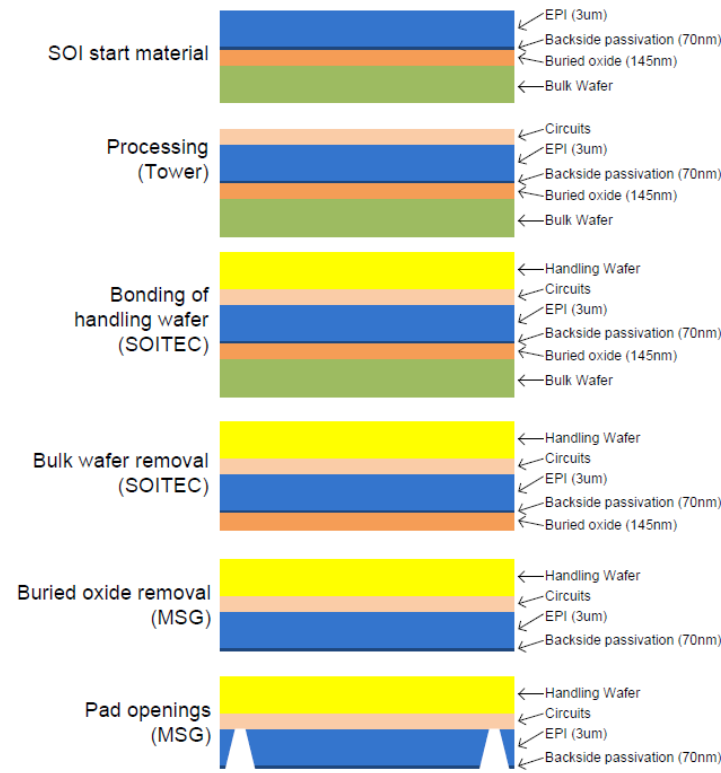
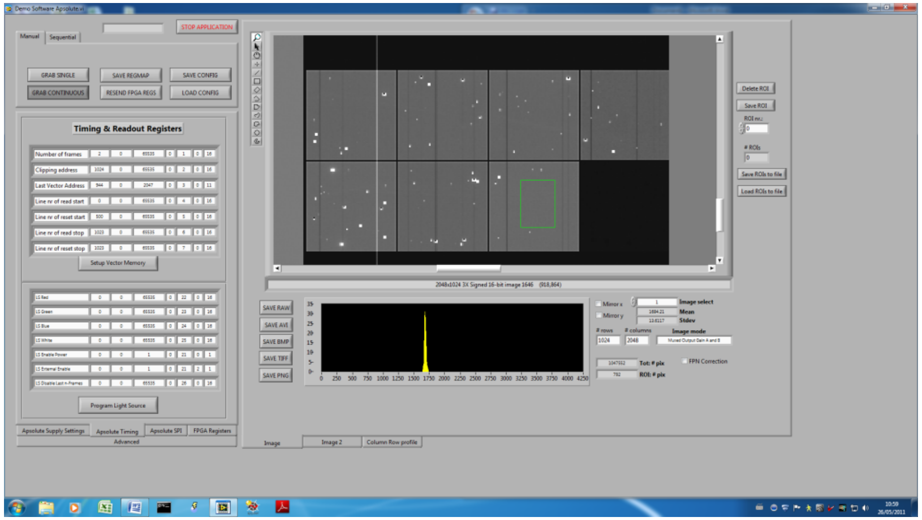
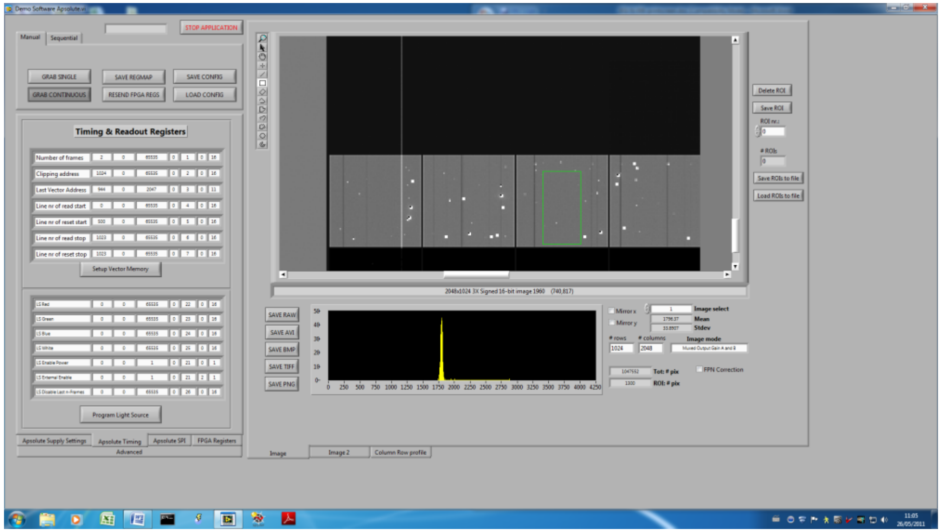


FIGURE 14 – PROCESS FROM STARTMATERIAL TO BACKSIDE THINNED WAFER

BSI: Functional tests





#1-7 (visible light)

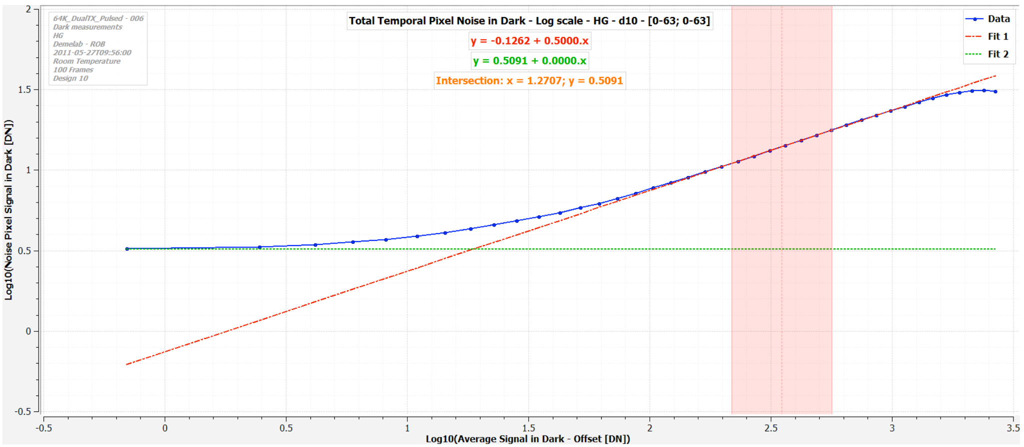
#9-12 (visible light)

Contamination issues with the BSI
→ Dead and Hot pixels (clusters)
→ Bad columns (under investigations)

Data under processing (photoresponse and MTF incl.):
→ difficult to estimate all parameters (e.g. PRNU and DSNU)
→ Windowing is needed (within the 64x64)

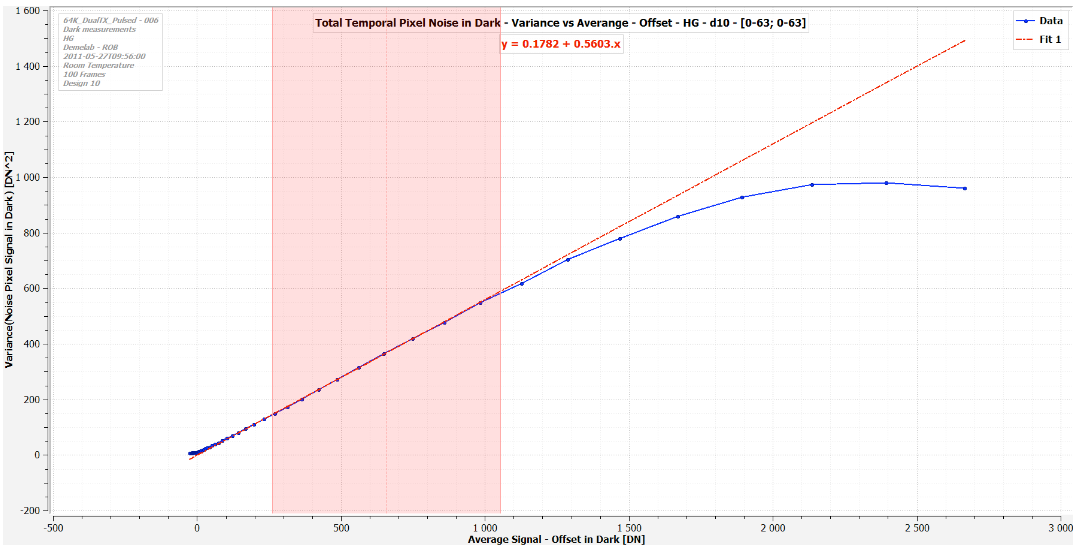
dualFD_5T 1	dualFD_5T_TXv4 2	dualFD_5T_TXv5 3	dualFD_5T_SF 4
dualFD_5T_TXv1 5	dualFD_5T_TXv2 6	dualFD_5T_TXv3 7	dualFD_7T 8
dualTX_6T 9 (1MV2)	dualTX_6T_TXv1 10	dualTX_6T_TXv2 11	dualTX_6T_TXv3 12
dualTX_8T 13 (1MV1)	dualTX_8T_TXv1 14	dualTX_8T_TXv2 15	dualTX_8T_TXv3 16

BSI: performance tests (1st results)

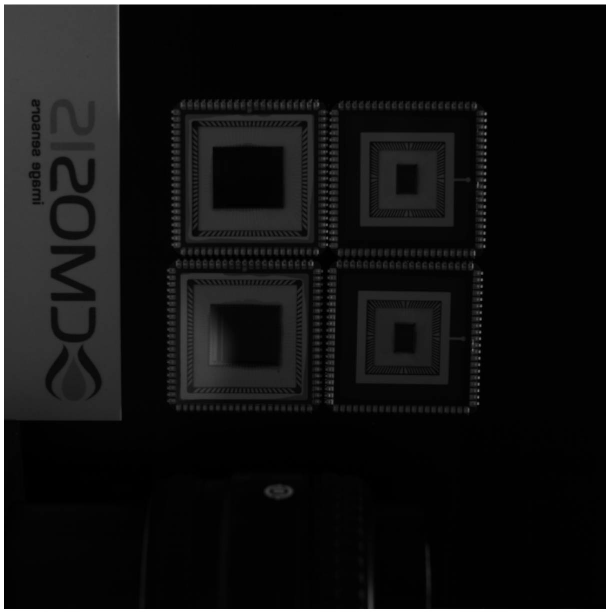


FPN (DSNU, PRNU, offset pixel)

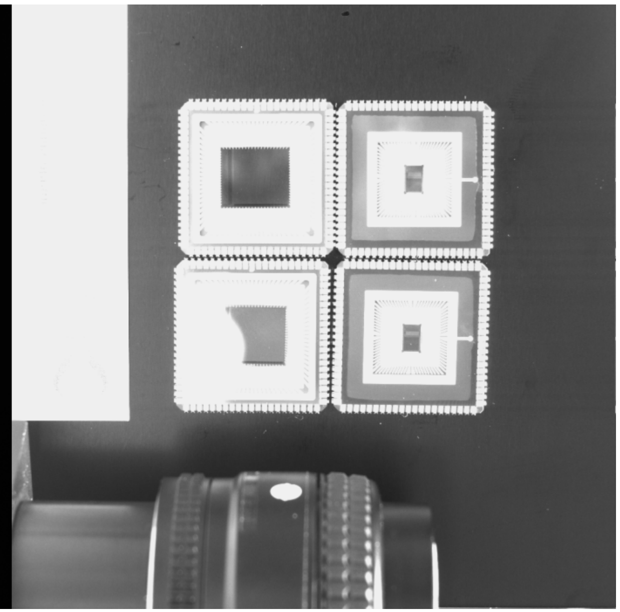
Conversion gain, RN (variance method)



APSOLUTE: 1MV2 (LG, HG)



Low gain



High gain

DR = 85.5dB

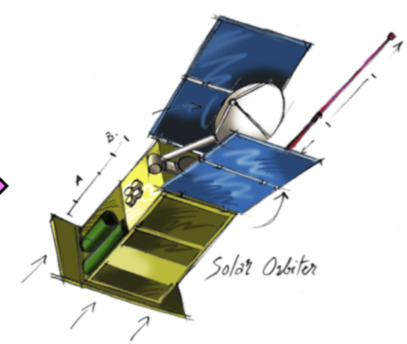
Reconstruction / normalization

High gain → 5 ke-
Low gain → 62.5 ke-

EUV detectors development activities

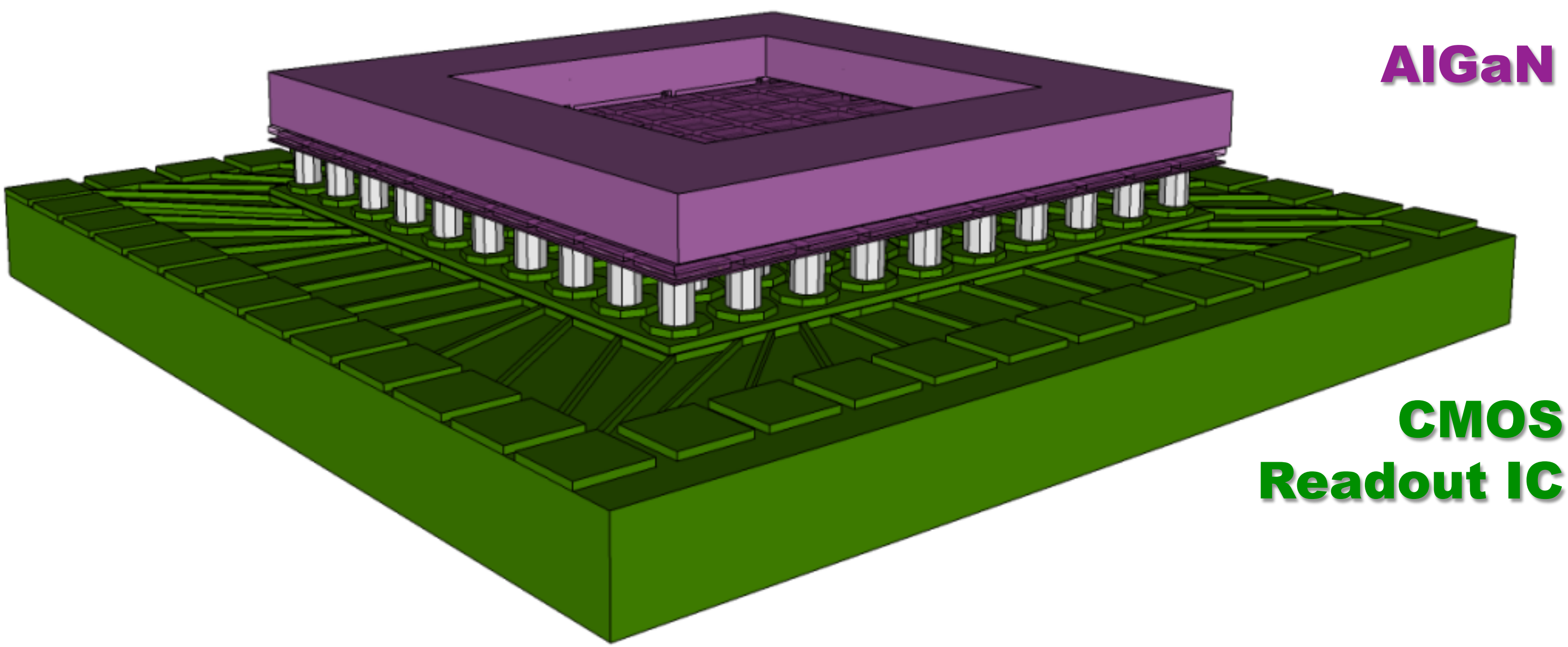
-1- APSOLUTE – Si CMOS APS

-2- BOLD – AlGaN 2D arrays **(courtesy of P. Malinowski)**



Device Concept

- BOLD : Blind to the Optical Light Detector
- Hybrid design: AlGaN array integrated with Si ROIC using flip-chip bonding with the In bumps (10µm pixel pitch)
- Back illuminated (removal of Si substrate not transparent in UV)
- Si frame left around the active area for mechanical stability



Introduction to AlGaN

Single Pixel Detectors

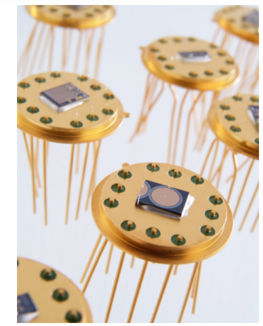
Integration and Imagers

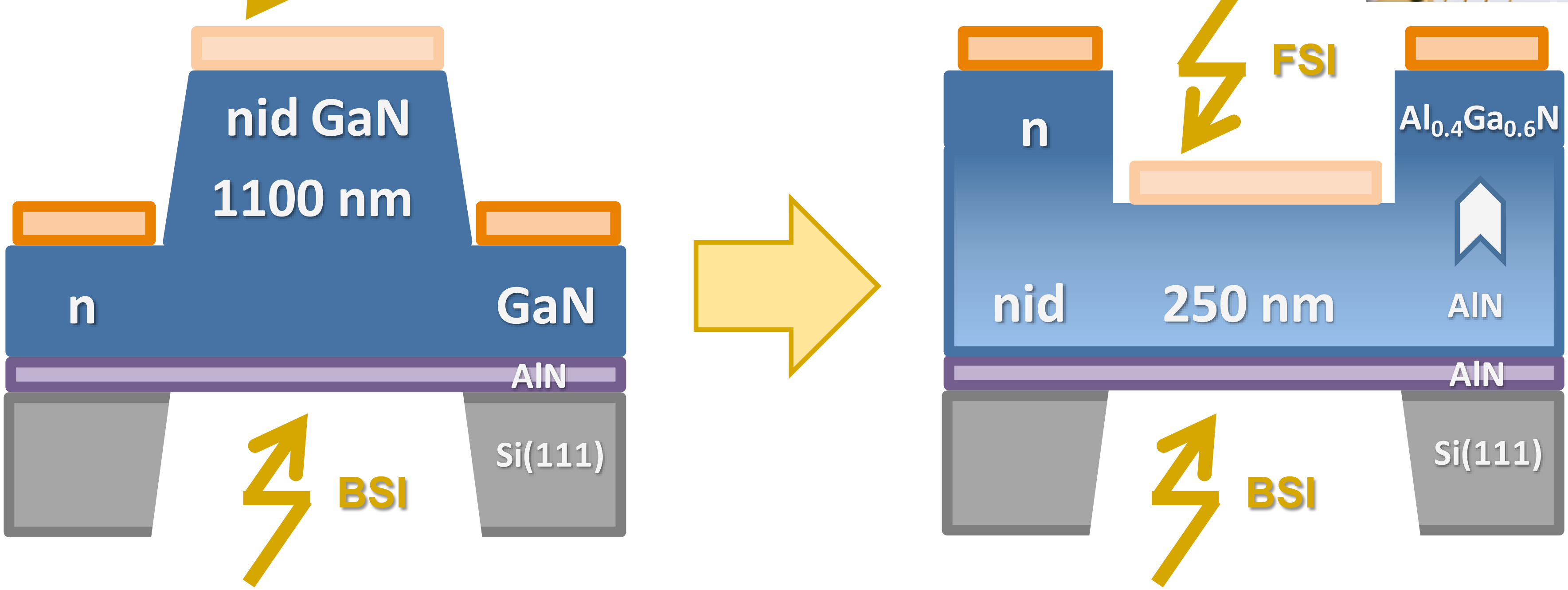
Results in UV and EUV

Summary and Conclusions

LAYER STACK IMPROVEMENT

- optimization of the active layer for the EUV and BSI



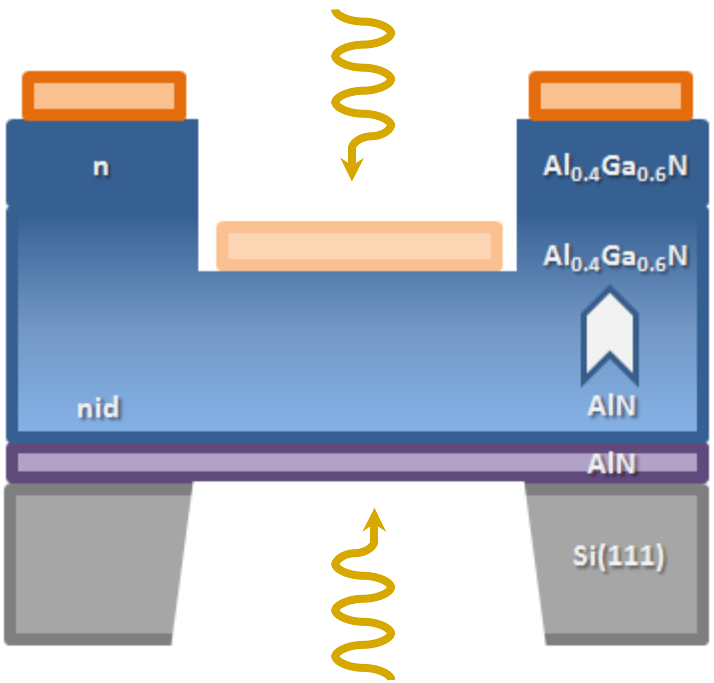


GaN active layer
standard Schottky

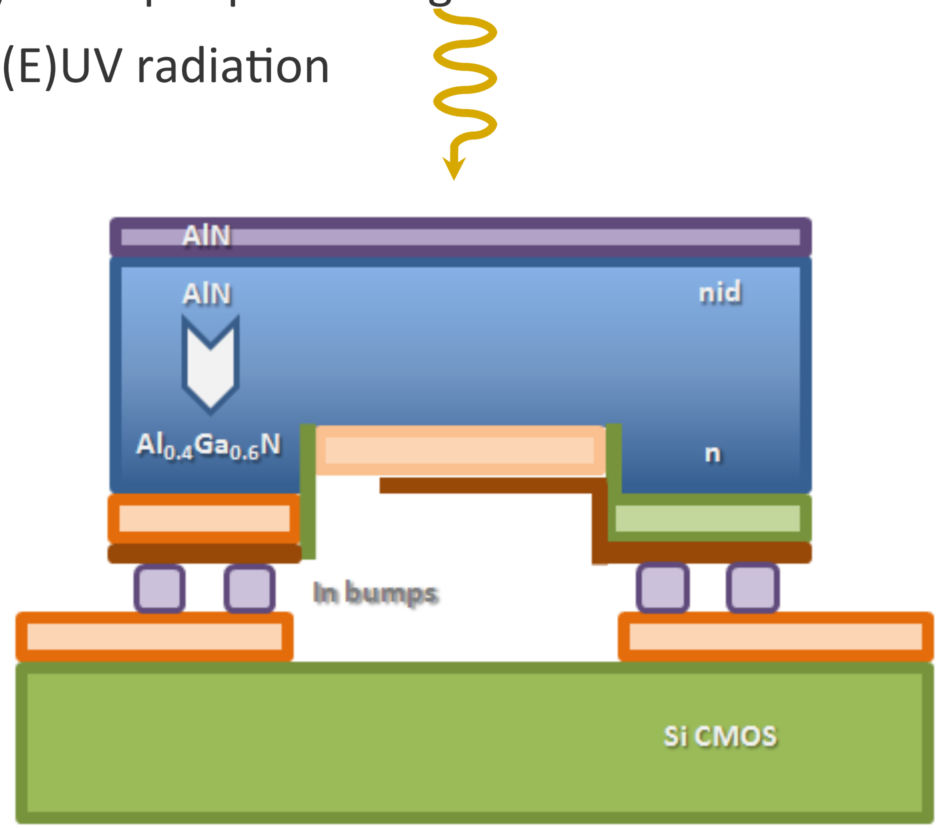
gradient AlGaN active layer
inverted Schottky

Backside Illumination

- Backside illumination necessary in 10 µm pitch imagers
- Si removal necessary to detect (E)UV radiation



local Si substrate removal



Si removal after integration

Introduction to AlGaN

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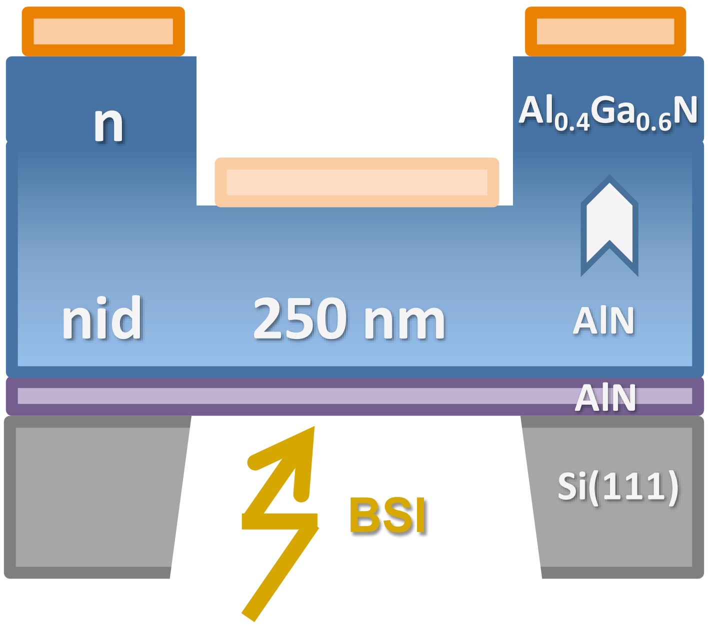
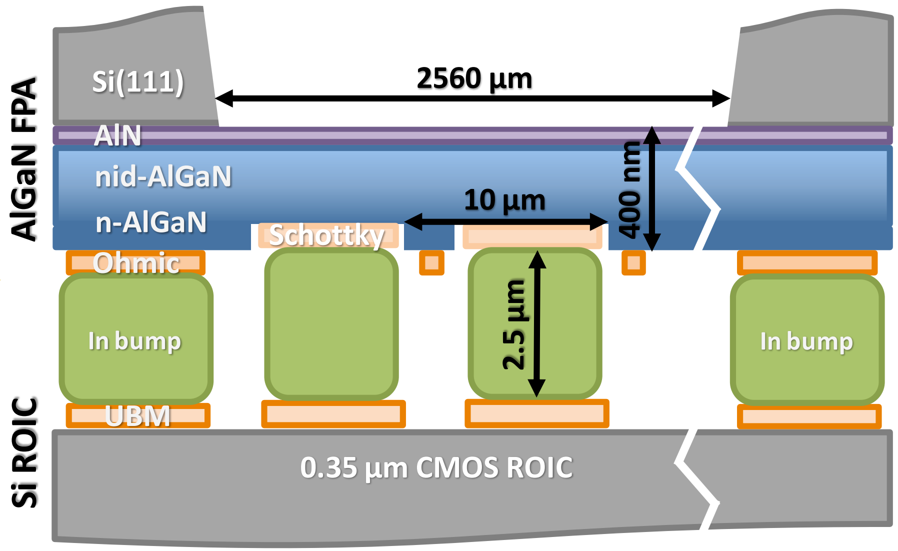
Summary and Conclusions

From Diodes To Imagers

- process transfer from single devices to the high density arrays
- wafers post-processed with In bump arrays
- samples integrated with the CMOS ROICs

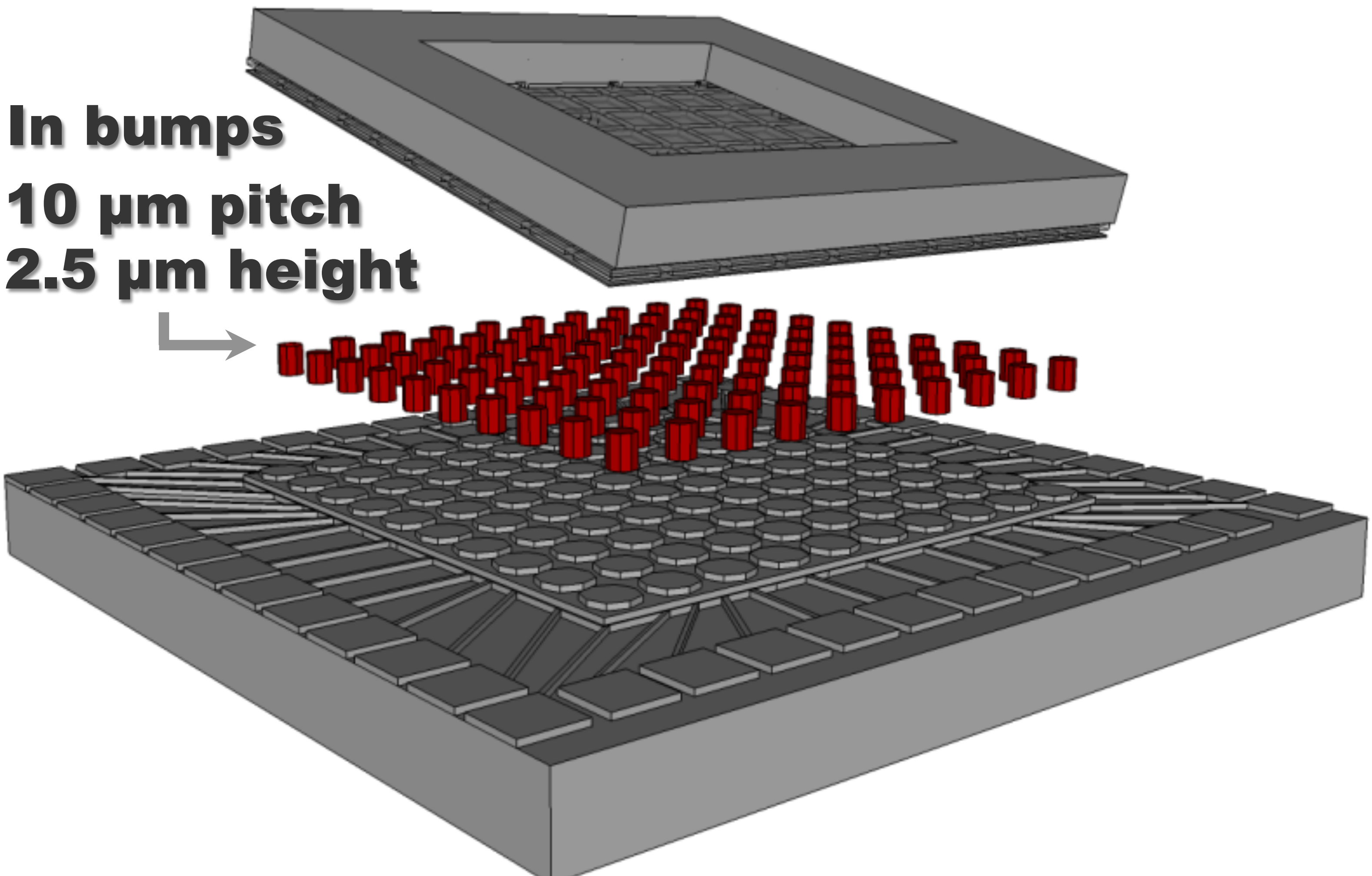


single pixel diode



imager after integration

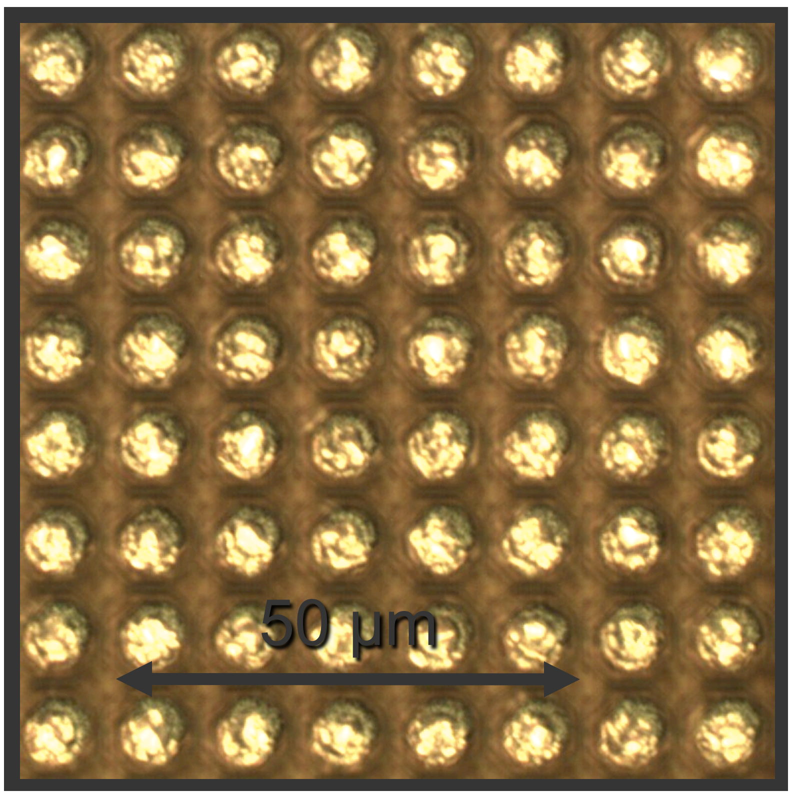
Interconnect processing

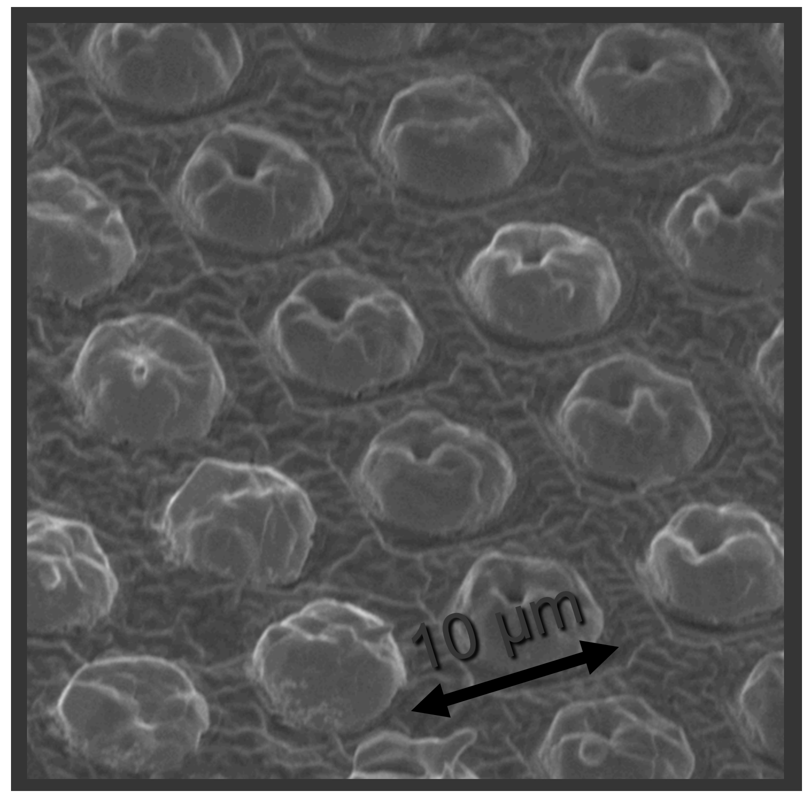


Interconnect processing

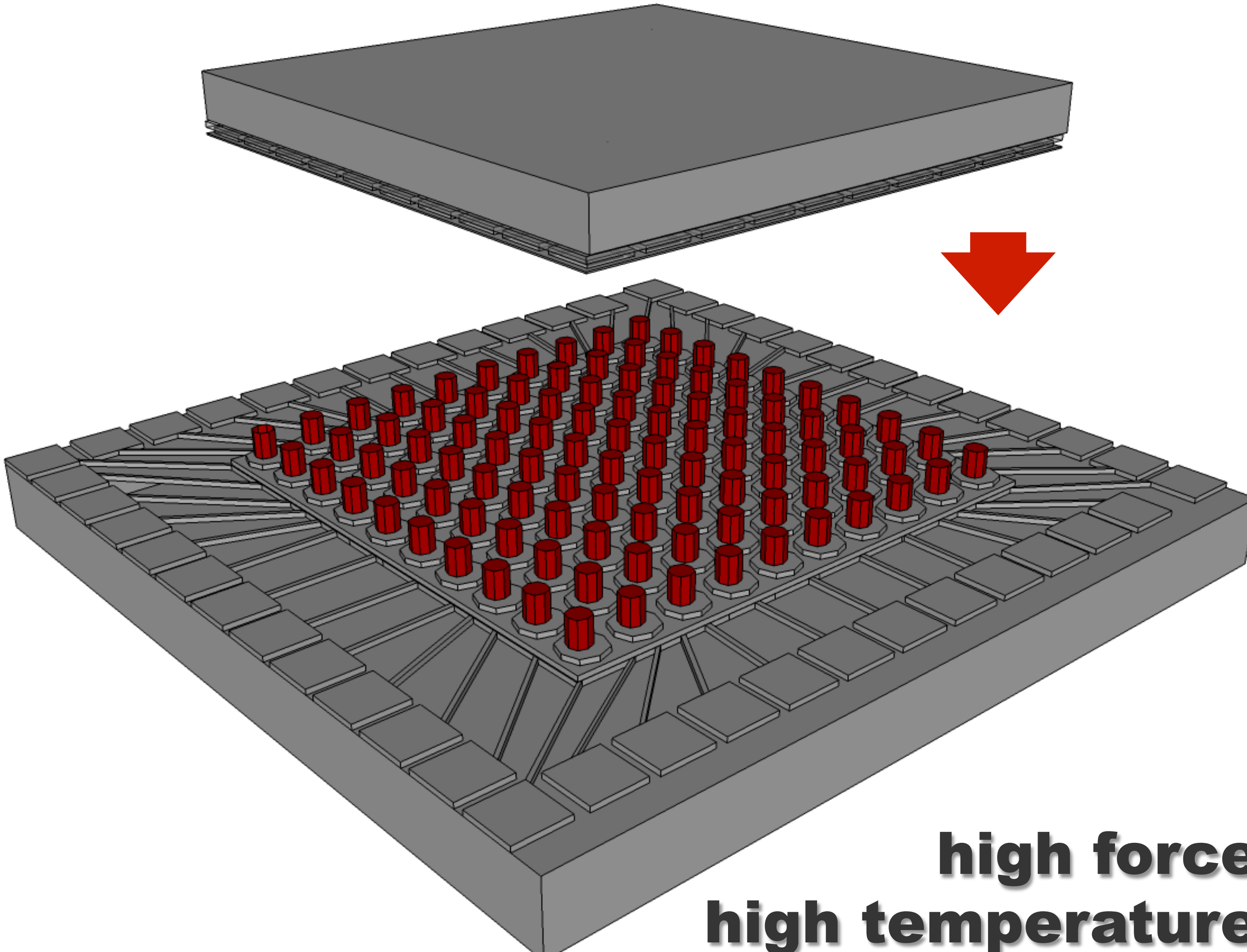
In bump deposited on each pixel

- evaporation of 2.5 µm In and lift-off
- additional bumps for mechanical stability



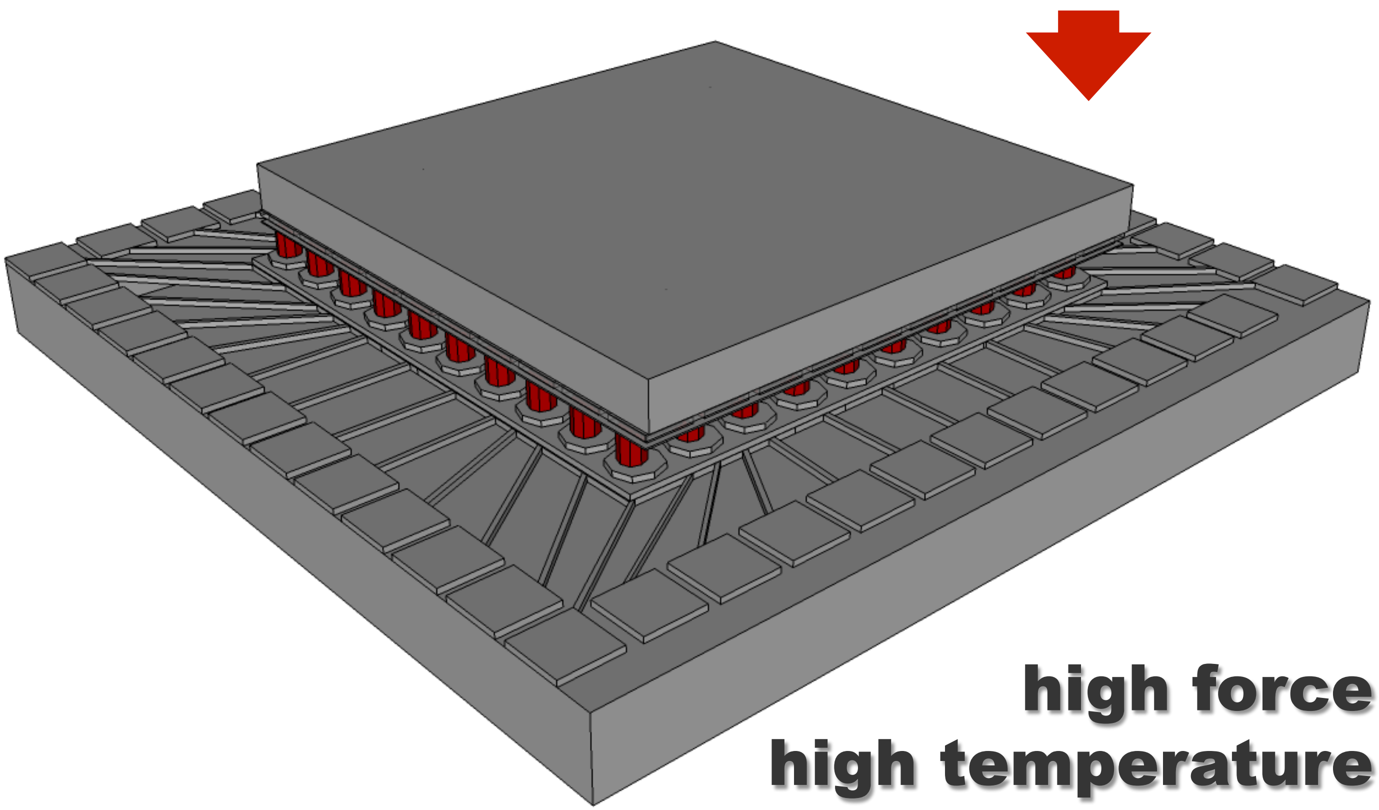


Flip-chip bonding



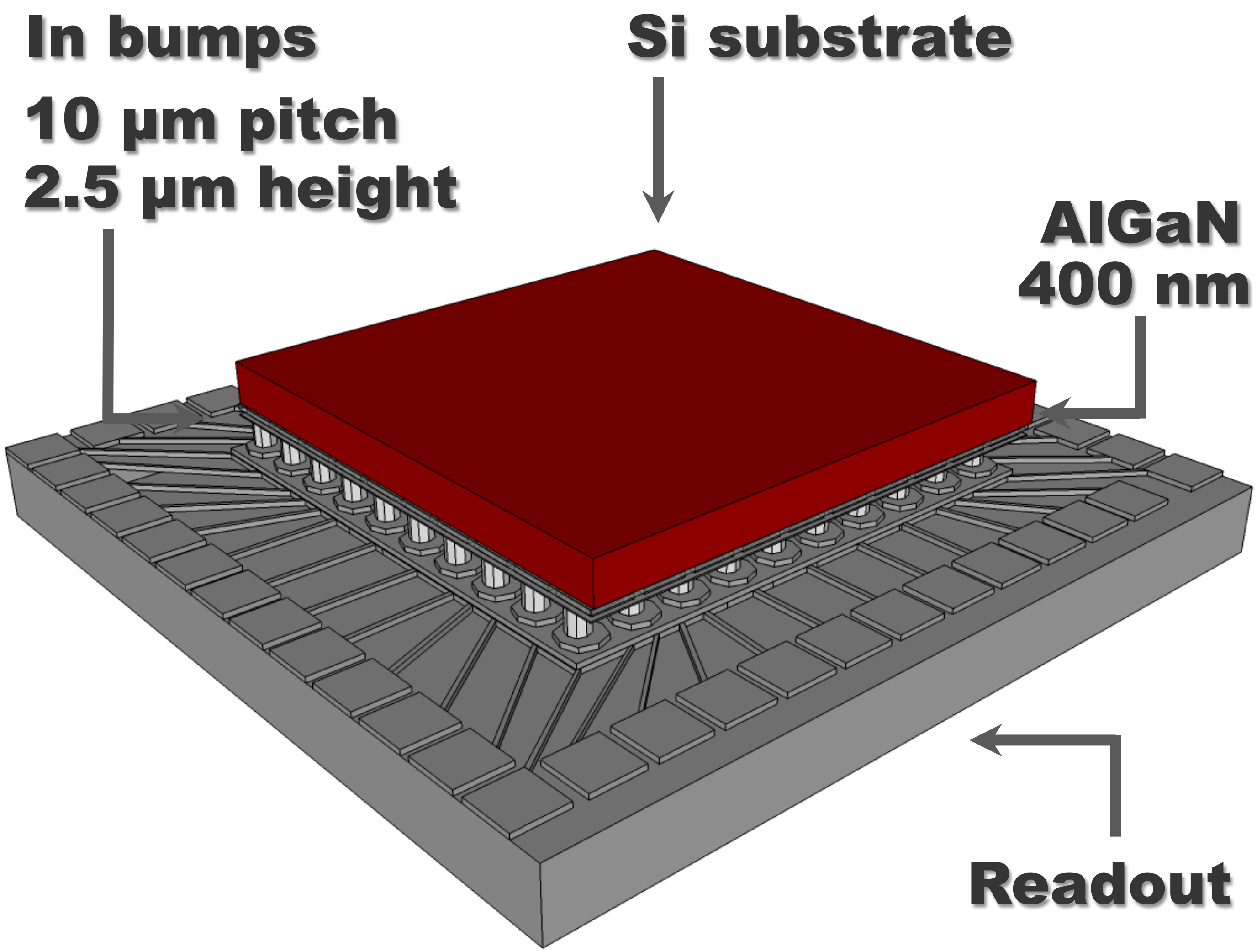
high force
high temperature

Flip-chip bonding

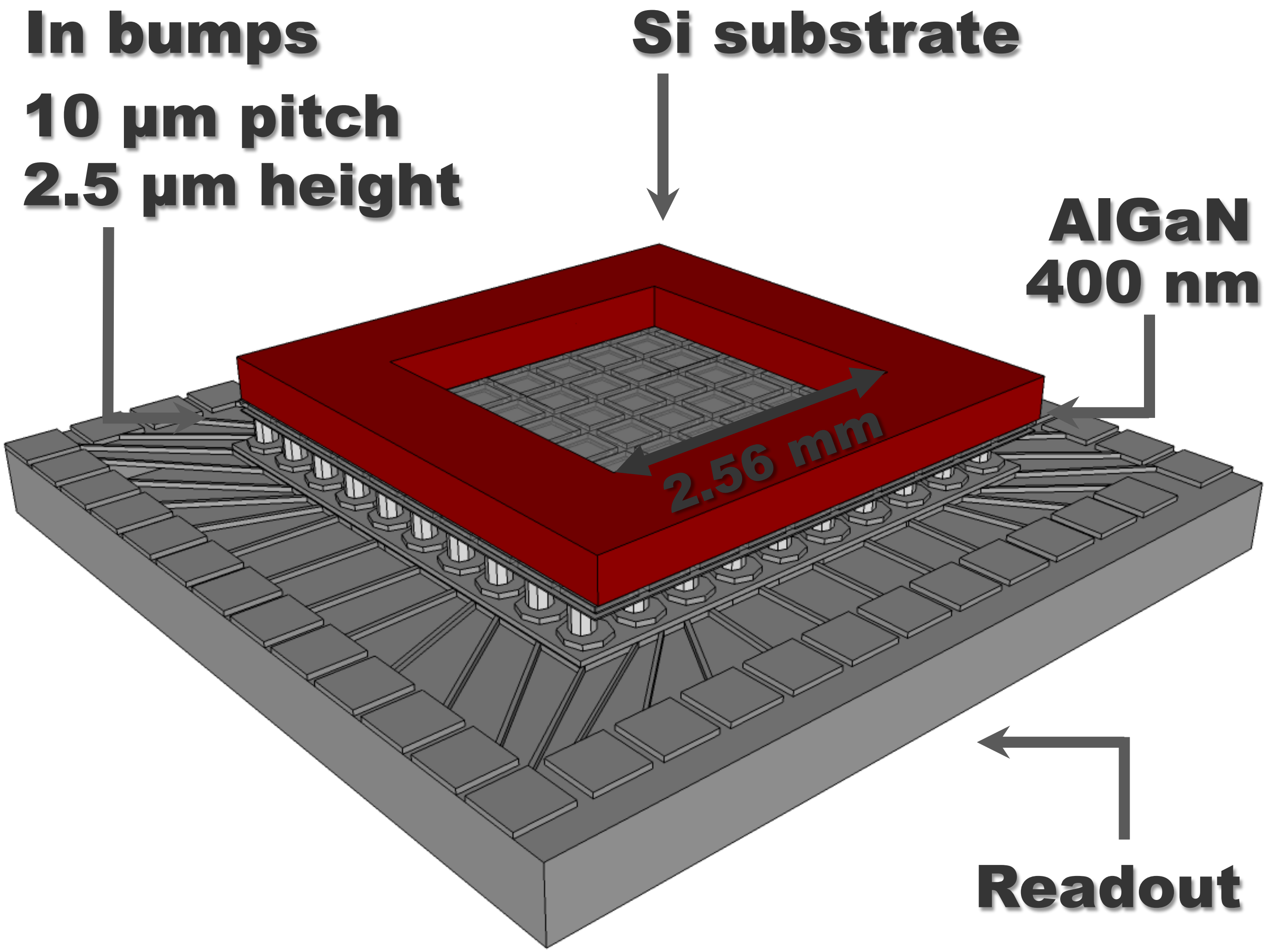


high force
high temperature

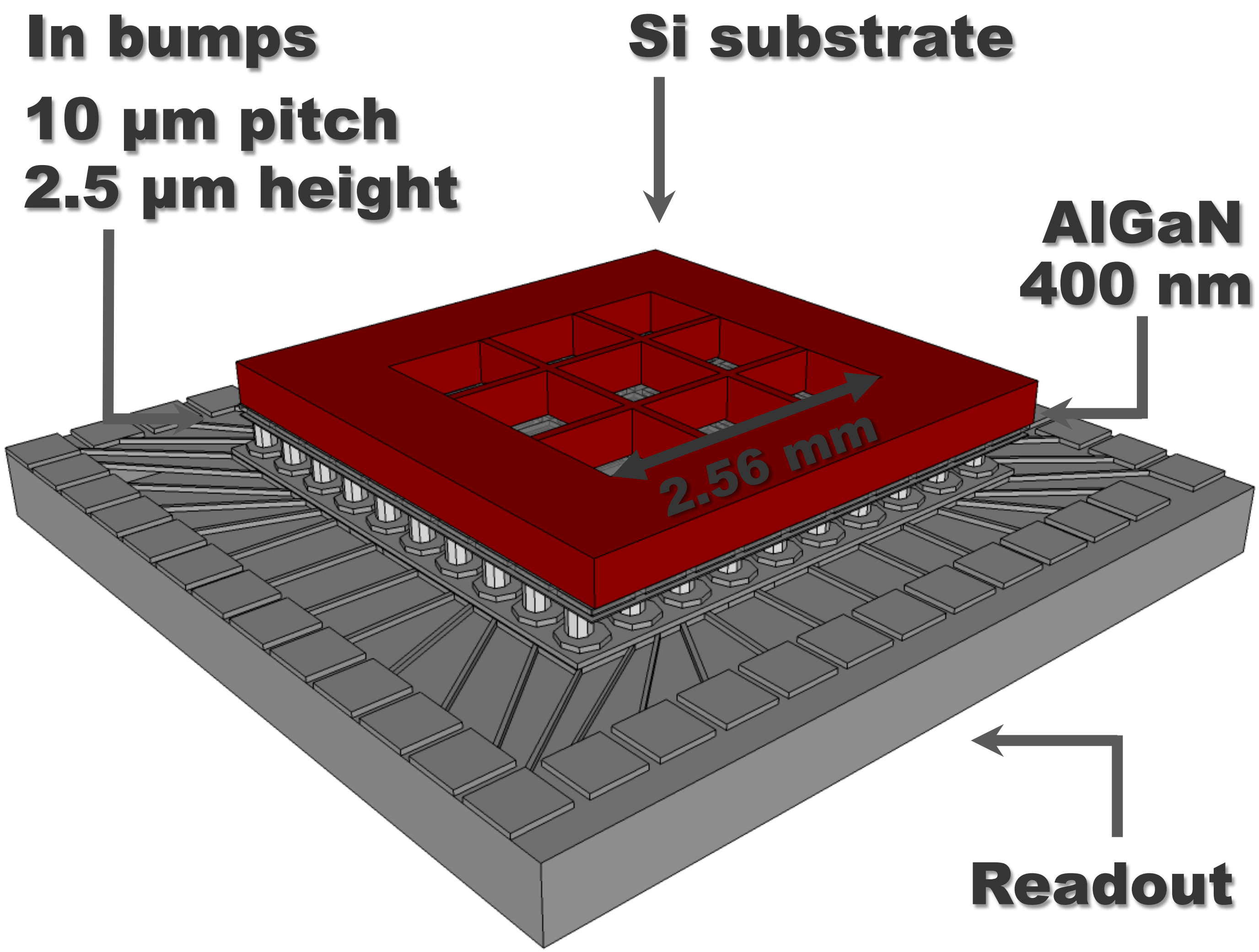
Imager after integration



Complete Si substrate removal

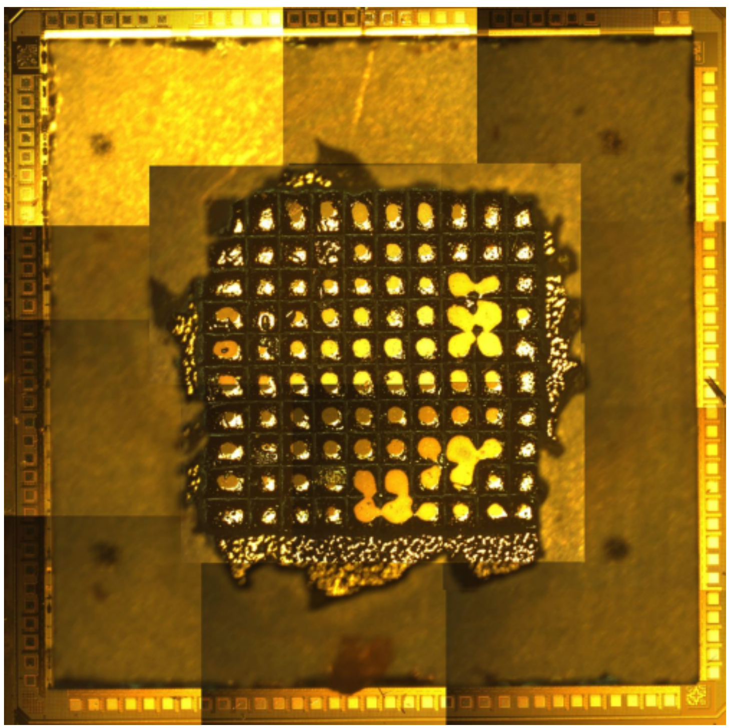


Si removal with grid pattern

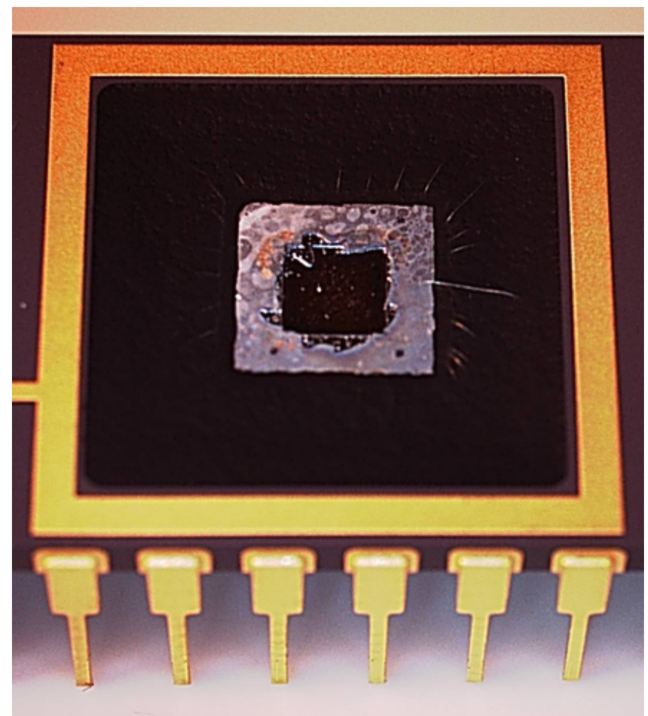


Improved Packaging

- imager encapsulated in GlobTop after wire-bonding
- better protection of the wires and the readout chip



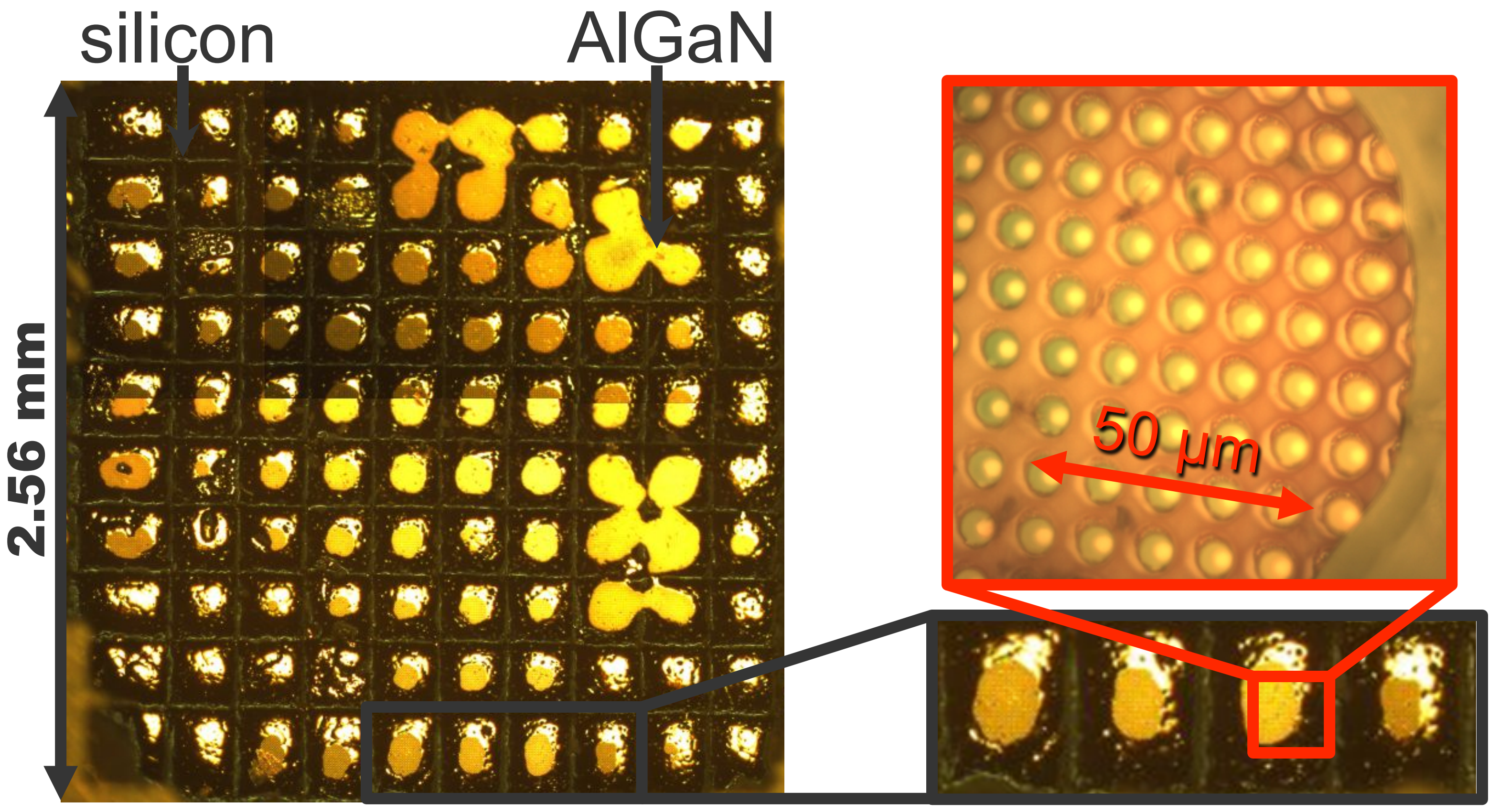
AlGaN imager, top view



AlGaN imager encapsulated with GlobTop

Si removal with grid pattern

- increased mechanical stability
- shadow mask on AlGaN layer



INTRODUCTION TO ALGAN

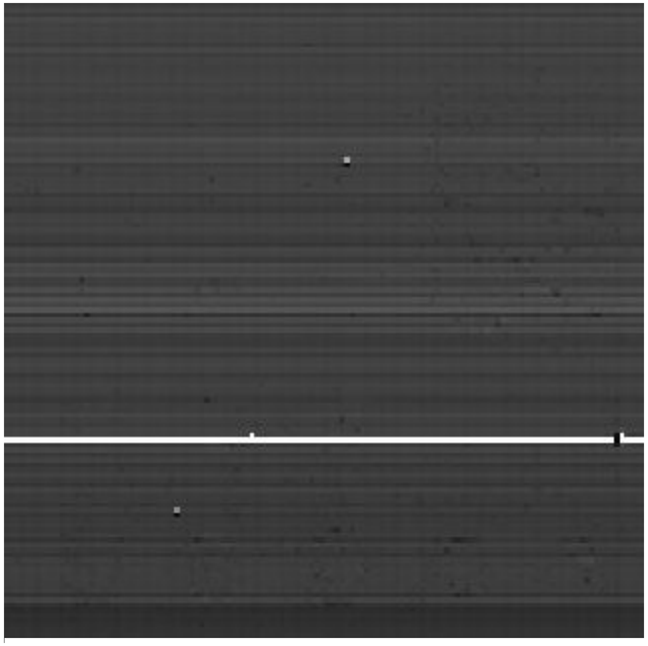
SINGLE PIXEL DETECTORS

INTEGRATION AND IMAGERS

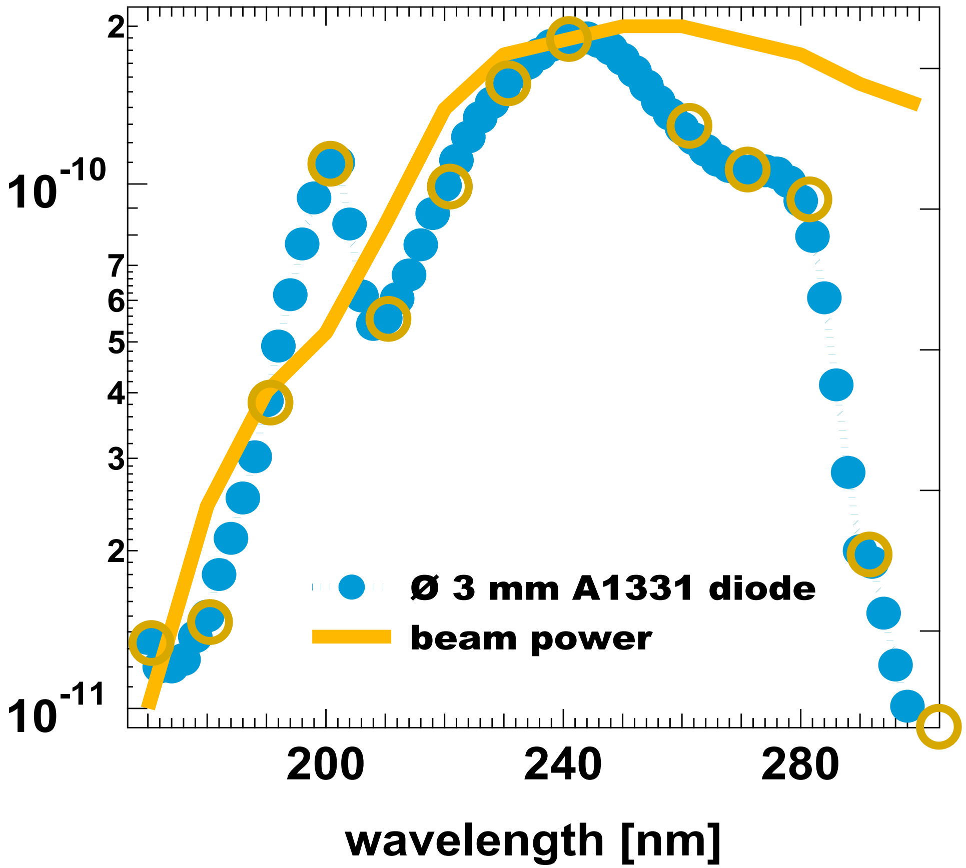
RESULTS IN UV AND EUV

SUMMARY AND CONCLUSIONS

Imagers



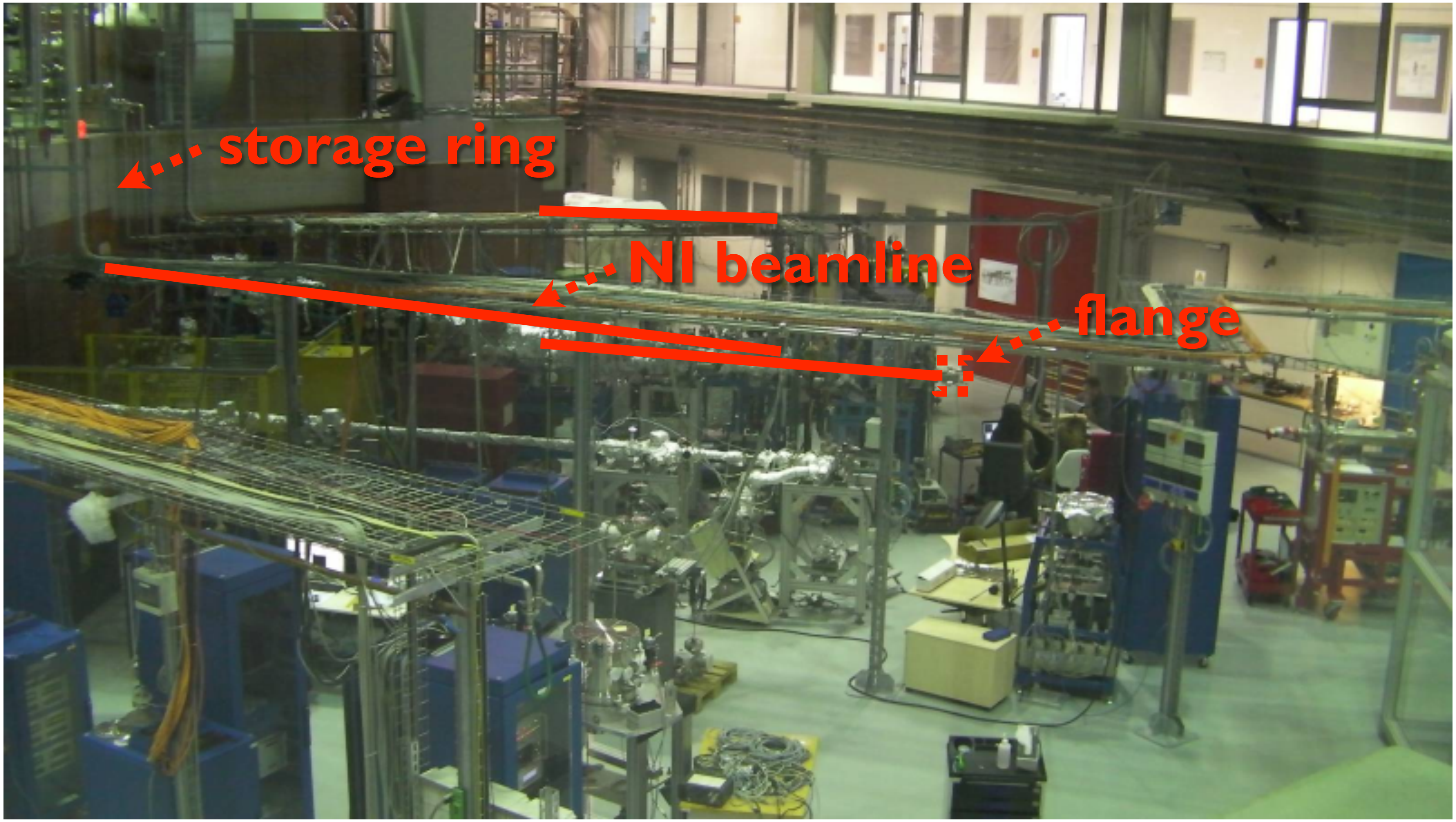
320 nm



- measurements of the imagers under illumination
- → Si etching issue : only few pixels are sensitive

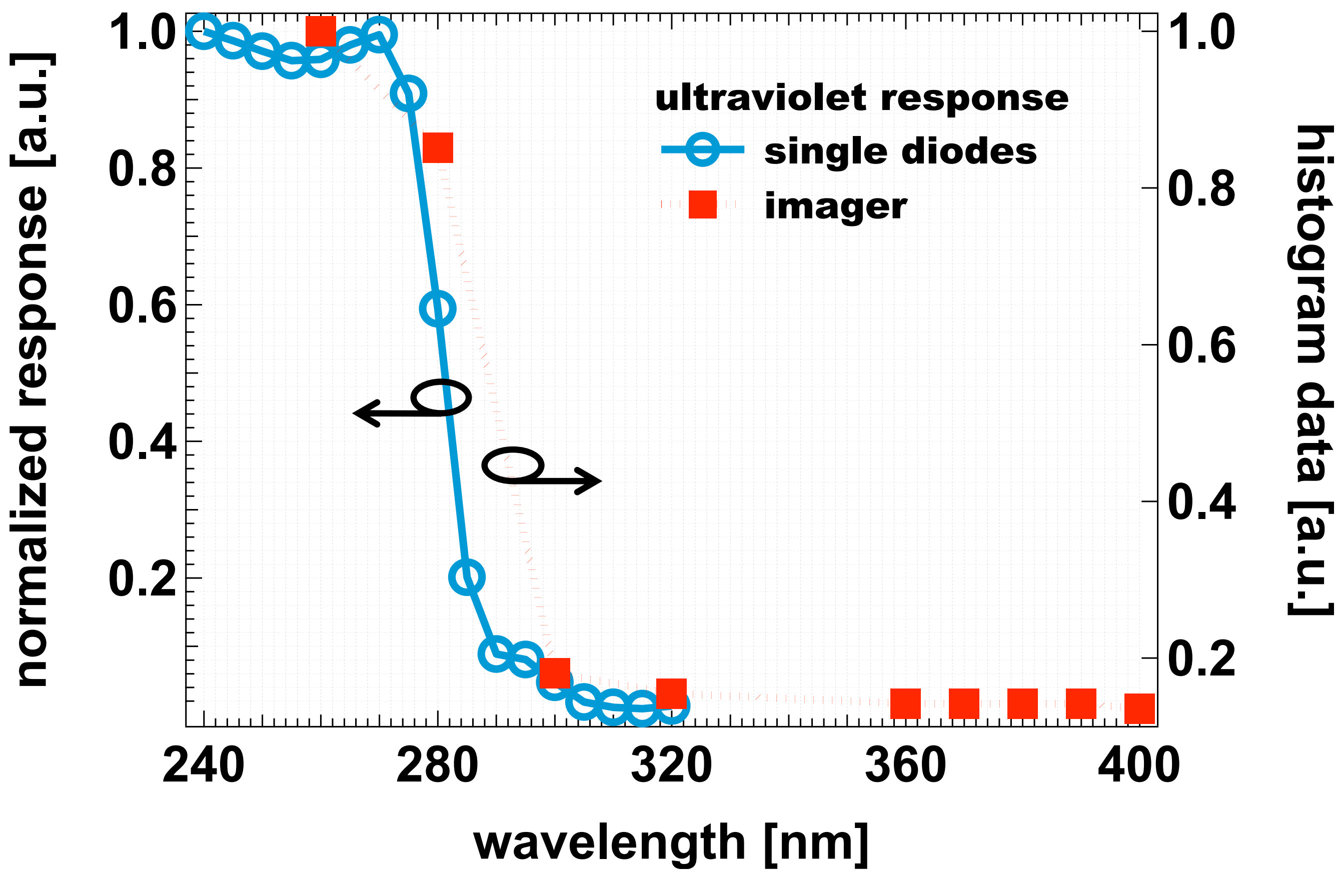
PTB CAMPAIGN: IMAGERS

- Normal Incidence beamline (40÷60 nm, 115÷330 nm)



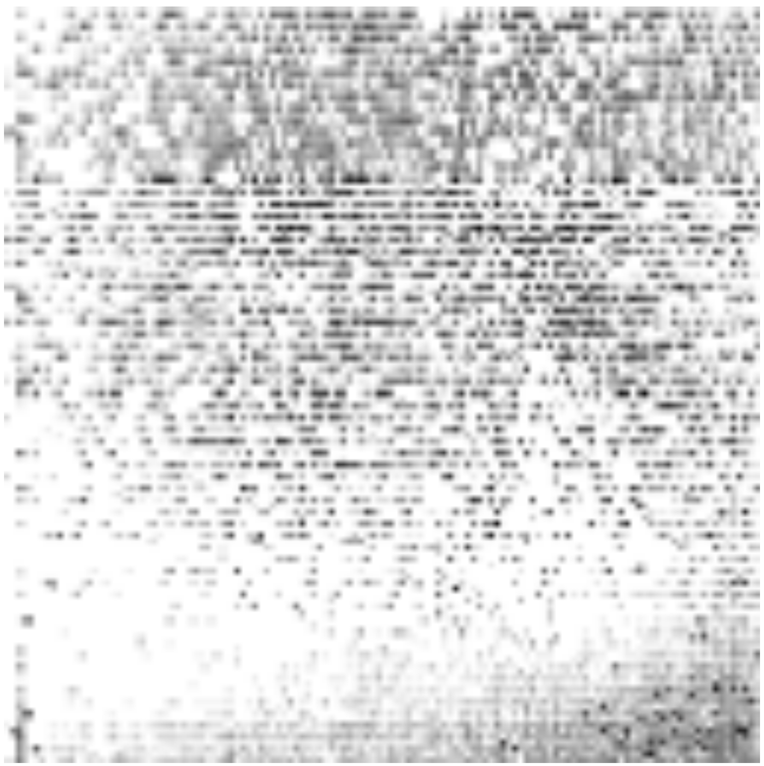
IMAGERS

- signal recorded only up to 280 nm: 40% AlGaN cut-off wavelength
- calculation of the spectral response from the histogram

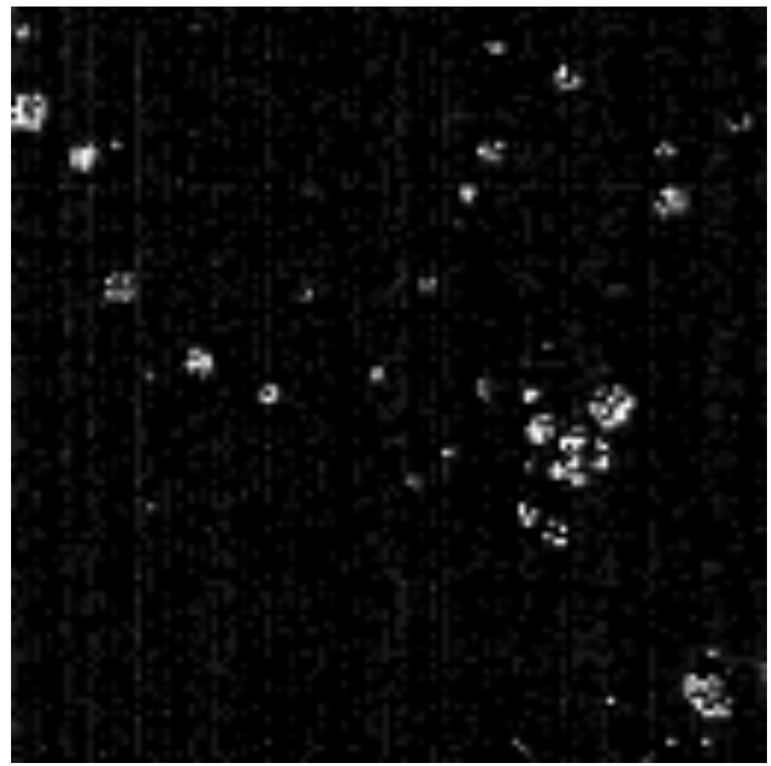


Thin Si layer left on top of AlGaN

- pixels active in the entire area of 128x128 pixels
- EUV radiation has enough energy to penetrate through thin Si



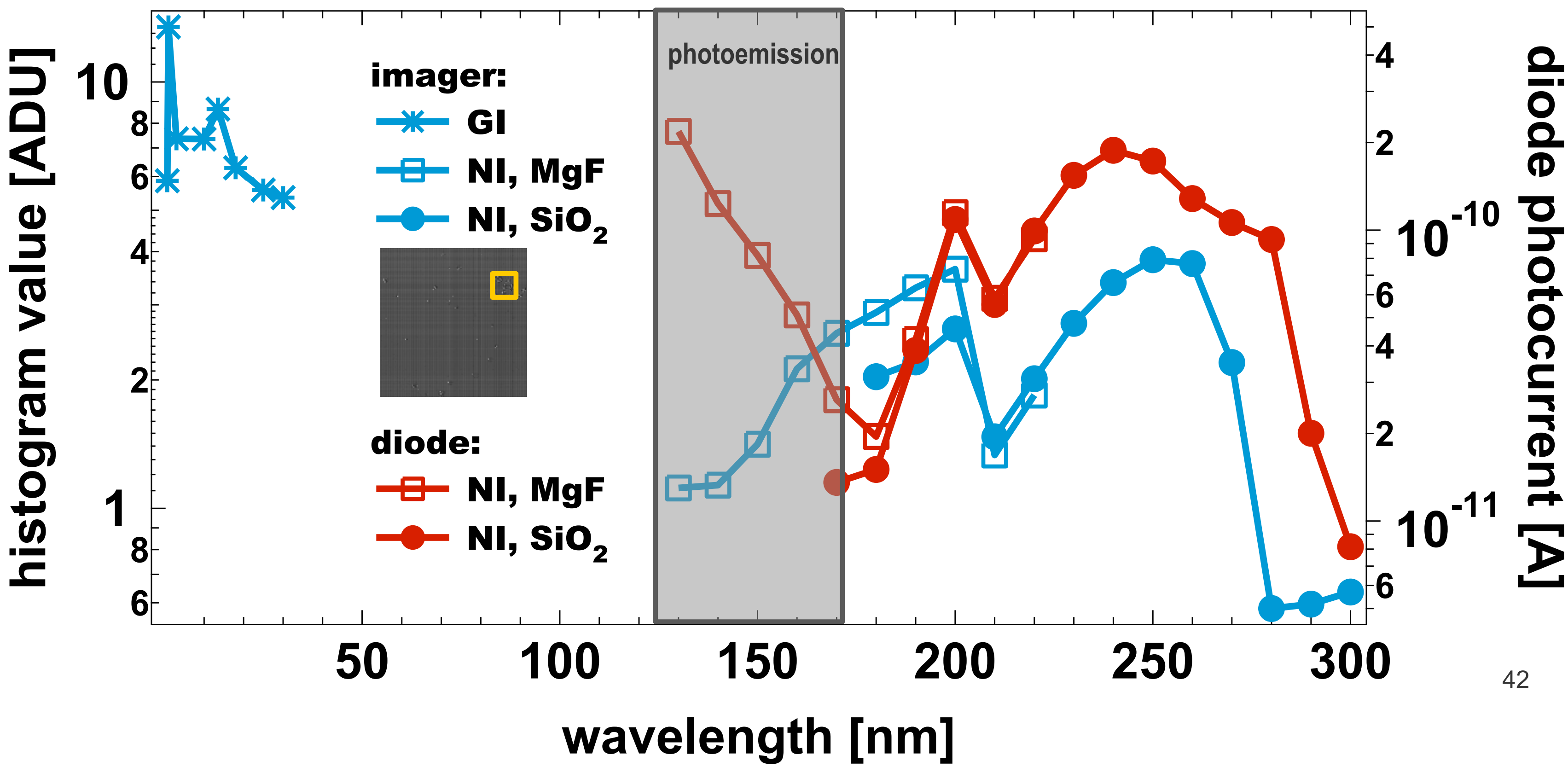
1 nm



240 nm

Analysis of the active pixels

- histogram values plotted vs. normalized spectral responsivity
- a 3 mm diode from the same wafer taken as reference
- a dip at 210 nm noticed again



Introduction to AlGaN

Single Pixel Detectors

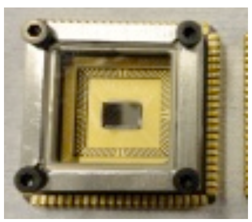
Integration and Imagers

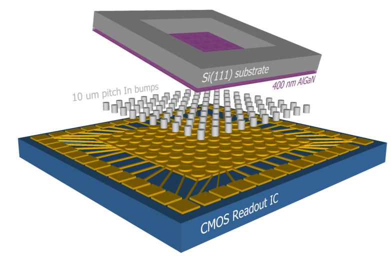
Results in UV and EUV

Summary and Conclusions

Summary/Conclusions

- EUV detectors development activities for EUI onboard SOLO
  - **Apsolute** : FSI fully characterized, BSI under processing
  - **BOLD** : AlGaN-on-Si based detectors for EUV applications
    - intrinsic solar blindness, sensitivity demonstration down to 1 nm
    - proof-of-concept for 10 µm pitch imagers (256x256)

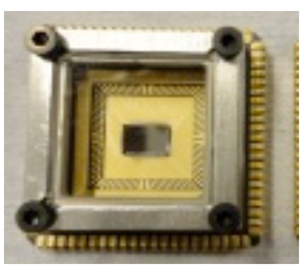


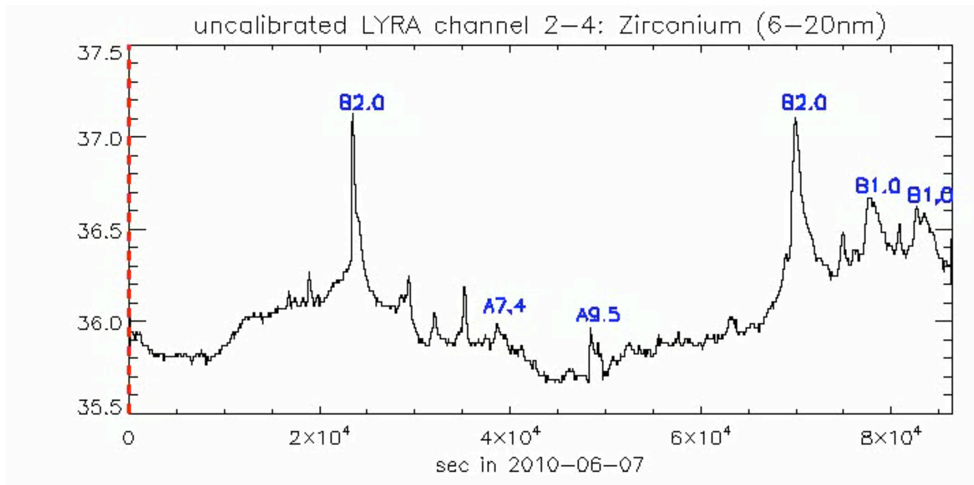


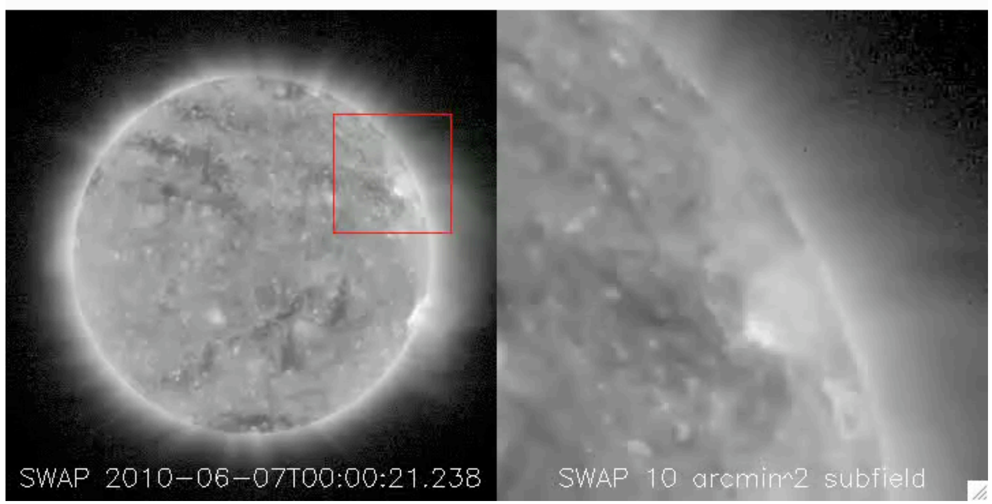
- Next steps for Apsolute: calibration and radiation tests:

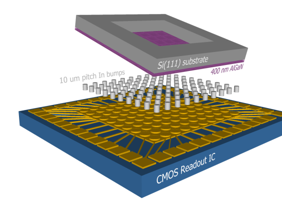
- EUV (1-30nm) – VUV (40-240nm) @ PTB/Bessy II (Week 29 – 18-22 July 2011)
- TID test (Gamma) @ CRC (Louvain-La-Neuve, Be), mid-August (→ 300krad)
- Proton (10, 30 and 60 MeV) and Heavies ions tests (SEL>60 MeV.cm2/mg)
  - → In the planning (sept, oct)
- EUV – VUV @ PTB/Bessy II (hopefully end of November 2011)

THANKS FOR YOUR ATTENTION









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