Caliste-256, 580 µm pixel pitch CdTe imaging spectrometer for space science

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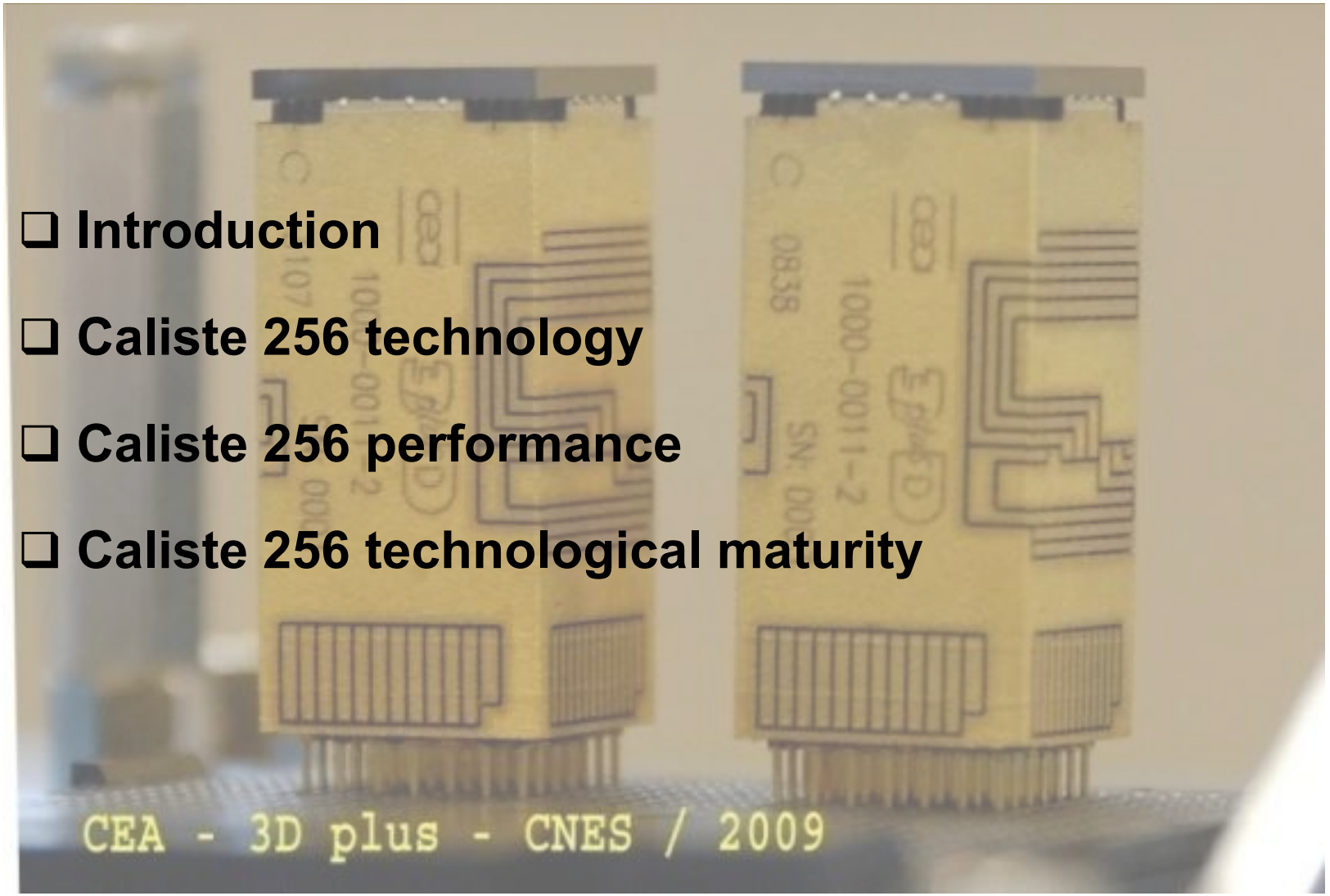
Outline



- Introduction
- Caliste 256 technology
- Caliste 256 performance
- Caliste 256 technological maturity

Recent developments for CdTe detectors

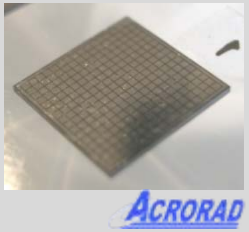
- Activity supported by CEA and CNES since 2003
- Goals
  - Bounce on Integral/ISGRI return
  - Demonstrate entirely new sensors based on CdTe pixel detectors in the hard X-ray domain
  - Develop new devices for space applications
    - High reliability and modular concept
  - Demonstrate high performance
    - Spectroscopy, imaging, timing
- Means
  - Microelectronics development in house for analog front-end ASICs
    - Low noise, low power, radiation hard
  - Industrial means for device production
    - Hybrid stacking technology
  - Development according on space rules
    - Technological evaluation for high technological readiness level
  - Performance evaluation

Needs for future hard X-ray astronomy missions

- Simbol-X, Astro-H, NuStar, NHXM...

- Energy band: 4-80 keV
- ~10 arcsec angular resolution
  - Typ. 1-2 mm HEW PSF
- Large effective area
  - ~10 arcmin field of view
- High spectral resolution
  - Typ. 1.2 keV FWHM @ 60 keV
- Background rejection by anticoincidence
  - Timing resolution < 100 ns rms
  - Integration in the shielding

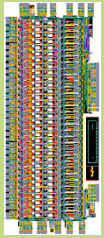
Detector



- ➢CdTe, 1-2 mm thick
- ➢Fine pitch pixels
- ➢Mosaïc of 1 cm^2 crystals
- ➢Low leakage current

Front-end electronics

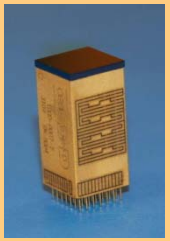
IDeF-X



- ➢Low noise ASIC
- ➢Time-walk correction

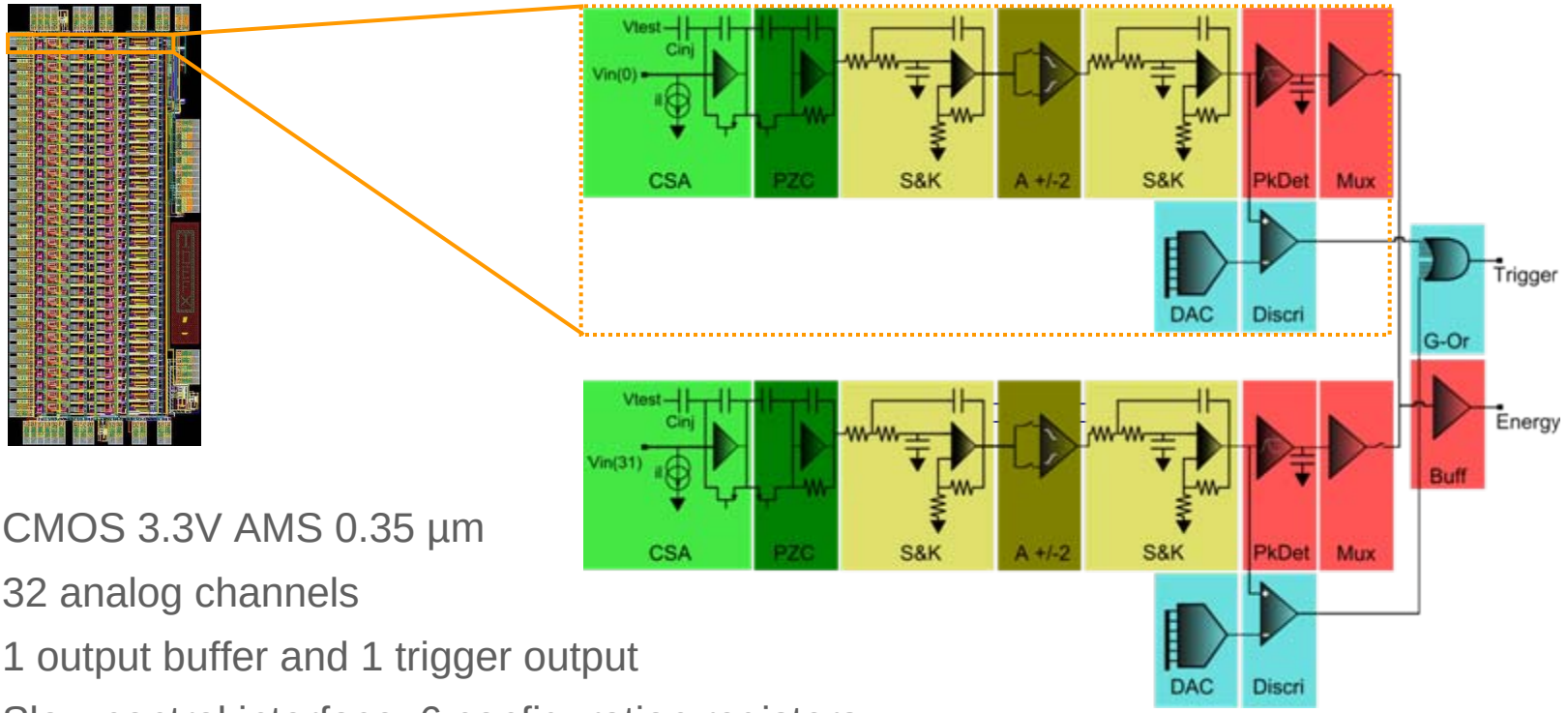
Hybridization

Caliste



- ➢Low input capacitance
- ➢4-side buttable device

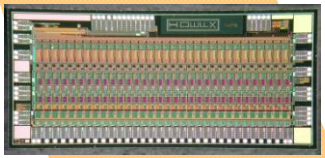
IDeF-X v2 front-end ASIC for Caliste-256



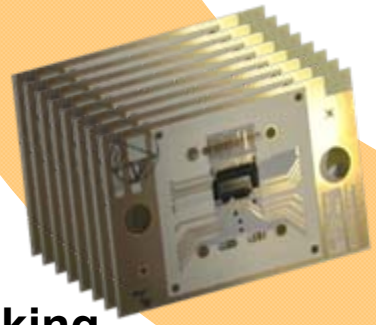
- CMOS 3.3V AMS 0.35 µm
- 32 analog channels
- 1 output buffer and 1 trigger output
- Slow control interface, 6 configuration registers
- Gain: 200 mV/fC
- Dynamic range: 50 ke-
- Shaper peaking time: 0.9-9 µs
- Individual low-level threshold set by 6-bit DAC
- 3 readout modes: all channels, hit channels or on demand

Caliste-256 design and technology

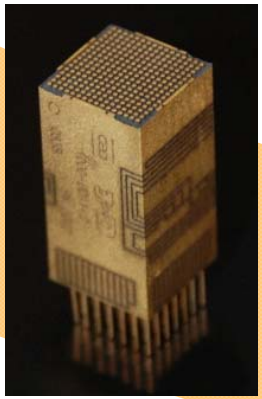
IDeF-X v2 ASIC
32 analog channels



Mounting on PCB

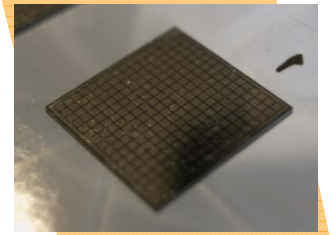


8 ASIC stacking
perpendicular to the detection surface

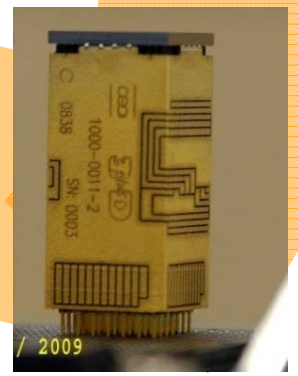


Electrical body
with a 7 x 7 pin grid array

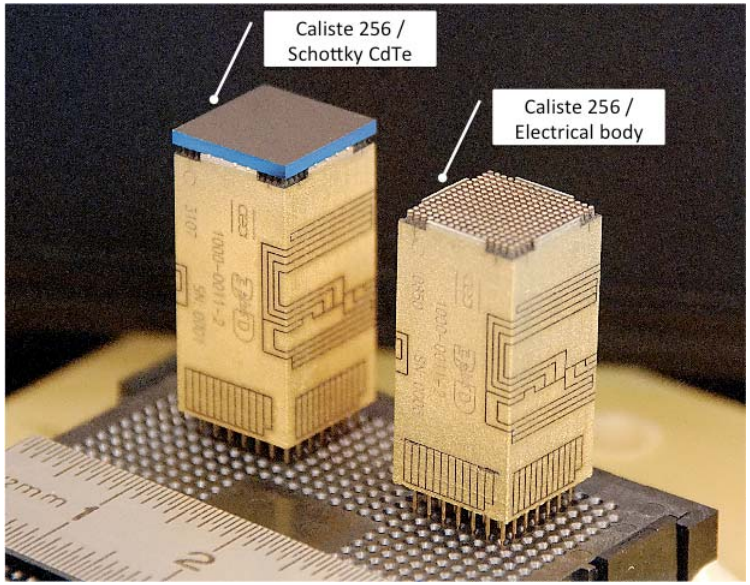
Cd(Zn)Te 256-pixel detector
(0.58 mm pitch, 1 or 2 mm thick)



Caliste-256 camera

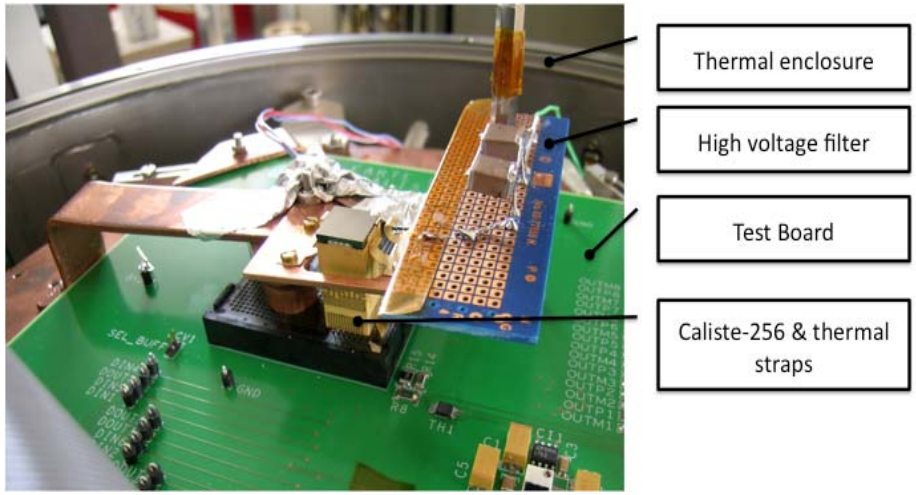


Caliste-256 fabrication and tests



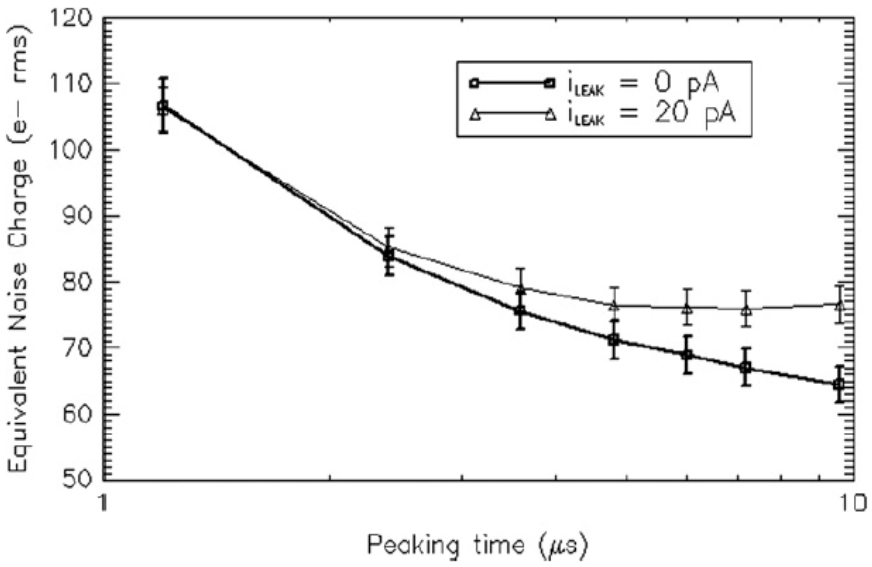
- Mean features
  - 16 × 16 pixels of 580 µm + guard ring
  - Volume: 10 × 10 × 21 mm^3 ; Mass: 4 g
  - Power: 816 mW (3.2 mW/channel)
  - 220 keV energy range
  - Programmable individual low-level threshold (step ~0.28 keV)
  - 8 differential outputs

- Operation in the lab
  - Vacuum chamber + cold finger
  - 14-bit ADCs
  - 20 MHz sequencing clock
  - 1 FPGA for ASIC and ADC control and data frame packaging

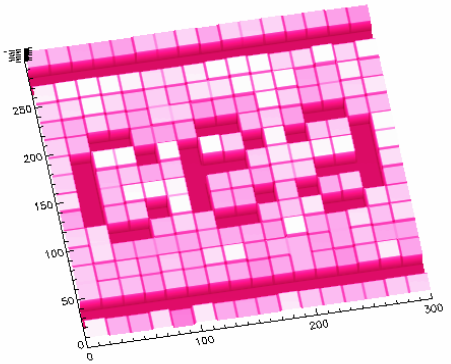


Noise performance

- Characterization with test injection signal over the 256 channels
  - 65 electrons rms without detector



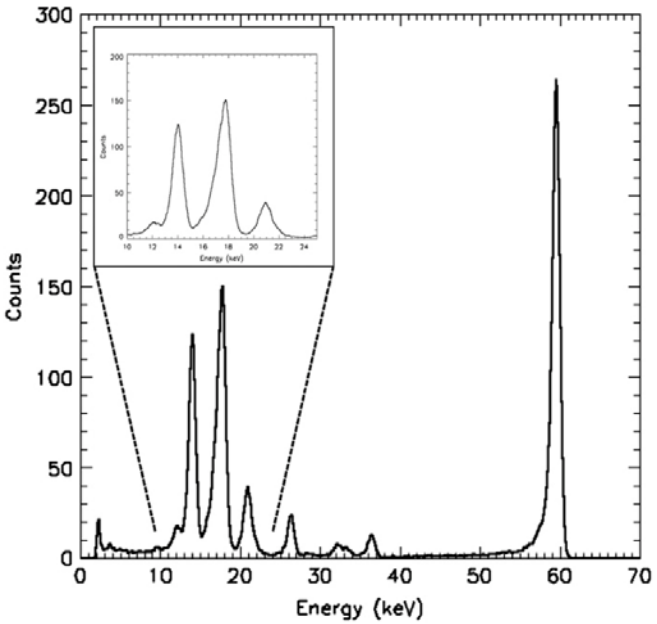
- Uniformity
  - σ_{256} = 5 el. rms (8%)
- Expected energy resolution (70 el. rms)
  - 0.76 keV FWHM @ 14 keV
  - 0.86 keV FWHM @ 60 keV



Noise map with test injection pattern

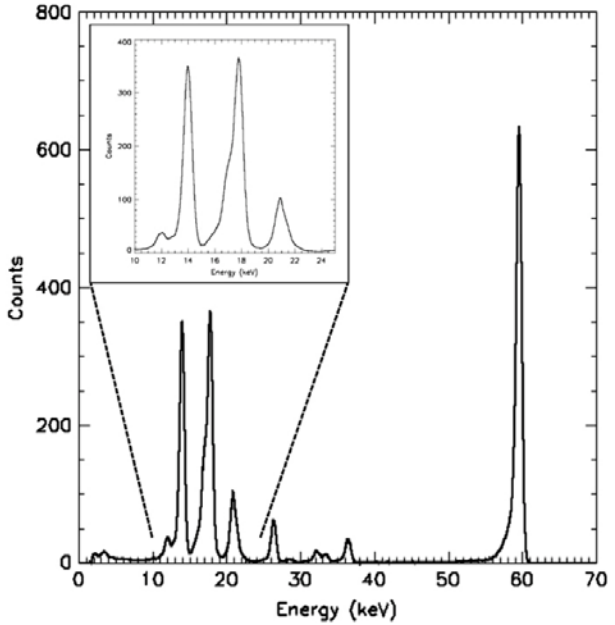
Spectroscopic characterization with ^{241}Am source

- 2 mm-thick CZT



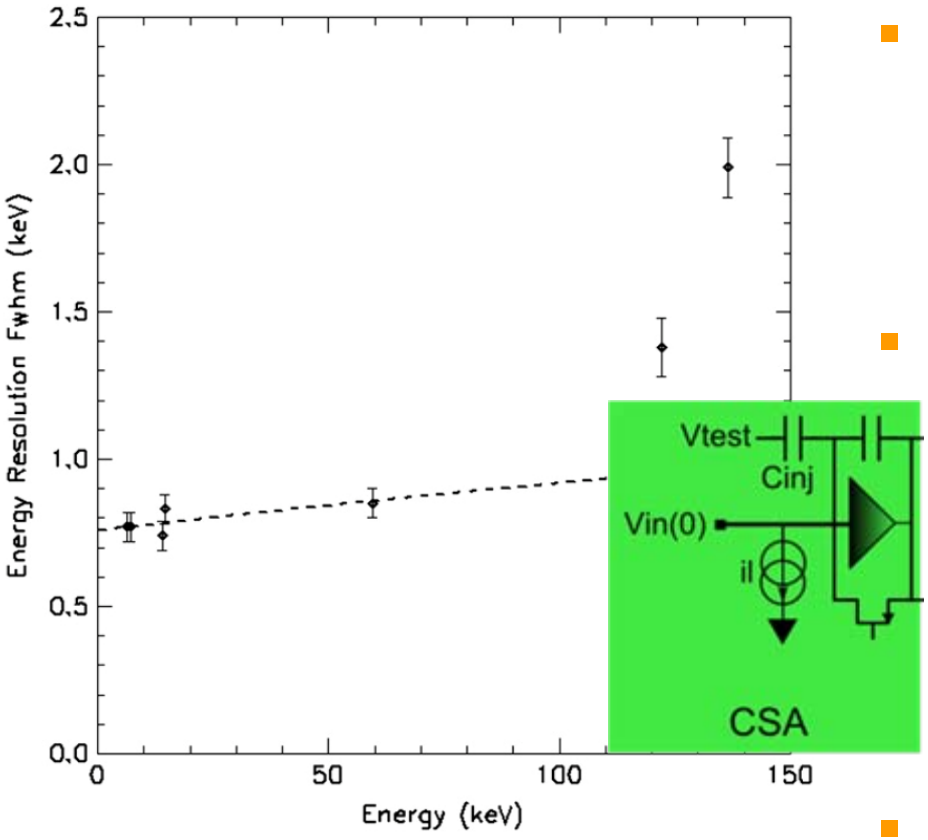
  - 800V, –15°C, 6.0 µs peaking time
  - 0.91 keV FWHM @14 keV
  - **1.09 keV FWHM @60 keV**
    - σ_{256}= 0.13 keV fwhm (12%)
  - **Low threshold ~2 keV**
  - Extracted current 30 pA/pixel

- 1 mm-thick Schottky CdTe



  - 300V, 0°C, 9.6 µs peaking time
  - 0.73 keV FWHM @14 keV
  - **0.85 keV FWHM @60 keV**
    - σ_{256}= 0.09 keV fwhm (11%)
  - **Low threshold ~1.5 keV**
  - Extracted current 10 pA/pixel

Energy resolution: analysis



- 1.38 keV FWHM @122.06 keV
  - σ_{256}= 0.09 keV fwhm (11%)
  - ~1.0 keV expected
- Interpretation: CSA architecture
  - Output voltage of the CSA opens the feedback reset transistor
    → causes additional noise source on the signal itself,
    → called **non-stationary noise**
- Fixed in the new IDeF-X version
  - See poster ID62 / session IV (A. Michalowska)

Technological evaluation

ASIC level (IDeF-X)
Hybrid level (Caliste)

- Total ionizing dose: OK up to 1 Mrad
- Latch-up: LET threshold > 65 MeV.cm^2.mg^{-1}
- Single-event upset: LET threshold > 9 MeV.cm^2.mg^{-1} (on-chip detection)
- Life-test: OK up to 2000 h at 125°C
- Sine vibrations: 20 *g*, 20-2000 Hz, 3 axis → passed
- Shocks: 1500 *g* → passed
- Thermal cycling: 50 cycles –55°/55°C + 50 cycles –55°/100°C → passed
- THB (temperature, humidity, bias): 240 h at 85°C/ 85% RH → passed

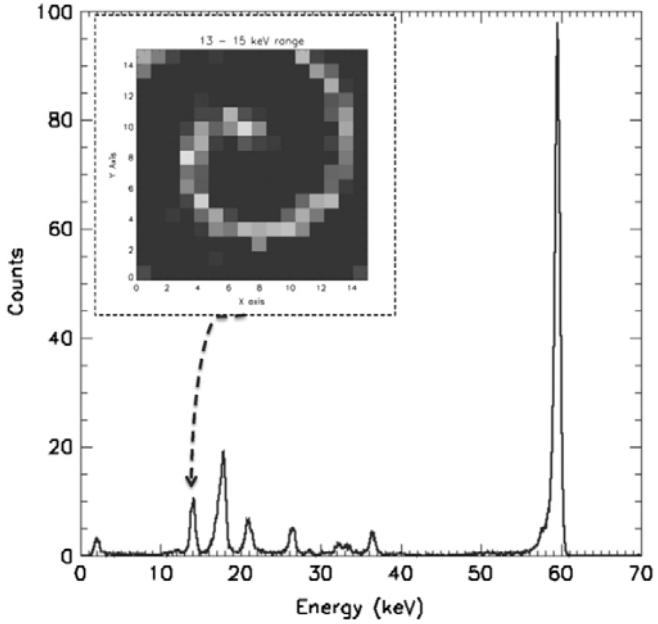
Conclusions

Tests performed according to ESA standards.

All tests required for space qualification have been passed.

Conclusions

- Caliste 256 performs in hard X-rays high resolution imaging spectroscopy.



- Technology mature to be used as a space-qualified component

- Ways of improvement
  - Power consumption (3 mW/channel) → thermal issue
  - Electrical interface (49 pins) → integration and PCB routing issue

- Next steps
  - New Caliste generation: 8 IDeF-X HD ASIC, 0.8 mW/channel, 16 pins
  - Modular assembly of Caliste Spectroscopic Imagers (MACSI)

For the next NDIP conference…

- MACSI: 8 cm^2 CdTe camera, 2048 channels