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High speed imaging using a capacitive division technique

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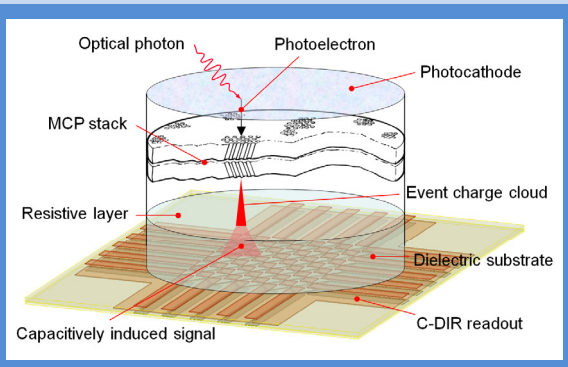
Introduction

The charge division technique is a simple concept used in photon-counting imaging detectors. It determines one or two dimensional event coordinates by locating the centroid of the charge cloud generated in the detector.

The Capacitive Division Image Readout (C-DIR) is a 'game-changing' charge division readout with major performance advantages which is simple and economical to construct. C-DIR utilizes three elements:

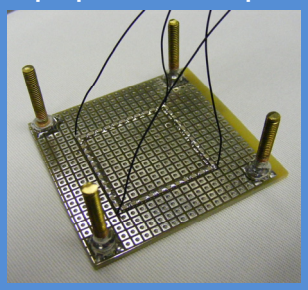
- a resistive layer providing event charge localization during signal measurement and DC signal current return path
- a dielectric substrate which provides electrical isolation from the detector voltages and capacitively couples the event transient signal to the third element, which comprises…
- an array of capacitively coupled electrodes which divides the signal among several charge measurement nodes

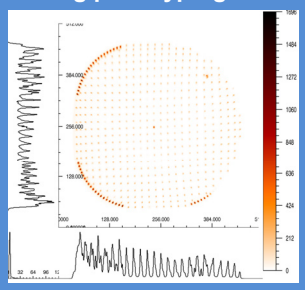
The purely capacitive signal paths have high bandwidth and present a low capacitive load to the preamplifiers, allowing an unprecedented combination of excellent event timing and spatial resolution.



- Event charge is localized on resistive "charge localizer"
- Transient signal induced through dielectric substrate
- Dielectric substrate acts as part of vacuum housing
- Induced signal sensed by C-DIR readout
- C-DIR - an array of capacitively coupled electrodes

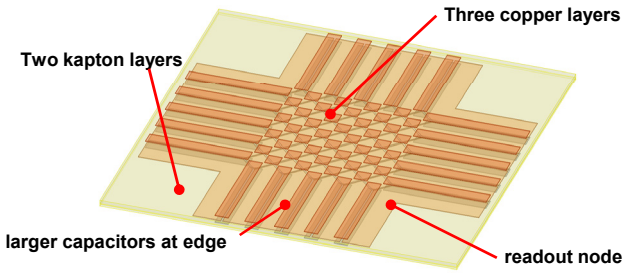
Simple proof-of-concept demo using prototyping PCB





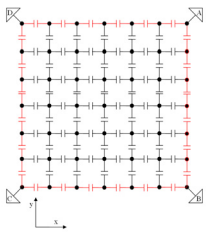
- Prototyping board consisting of an array of isolated vias
- Used as a capacitively coupled electrode array
- Surface mount capacitors mounted along active area perimeter
- Charge signals read out at 4 corner nodes (wires in photo)
- C-DIR underside in contact with detector dielectric substrate
- Image from detector illuminated via 1 mm pitch pinhole array
- Obtained with unoptimised readout design and electronics
- ~150 microns FWHM achieved at <10^6 gain

Optimised C-DIR pattern design

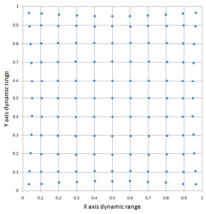


- Simple manufacture – using standard flex PCB construction
- Four signals read out with charge sensitive preamplifiers
- Higher capacitance at edges maintains readout linearity
- 8 pF preamplifier input capacitance for a 25.4 mm^2 pattern
- ~85% charge collection efficiency

Effective equivalent circuit



Simulated linearity using FEA model



Capacitive division advantages

- Capacitively coupled – therefore no resistive noise
- No geometric charge division – therefore no partition noise
- Purely capacitive – high speed signal with MCP-limited timing
- Sole noise - electronic, dominated by preamp input capacitance
- 25 x 25 mm^2 C-DIR – modelled pattern capacitance of 8 pF!
- Very low total noise possible (<200 e^- rms at τ=250ns) ⟶ 1000 1000 pixel^2 at 10^6 electrons.
- Simple linear algorithm – minimal digital processing required
- Excellent linearity - able to utilize >80% of anode dynamic range
- Capacitances in-built in pattern geometry – no discrete cpts.

Game-changing attributes

- Very low noise – expands spatial resolution/count rate envelope via choice of pulse shaping and detector gain
- Capable of MCP-limited timing with fast electronics
- Flexible format – scalable from 10 mm square to 100 mm square
- Simple operation – capacitive coupling means no vacuum compatibility issues or vacuum feedthroughs required

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