An acquisition system for CMOS imagers with a genuine 10 Gbps bandwidth

ID: 164

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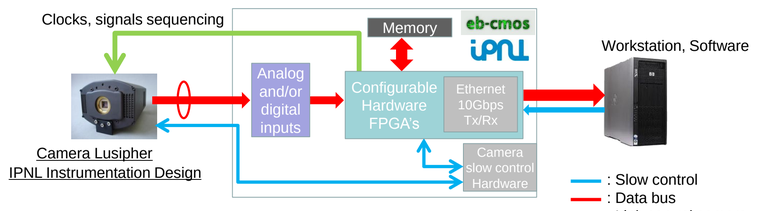
Goals

Design and achieve an **acquisition system for CMOS image sensors** that allows the data transfer over a **high speed link** with:

- ✓ **In-line computing** → ▪ **Workstation, Software**
- ✓ **On board processing** → ▪ **FPGA, Memory**
- ✓ **High bandwidth** → ▪ **Ethernet, UDP**
- ✓ **An open system** → ▪ **Custom mezzanine**

How ?

- ✓ A custom electronic system
- ✓ A 10Gbits Ethernet link between the card and a commercial Ethernet controller.
- ✓ A rugged workstation and an optimized software



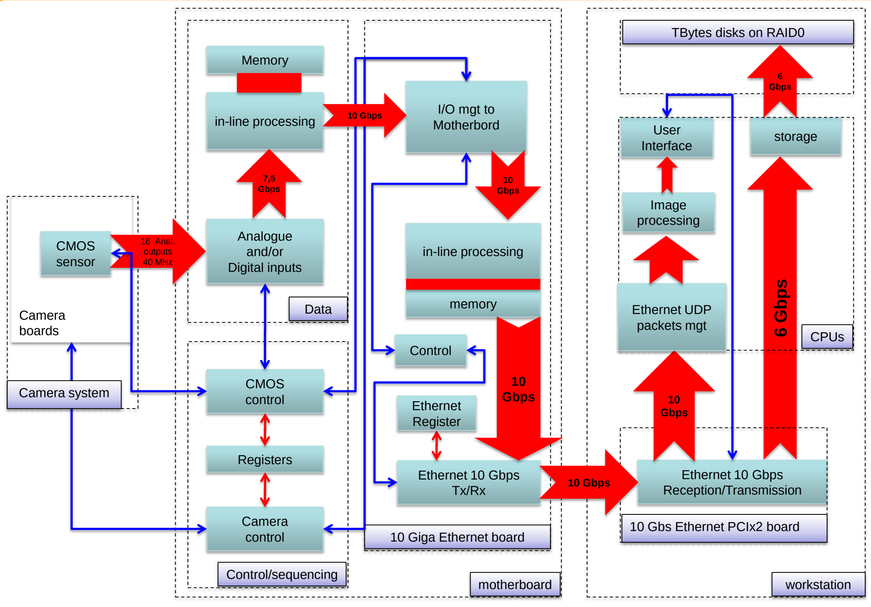
Applications

Used with the scientific low light camera Lusipher, **800x800** pixels **and single-photon sensitive: thanks to** electron-bombardment of the CMOS.

Applications:

- ✓ Fluorescent single-molecule tracking
- ✓ Bio-luminescence imaging
- ✓ Quantum Dots tracking
- ✓ Single-cell tracking (*E. Coli*)
- ✓ Microarray imaging – DNA chip
- ✓ Adaptive Optics

Data Acquisition System



Synoptic of the 10Gbps Ethernet acquisition system

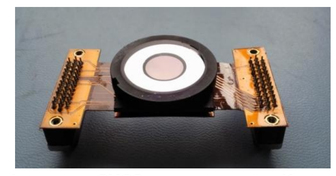
Features:

On board:

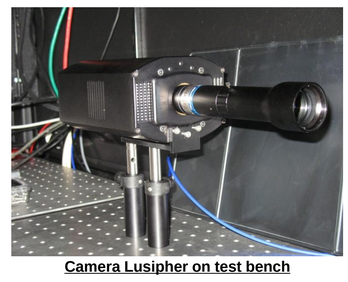
- ✓ **Drive** the CMOS sensor (digital pattern generator with clock, reset …)
- ✓ Frame **reconstruction from the pixels ADC values (16 inputs)**
- ✓ Frame **preprocessing** (Correlated Double Sampling)
- ✓ **Slow control of the camera and the ebCMOS**
- ✓ **Data transmission** to workstation

On the workstation:

- ✓ Manage the **10 Gbps Ethernet continuous input flow**
- ✓ **Reconstruct** the image and perform **multithreading** for **in-line image processing**
- ✓ Manage the **machine vision system**



Lusipher ebCMOS connected by flex Kapton

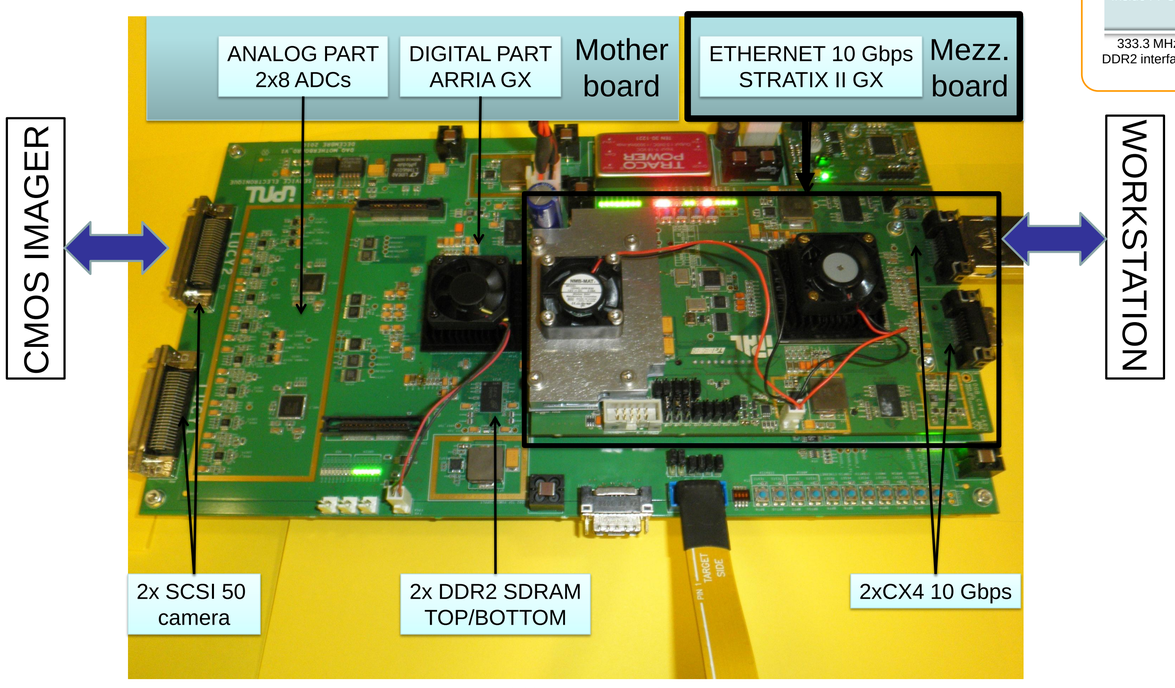


Camera Lusipher on test bench

Board Architecture and Design

Boards architecture:

- ▪ 16 analog channel digitized with AD9222 (Analog Device,12bits)
- ▪ ARRIA GX and STRATIX II GX FPGA coupling with DDR2 modules (Micron MT47H32M16)
- ▪ No processor used
- ▪ Very high speed bandwidth connectivity (CX4, mezzanines)
- ▪ Temperature monitoring and cooling
- ▪ DC/DC and linear power supply
- ▪ Jtag, Flash configuration hardware
- ▪ Tests



Acquisition System Boards

Hardware performances:

- ▪ Imaging at 1000 fps
- ▪ 2 x 10Gbps Ethernet link for acquisition
- ▪ 16 analog channels digitized at 40Mhz (7.68 Gbps)
- ▪ 4 x 32bits memory buses (bandwidth)
- ▪ Up to 21.3 Gbps Memory bandwidth on board
- ▪ Creation of Ethernet frame (UDP)
- ▪ 4Gbits DDR2 SDRAM
- ▪ Serial link to mezzanine or digital boards with 12.5Gbps bandwidth

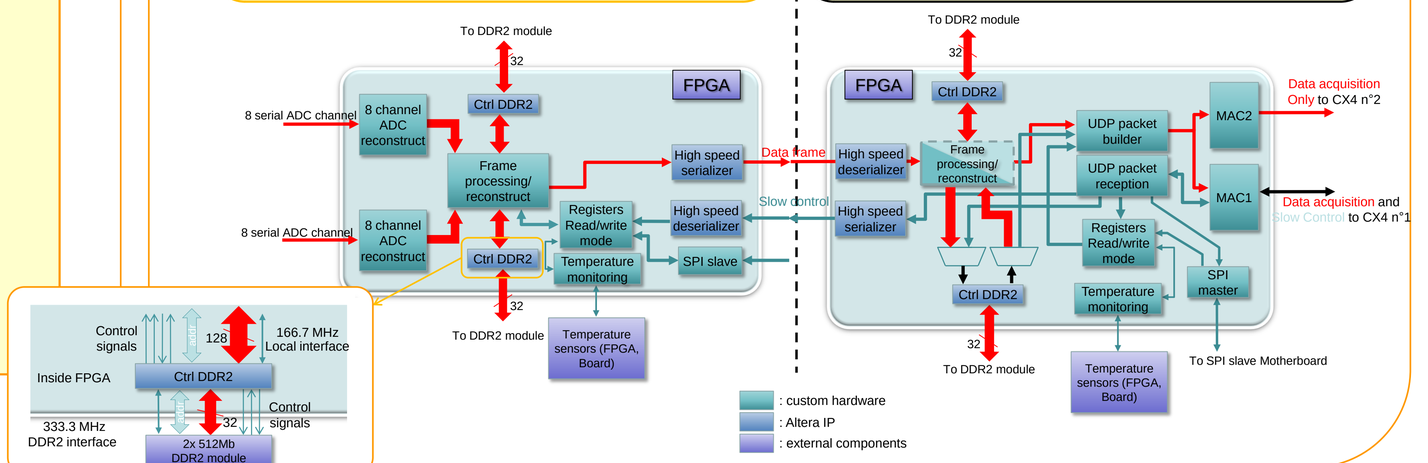
FPGA Architecture

Motherboard FPGA architecture:

- ▪ ARRIA GX EP1SGX90FF1500 (Altera)

Mezzanine FPGA architecture:

- ▪ STRATIX II GX EP2SGX90FF1500 (Altera)



Software

Software performs:

- ▪ Data reception from socket
- ▪ In-line Storage on HDD or SSD
- ▪ Frames building
- ▪ SNR computing
- ▪ Clustering – Single Phe Sensitivity
- ▪ ebCMOS Noise suppression
- ▪ Kalman filtering (spatial and temporal)
- ▪ Display frames (GUI)

✓ in real time at 6,7 Gb/s
✓ CPU usage : 50%

Platform:

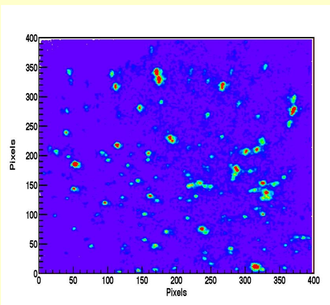
- ▪Hewlett-Packard Z800 with two 6-cores Intel Xeon X5660
- ▪ Storage : OCZ Z-Drive R2 p88
- ▪ Network : Mellanox MNEH29-XTC
- ▪ OS : Linux 2.6.35 (Ubuntu)

Software:

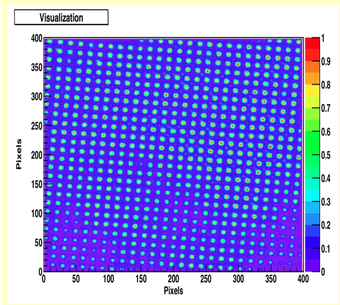
- ▪ Multithreaded (pthread)
- ▪ SSE, NUMA, cache memory optimization
- ▪ HDD writing optimization
- ▪ Qt for display

Conclusion and perspectives

- ▪ More In-line processing
  - ▪ Cluster finding optimization
  - ▪ Local Noise suppression
  - ▪ Multi spot tracking
- ▪ 40 Gbps upgrade
- ▪ GPU computing



CdSe Quantum Dots



640 spots of a microlens array