6th International Conference on New Developments In Photodetection
NDIP 2011 — Lyon - France, July 4-8, 2011

PMm²

AGENCE NATIONALE DE LA RECHERCHE ANR

LABORATOIRE DE L'ACCÉLÉRATEUR LINÉAIRE

IN2P3 — INSTITUT NATIONAL DE PHYSIQUE NUCLÉAIRE ET DE PHYSIQUE DES PARTICULES

CNRS — CENTRE NATIONAL DE LA RECHERCHE SCIENTIFIQUE

Omega

PARISROC

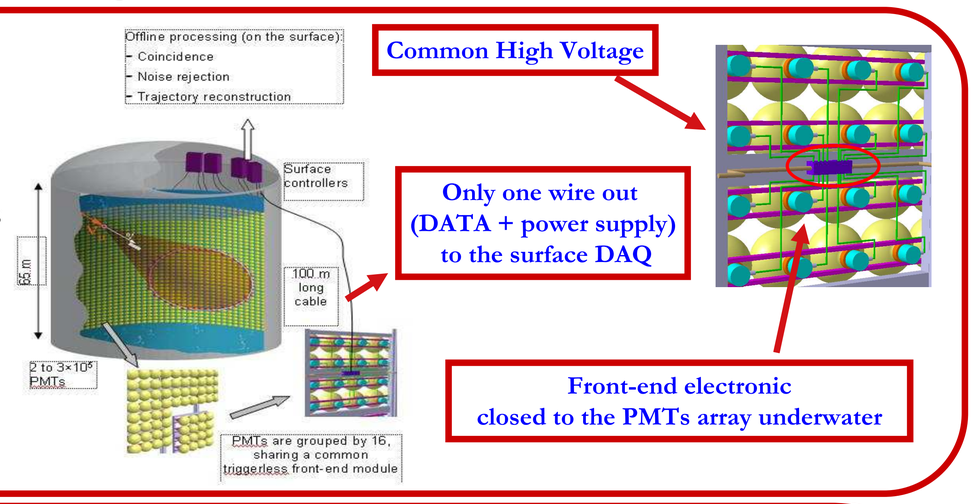
S. Conforti Di Lorenzo*[a], J.E. Campagne[a], F. Dulucq[a], S. Drouet[b], M. El Berni[a], C. de La Taille[a], B. Genolini[b], G. Martin-Chassard[a], N. Seguin Moreau[a], E. Wanlin[b], Y. Xiangbo[c].
*Corresponding author: conforti@lal.in2p3.fr - Phone: +33 1 64 46 82 87 - Fax: +33
[a]Laboratoire de l'Accélérateur Linéaire, IN2P3-CNRS, Université Paris-Sud, Bat. 200, 91898 Orsay Cedex,
[b]Institut de Physique Nucléaire d'Orsay, IN2P3-CNRS, Université Paris-Sud, 91406 Orsay Cedex, France
[c] Institute of High Energy Physics, Beijing, China

An autonomous front-end ASIC for triggerless acquisition in next generation neutrino experiments

Introduction

PMm² ("Square Meter Photomultiplier"):

- A project funded by French Research Agency (ANR-06-BLAN- 0186) for 3 years (2007-2010).
- A collaboration with 3 French laboratories (LAL, IPNO, LAPP) and an industrial company Photonis.
- An R&D project to implement a solution for a low cost and trigger-less acquisition for any detector using large number of photodetectors;
- LAL works on the front-end chip :➔ **PARISROC:**
  - An adjustable gain channel by channel;
  - Auto-trigger on 1/3 of photoelectron (p.e.) (50 fC at PM gain of 106);
  - Charge measurement efficient for 1 p.e. and up to 300 p.e. (50 pC);
  - Time tagging better than 1 ns;
  - Internal ADC (Analog to Digital Converter).
  - Serial data readout.



Performance

16 input preamplifiers :
- ➢ 2 gain paths (high and low gain);
- ➢ PMTs gain adjustment by a factor 4 (8 bits) per channel;
- ➢ Input dynamic range : 0 → 600 pe (0→ 100 pC);
- ➢ Good linearity (1%).

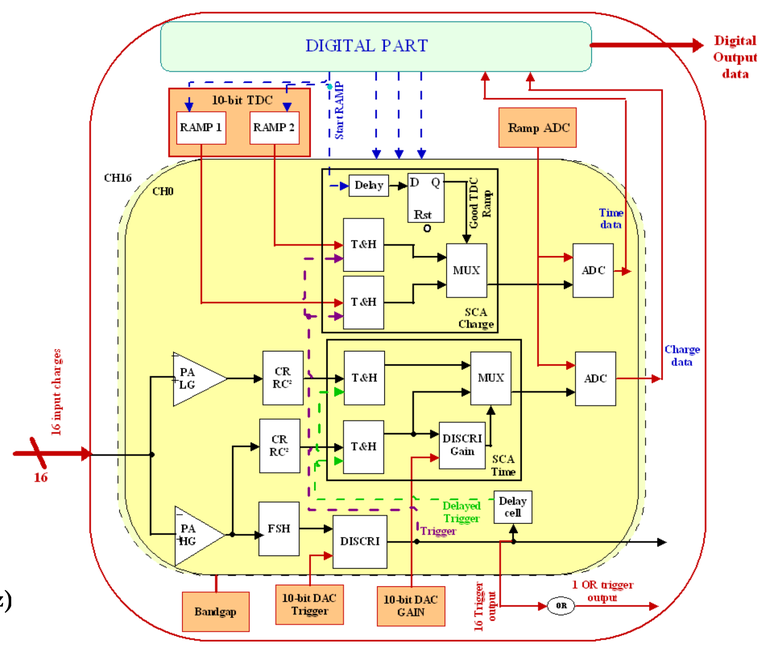
Trigger channel:
- ➢ Fast shaper (t= 5ns);
- ➢ Low offset discriminator;
- ➢ Threshold provided by common 10-bit DAC (1/3 p.e./50 fC);
- ➢ "OR" of 16 triggers output.

Charge channel:
- ➢ Slow shaper CRRC2 with variable shaping time (t= 50ns, 100ns, 200ns);
- ➢ SCA with depth 2 (C = 0.5 pF)

Charge and fine time measurement :
- ➢ 10 bit Wilkinson ADC;
- ➢ T&H on slow shaper for charge measurement;
- ➢ T&H on TDC ramp (100 ns) for fine time measurement;
- ➢ Coarse time measurement : timestamp with 100 ns step (10 MHz)

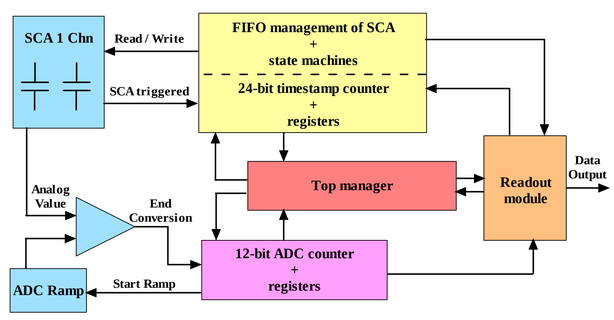
Serialization of digital output information

Architecture



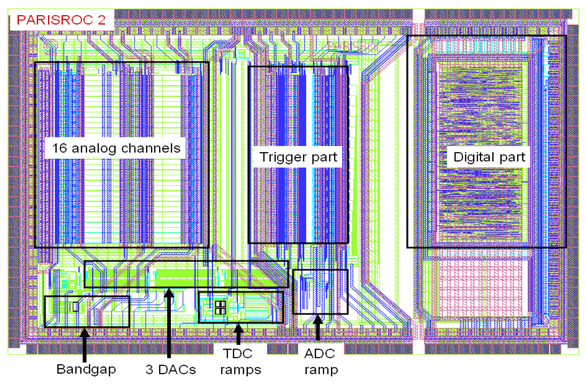
Digital Part

Digital architecture :
- SCA management of 16 channels independents;
- SCA management with depth of 2 for time and charge;
- SCA management like FIFO (ping-pong);
- Timestamp 24b +1b counters @ 10 MHz (1.67s)
- 40 MHz clock for ADC + SCA management + readout



Working overview :
- Only hit channels are readout
- Readout clock : 40 MHz
- Max Readout time (16 ch hit) : 25 µs
- 51 bits of data / hit channel (all gray)

Measurements

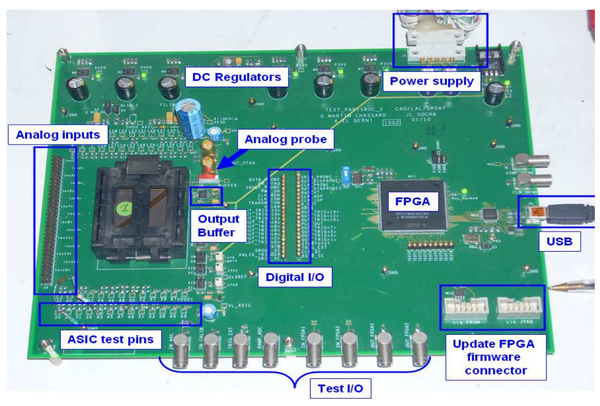


PArISROC layout in AMS SiGe 0.35µm

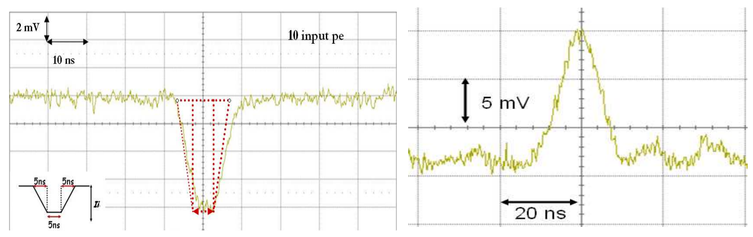
Chip area : 17 mm² (5mmx 3.4mm)

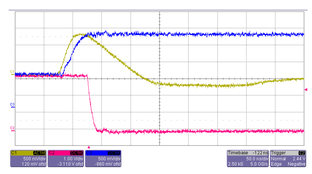
Submitted November 2009 and received in February 2010

Test board



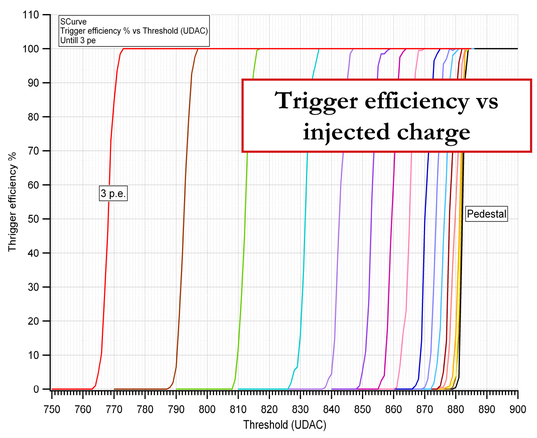
Analog part test

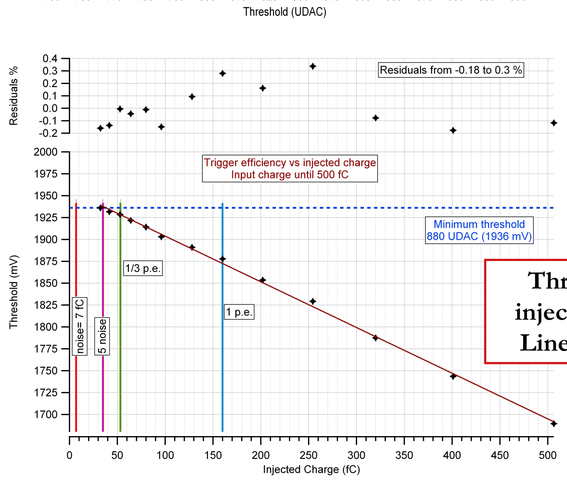




1 p.e. = 160 fC At PMT gain 10^6	PREAMPLIFIER	SLOW SHAPER	FAST SHAPER
GAIN (mV/ p.e.)	12 mV/p.e.	6 mV/ p.e.	78 mV/ p.e.
NOISE (p.e.)	1 mV	1 mV	3.4 mV
SNR	12	6	23

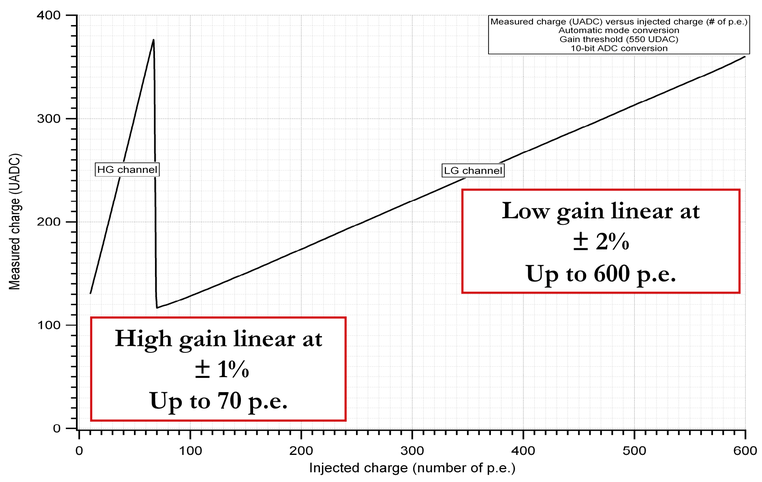
Trigger efficiency



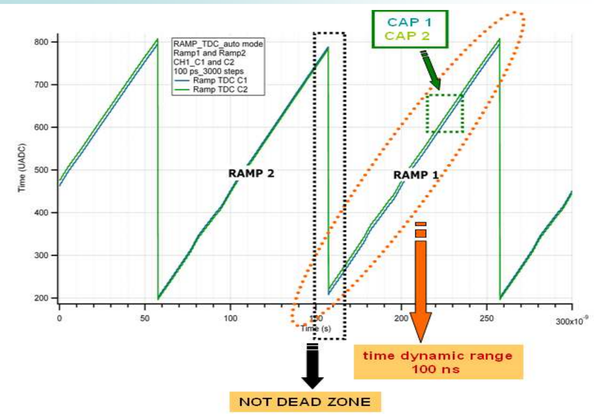


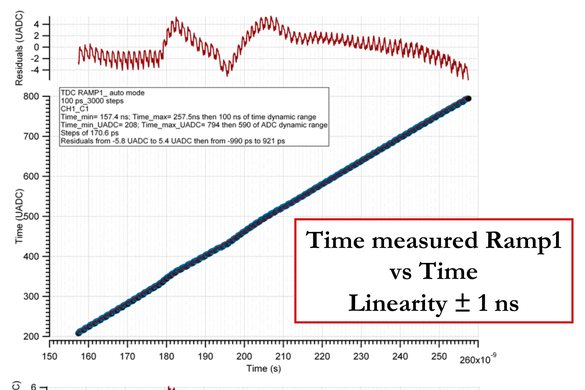
Threshold vs injected charge Linear at 0.3%

Charge measurements

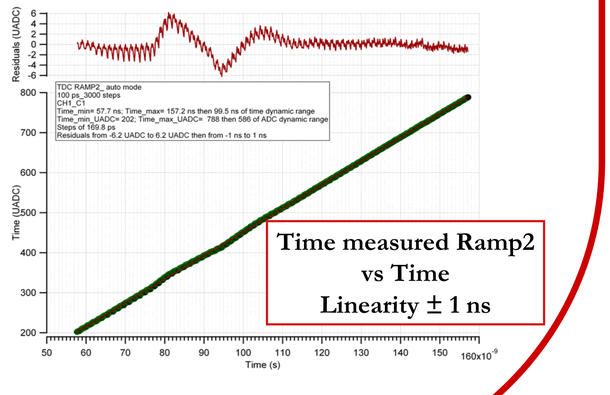


Time measurements



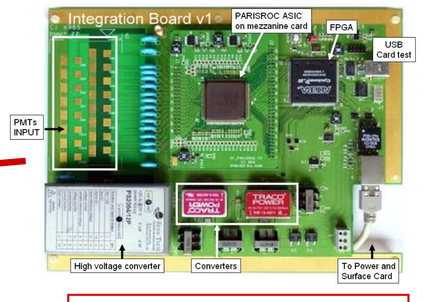


Time measured Ramp1 vs Time Linearity ± 1 ns

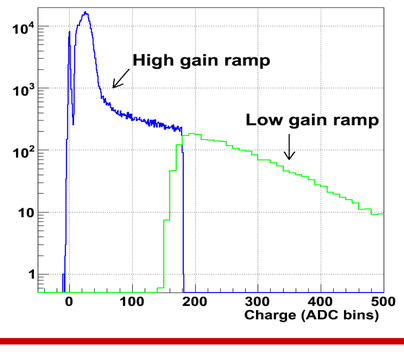


Time measured Ramp2 vs Time Linearity ± 1 ns

PMT measurements



8-in (Hamamatsu R5912) single p.e. noise spectrum. Blue: high gain channel; Green: Low gain channel.



8-in (Hamamatsu R5912) Single p.e. noise spectrum.