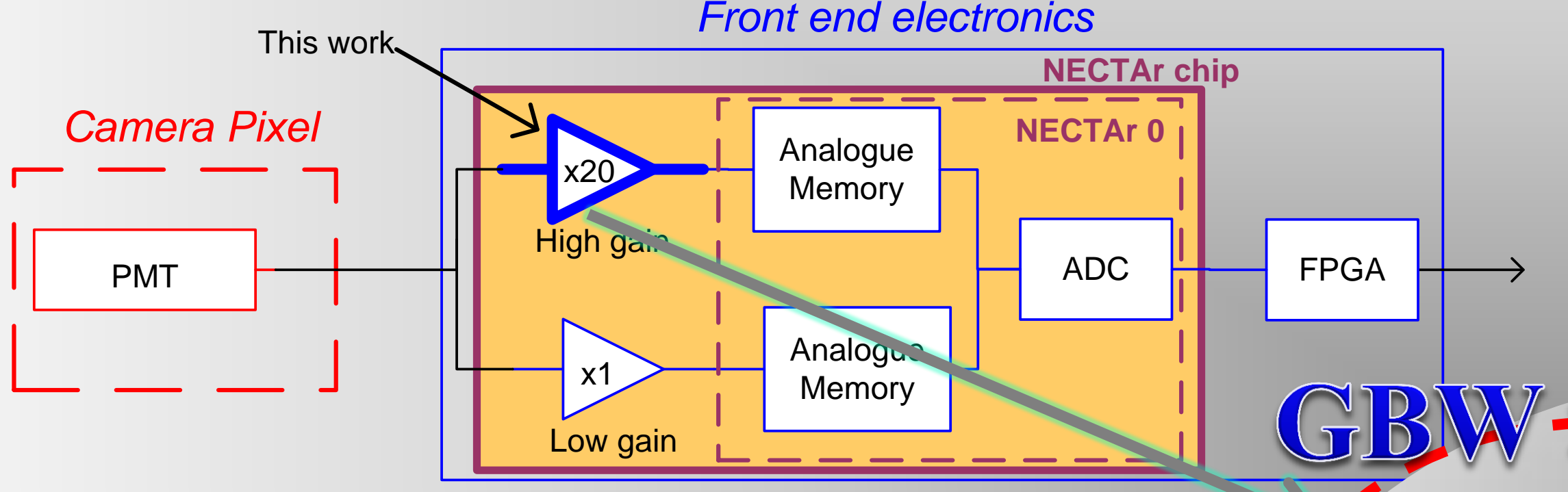


Abstract NECTAr collaboration FE option for the camera of the CTA is a 16 bits and 1-3 GS/s sampling chip based on analogue memories including most of the readout functions. Here we describe the input amplifiers of the NECTAr ASIC. A fully differential wideband amplifier, with voltage gain up to 20 V/V and a BW of 400 MHz. Being impossible to design a fully differential OpAmp with an 8 GHz GBW product in a 0.35 CMOS technology, an alternative implementation based on HF linearised transconductors is explored. The output buffer is a class AB miller operational amplifier, with special non-linear current boost.

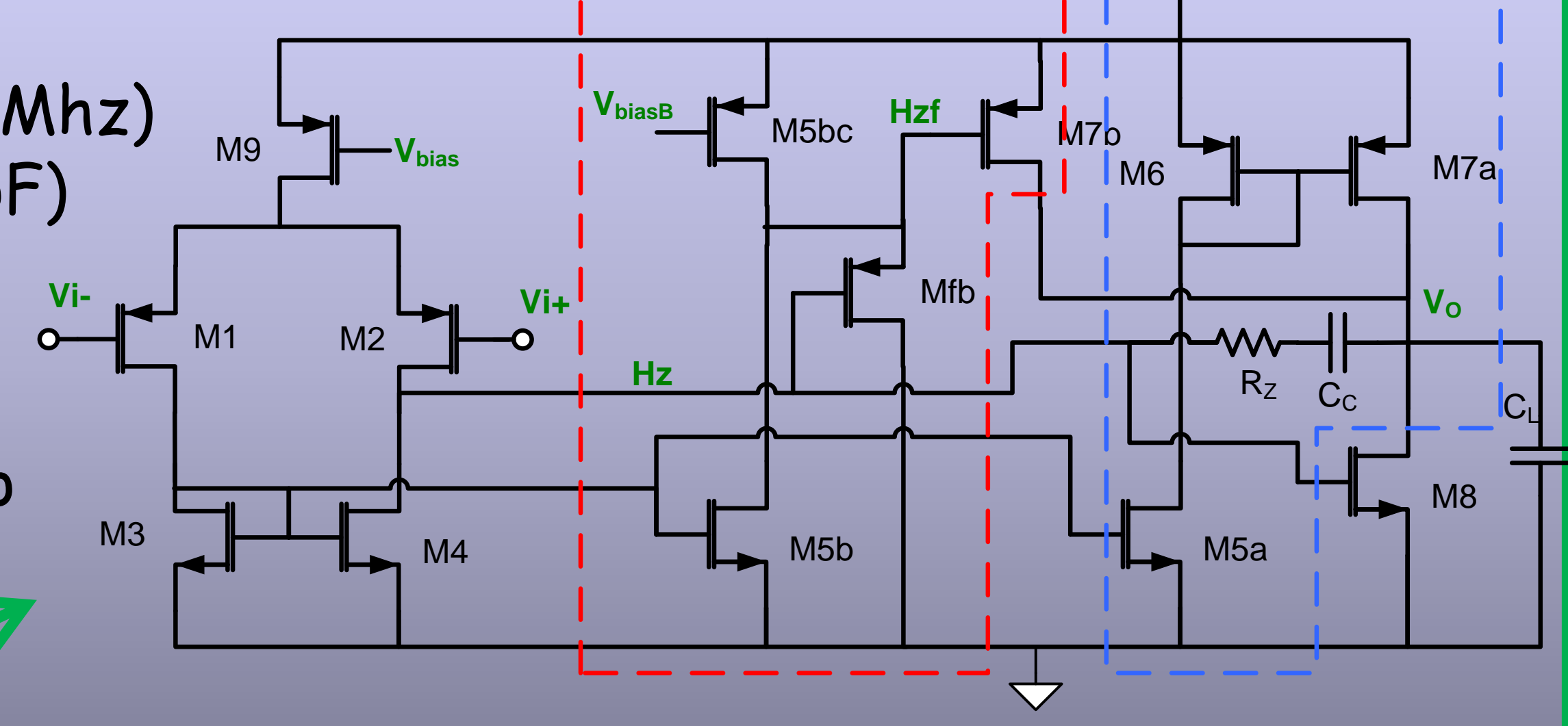
NECTAr :New Electronics for the Cherenkov Telescope Array (CTA)

- Front end electronics of the camera of CTA
- Single GHz sampling chip : analogue memories
- Digitization at >1 GS/s & 16 bits : > 300 MHz BW



- Unity gain wideband follower (500 Mhz)
 - Large capacitive loads (up to 5 pF)
 - Slew rate of about 1 V/ns
- Power consumption of 1 to 3 mW
- Applications
 - Output stage of the gain 20 amp
 - Input buffer of NECTAr0 SCA

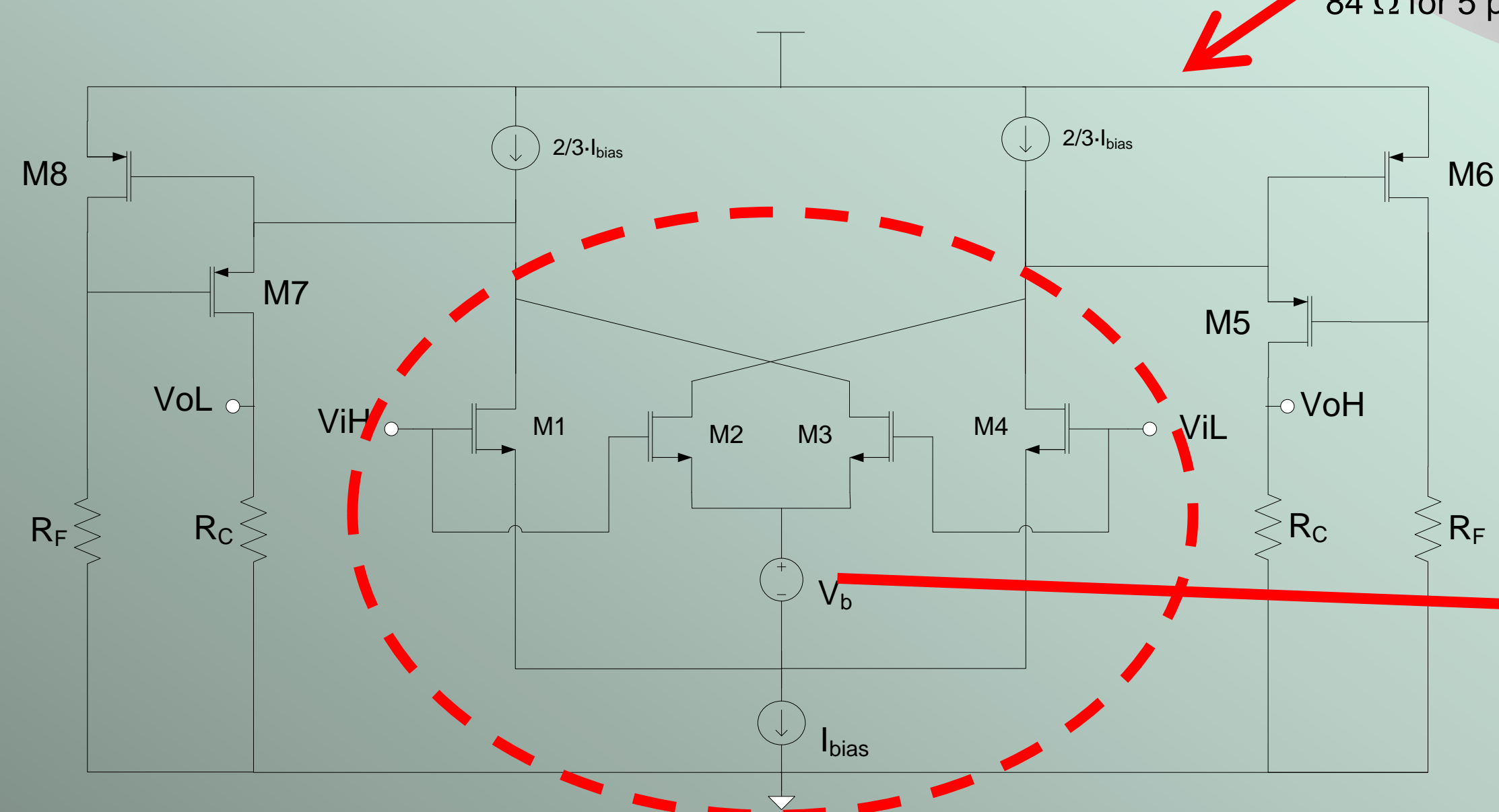
Output buffer



GBW > 6 GHz !

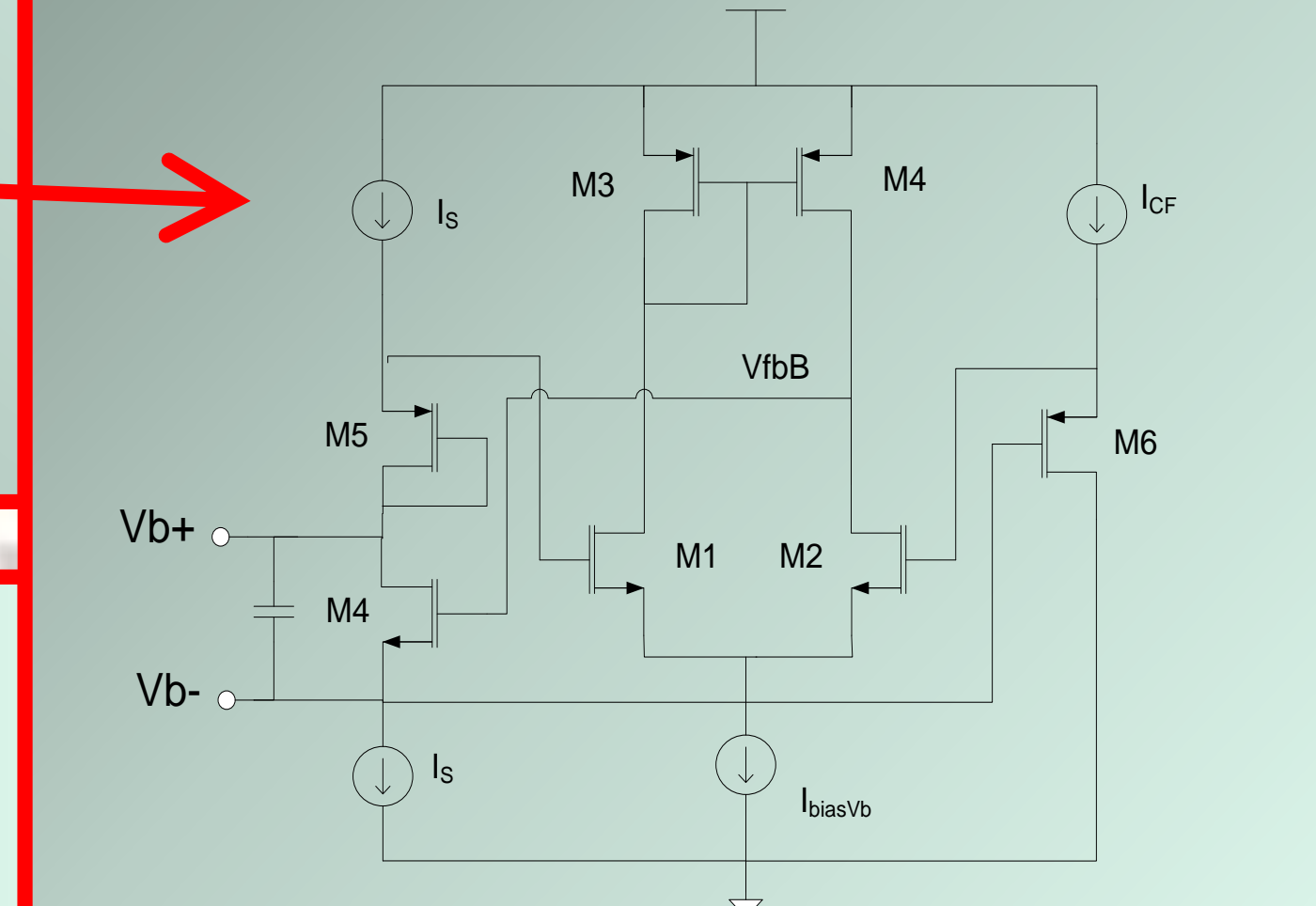
Gain block

- Fully differential 400 MHz BW amplifier
- Voltage gain: 5 to 20 V/V
- Based on HF linearised transconductors



Floating voltage source

- Bias voltage is offset in Vgs of two matched PMOS
- Neg. feedback to ↓↓ r_{out}

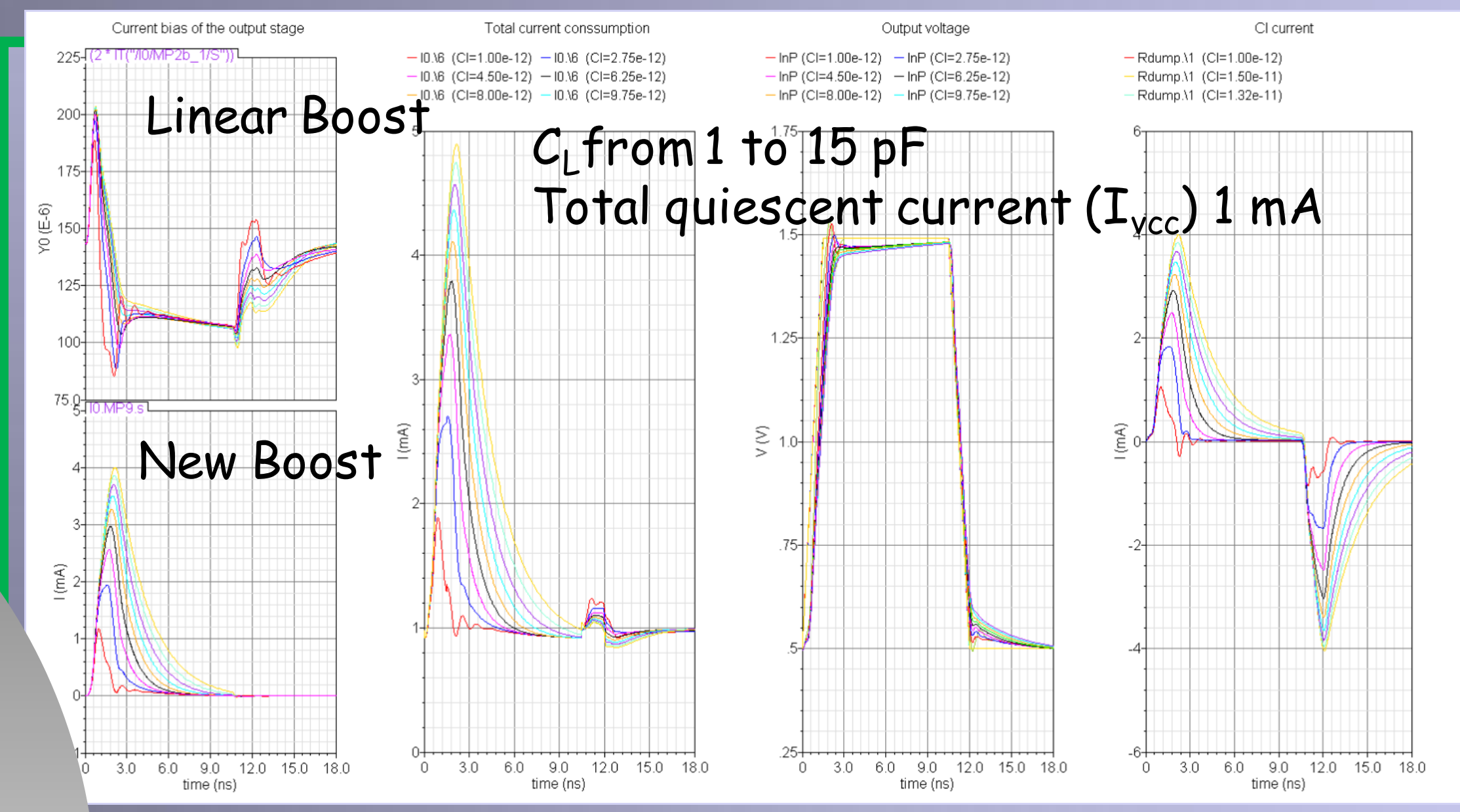


Bias-offset cross coupled differential pair

- Linear transcond. $I_{oD} = KV_b V_{iD}$ $K = \frac{1}{2} \mu C_{ox} \frac{W}{L}$
 - First order:
 - Linear using square law MOS: saturation $\rightarrow |v_{in}| \leq \sqrt{\frac{I_{bias}}{K} - \frac{3}{4} V_b^2} - \frac{V_b}{2}$
 - Tuneable gain
- Second order effects on linearity
 - Channel length modulation \rightarrow Control V_{DS} variations
 - Mismatch \rightarrow Large WL and common centroid
 - Mobility reduction \rightarrow Scaling M1-4 vs M2-3 (for a given G_m)
 - Body effect \rightarrow Cannot use PMOS (large K needed)

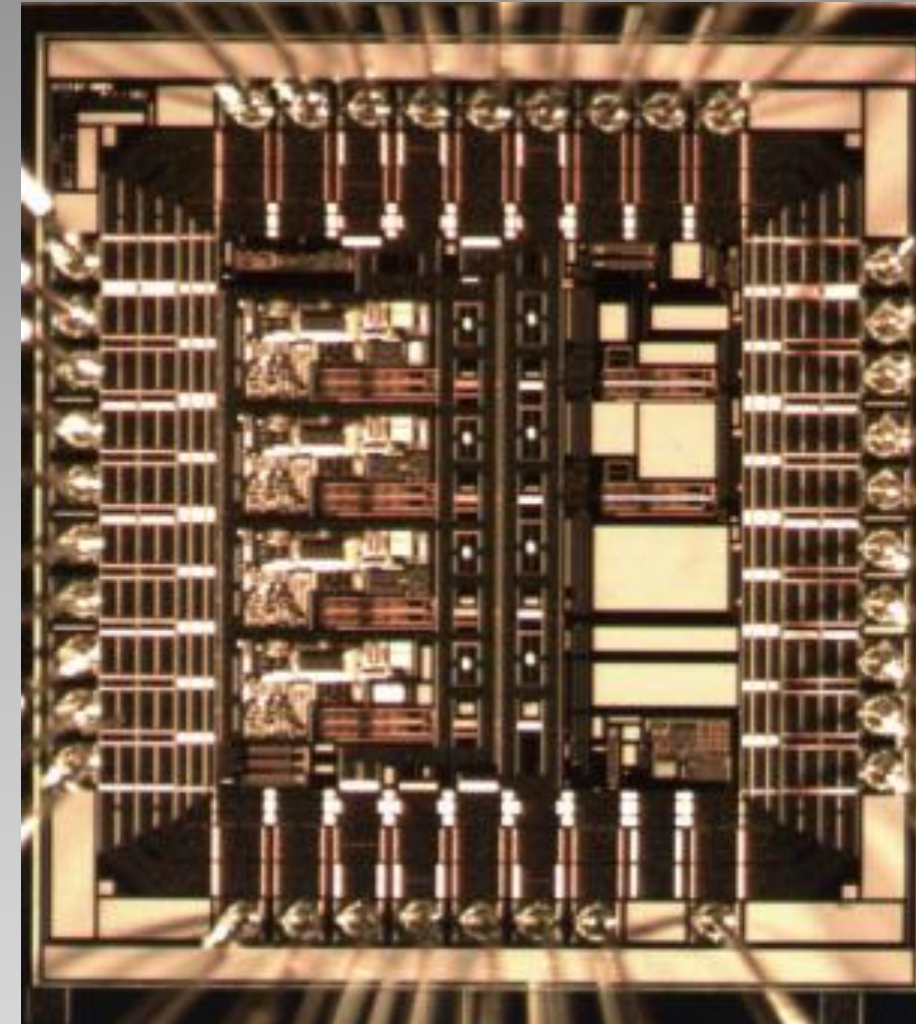
Two current boost circuits: class AB and class B

- Linear class AB moderate (120 uA x 2) boost: SAM chip
- New class B boost current sourcing to load through M7b
 - Follower configuration: when Vi+ increases very fast
 - Non linear transient : Vi- < Vi+ so HZ node ↓↓
 - Negative feedback by Mfb transistor:
 - Copy small signal variation in node HZ to the gate of M7b (Hzf)
 - When HZ node ↓↓ the current in M7b ↑↑ : speed up C_L charging
 - Vi- ↑↑ and HZ node ↑↑
 - Mfb is controlled by a non-linear biasing circuit:
 - VbiasB is such M7b is off at quiescent state
 - When Vi- << Vi+ : M1 takes the diff pair current
 - So M5a(b) current increases subtracting M5bc current
 - Vgs of Mfb increases: Hzf increases: class B enhanced by fb
- Provides up to 4 mA peak current (total Iq 1 mA)



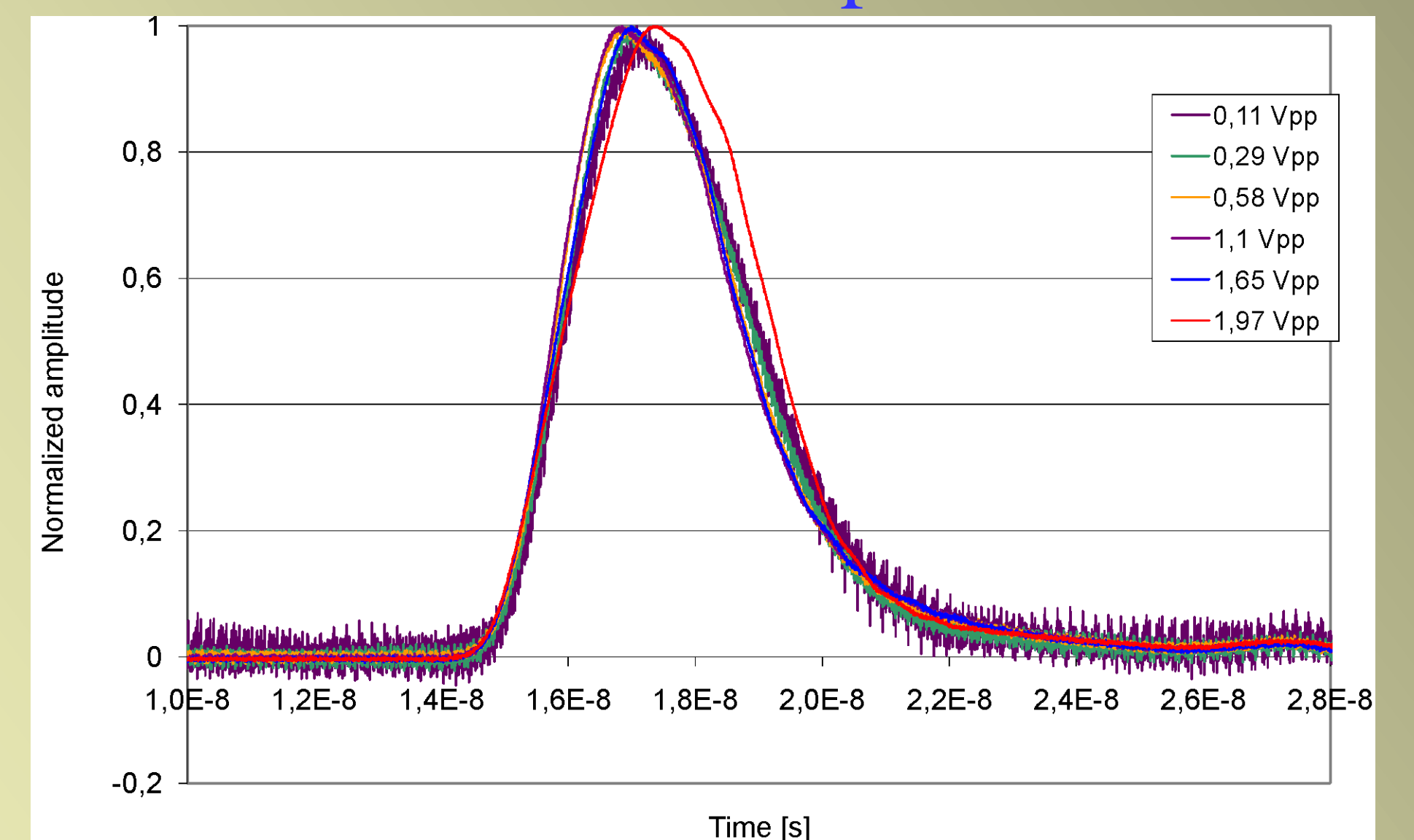
Measurement results

Parameter	Value	Units	Comments
Gain	5 to 20	V/V	Tuneable (through I _{cf} and I _{bias})
BW	400	MHz	C _L =3-4 pF. Extrapolated from B01
Slew Rate	1 to 1.5	V/ns	For 3-4 pF load (tuneable OpAmp bias)
Linearity (VoD<1Vpp)	< 1	%	Depends on I _{cf} and I _{bias}
Linearity (VoD<2Vpp)	< 3	%	Depends on I _{cf} and I _{bias}
Input ref. noise (e _n)	< 3		For gain > 5
DC offset (output)	0 to 1.5	V	Tuneable by control current (I _{bof})
Gain Temp. Coef. (TC)	0.06	%/C	After temp. compensation via TC of I _{cf}
Power consumption	20 - 30	mW	

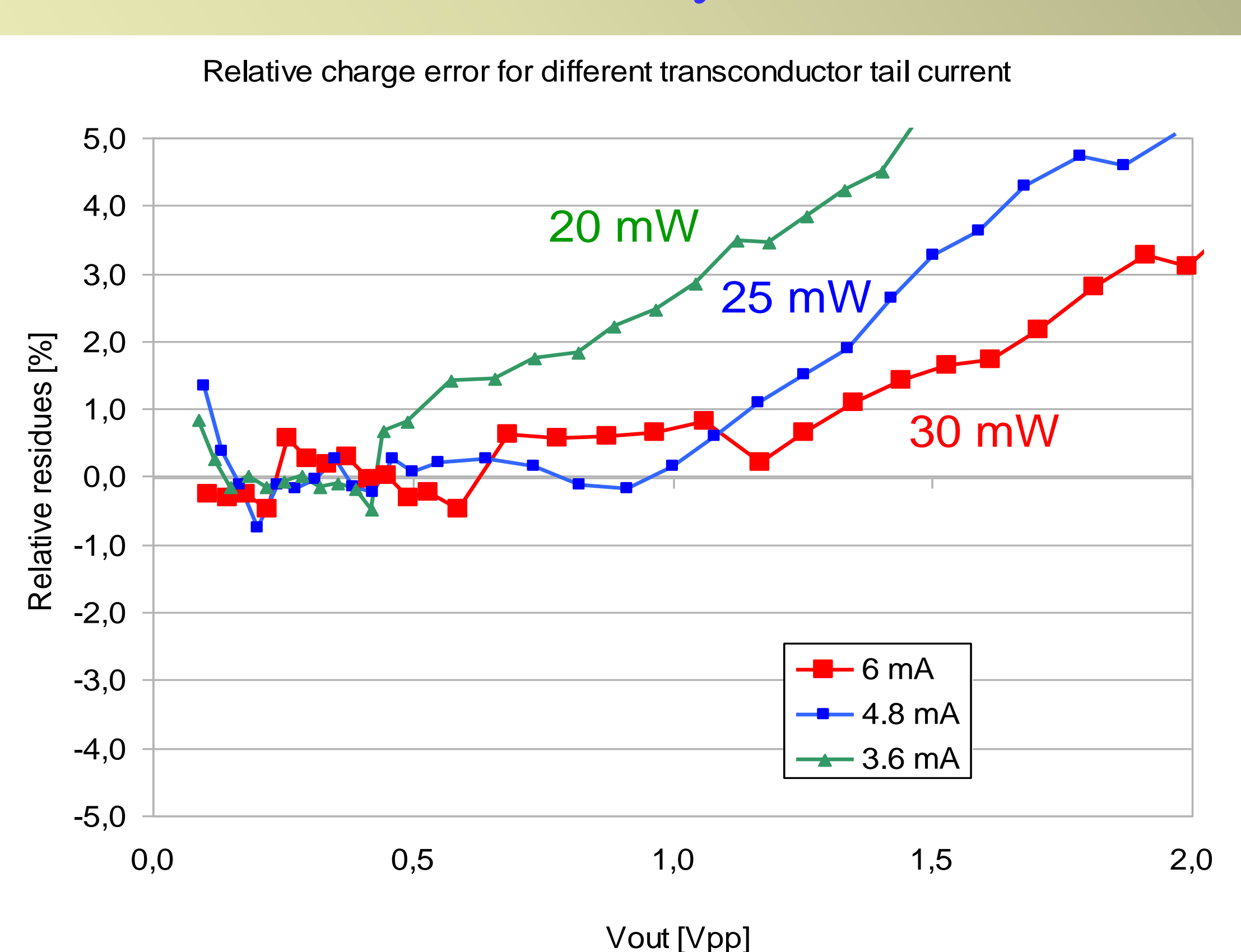


ACTA3
4 ch
CMOS
0.35um
AMS
3 mm²

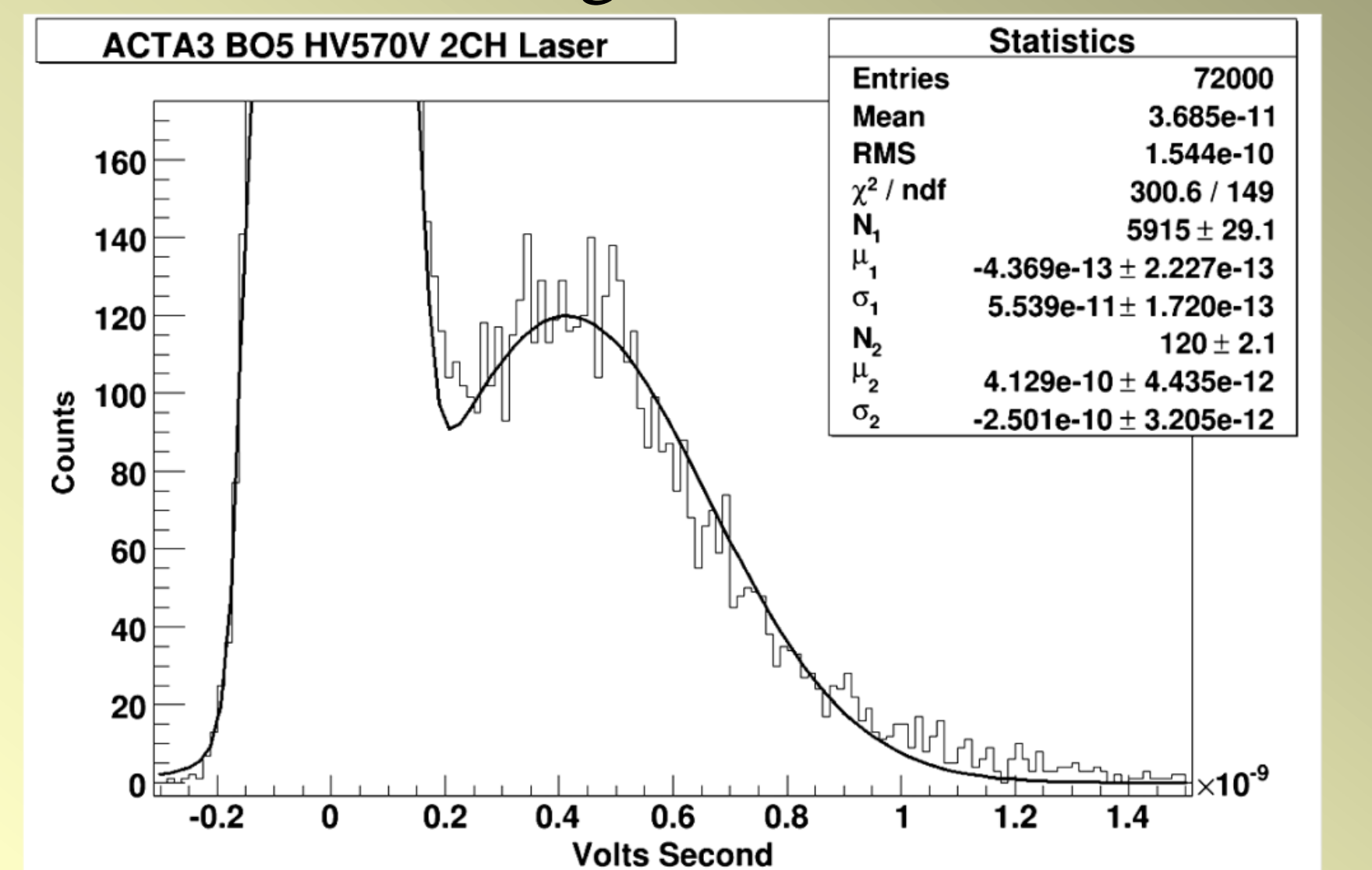
Pulse shape



Linearity



Single photoelectron spectra



Frequency response

