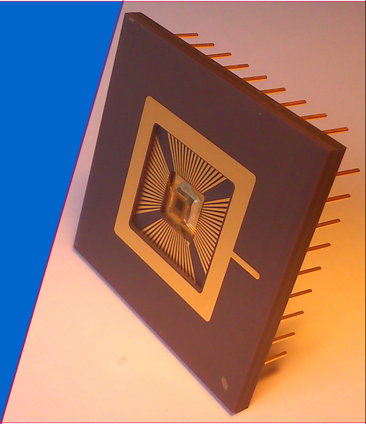
Low light electron multiplying image sensors modeling and characterization :

Study of the EMCMOS concept

Timothée Brugière



NDIP 2014 - 30 juin 2014

Groupe ebCMOS

Why low flux ?

Fast detection

- Acquisition frequency
- Very short integration time (less than 10 ms)
- Low number of photons per frame

Low flux

Few ($\sim$ 1 to 10) photons per frame and per pixel

- Maximization of the number of detected photons :
  - Quantum efficiency
  - Fill factor → Micro-lens
- Minimization of noises :
  - Charge transfer
  - Dark current → Cooling
  - Read noise : → Correlated Double Sampling (CDS)
    → Low noise readout
    → Charge multiplication

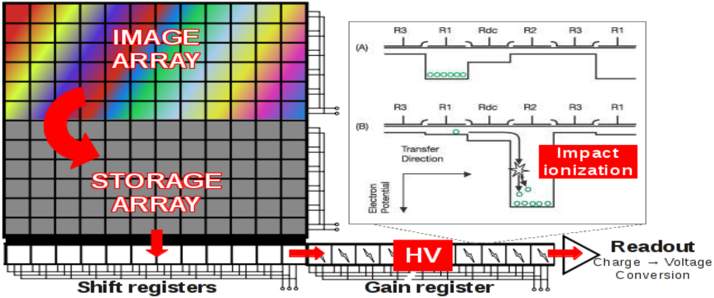
How to make imaging with low fluxes ?

Existing devices : sCMOS, EMCCD, ebCMOS, ...

Limitations : Frame rate, Matrix size, Power consumption, Cooling, Read noise

sCMOS
- No charge multiplication, Read noise : $\sim 1e^-$

EMCCD
- Effective readout noise : $\sim 0.1e^-$
- CIC noise («Clock-Induced Charge») in shift registers
- Power consumption, cooling, slow frame rate, smearing

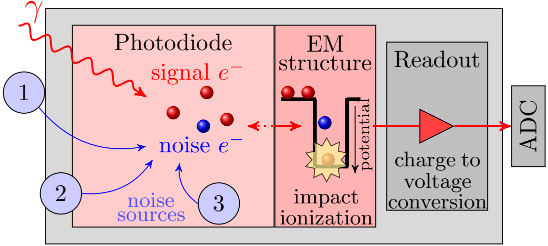


The EMCMOS concept

EMCMOS

- In-pixel charge multiplication → no CIC noise expected
- "System-on-chip" → compactness
- Low power consumption
- Large dynamic range, no smearing
- Implementation in mature technology → Reliability and cost

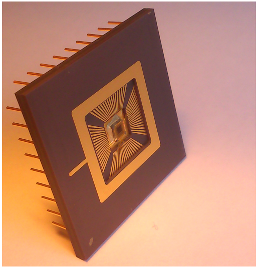
EMCMOS Pixel



Noise sources :

1. Band-to-band tunneling
2. STI (Shallow trench isolation) and metal oxides
3. Thermal generation

The MULTIMOS project



Production of EMCMOS prototypes

- E2V Saint-Egrève (France, Isère)
- Design / Technological variants

  ~ 200 distinct pixel structures

  ~ 120 control parameters

Characterization of the in-pixel multiplication

- Modeling

  EMCMOS original sequencing
- Optical benches and Acquisition card
- Acquisition and Analysis softwares

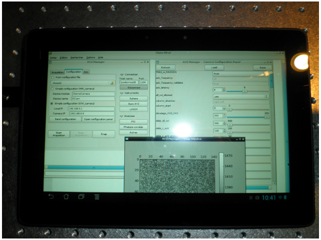
  Automation, quick view of results
- Sequencing, operating point
- Study of in-pixel impact ionization

  Parameter α

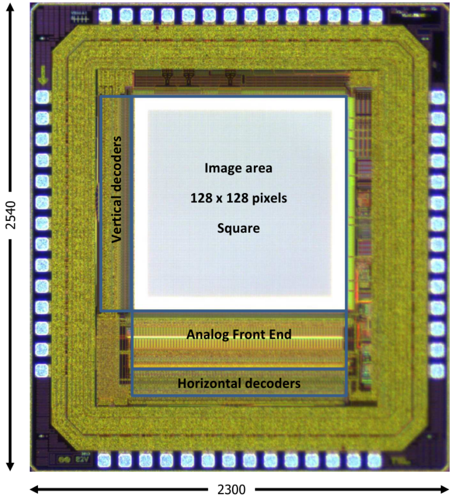
Imaging with EMCMOS

- SNR, QE, PSF, ...

  On-going

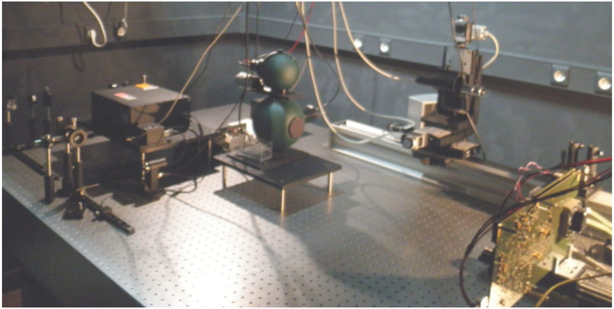


EMCMOS chips by E2V



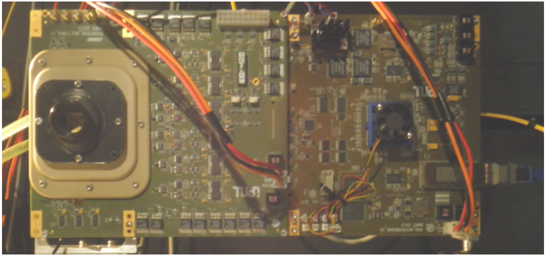
- CMOS analog circuitry
- Differential analog front end (AFE)
  CDS, Column FPN rejection
- Electronic Rolling Shutter (ERS) and Global Shutter (GS)
- Pitch : 8 μm
- Off-chip adjustable gain and 12-bits ADC

Characterization set-up at IPNL



3 optical benches

- Flat field
  PTC, QE, ...
- Focused source
  PSF
- Correlated photons
  QE

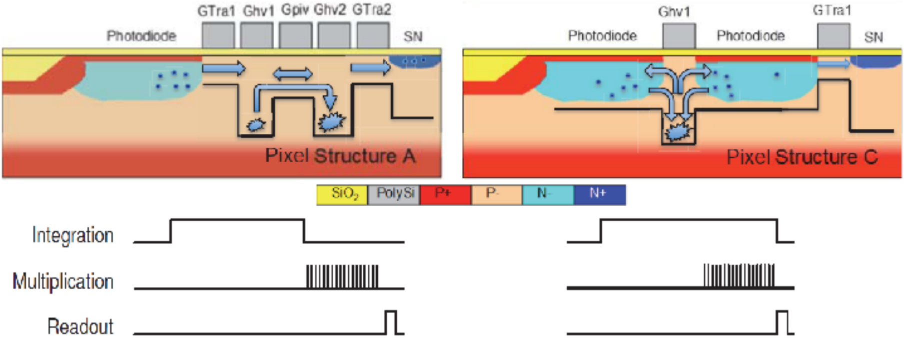


Acquisition card

- Power sup., Bias cur.
- FPGA
  Sequencing, 120 par.
- 10Gb/s Ethernet
- Cooling, C-mount

EMCMOS pixel structures

Multiple possible designs (Sanyo / E2V patents) :



- Multiplication cell separated from the photodiode

  Multiplication occurs AFTER the integration

- HV gates integrated within the photodiode

  Multiplication occurs DURING the integration

EMCMOS modeling

Impact ionization :

- Stochastic, $\alpha(E) = \frac{\gamma}{Z(E)} e^{-\beta/E}$
- Excess Noise Factor (ENF)

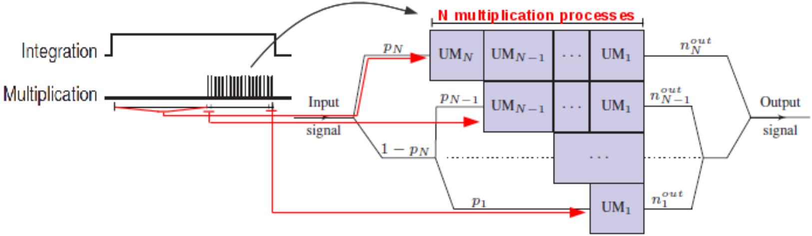
Previous works :

- Van Vliet (1979), Hollenhorst (1990)
- Multiplication AFTER the integration

A theory of multiplication noise for electron multiplying CMOS image sensors

T.Brugière, F. Mayer, P. Fereyre, A. Dominjon, R. Barbier
published in *IEEE Transactions on Electron Devices*

Generalized modeling :



- N contributions to the output signal
- Probability Generating Functions (PGF)
- Response to 1 electron → contributions are not independents **(Categorical distribution)**

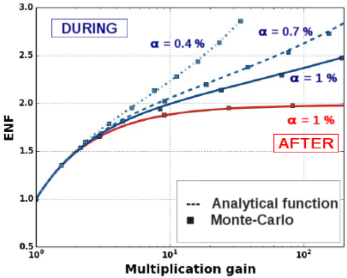
EMCMOS modeling

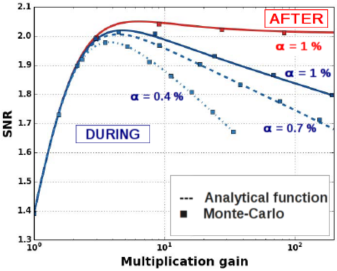
Output signal :

$$\sigma^2_{n^{out}} = \langle m^{eq}\rangle^2 \sigma^2_{n^{in}} + \underbrace{\left\langle n^{in}\right\rangle \left(\sum_{i=1}^{N_c} p_i \sigma^2_{m_i^{eq}} + \sum_{i=1}^{N_c} p_i \left(\langle m_i^{eq}\rangle - \langle m^{eq}\rangle\right)^2\right)}_{\text{Excess noise}}$$

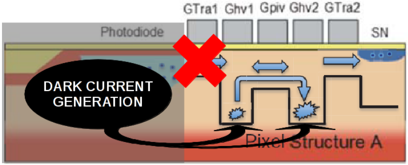
Excess noise factor :

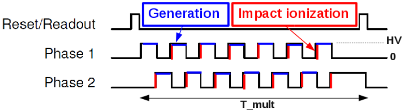
$$ENF = 1 + \frac{EN_{\varphi} + EN_{TPN}}{\langle m^{eq}\rangle^2 \sigma^2_{n^{in}}}$$





Multiplication test structure

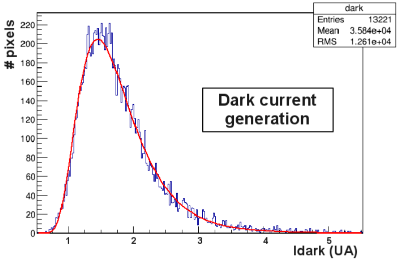




- Structures without photodiode
- Dark current generation under HV gates used as source

  Generation of e^- DURING the multiplication
- Generation boosted by heating
- Input signal $\propto$ multiplication time

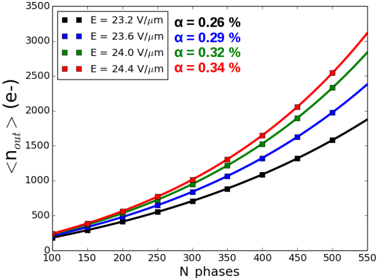
  Integration and multiplication fully overlapped

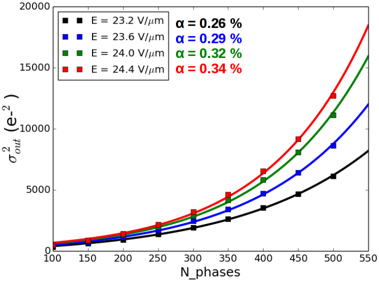


- Dark current generation

  Log-normal distribution over the matrix
- Flux driven by temperature

Results on test structures





Data :

- Data taking at multiple HVs
- Conversion factor from PTC analysis

CVF $\sim$ 80 μV/e^-

Model :

- Multiplication → Bernoulli
- Source → Poisson

$\langle n_{in} \rangle = \sigma^2_{in}$

Results :

- Fit output signal with the modeling

$\alpha = 0.32\%$ at E $= 24$ V/μm

- Limitation from test structures
- To be compared to values extract from full structures

On-going

Conclusion

- Automated acquisition and analysis
  Fast characterization of a chip
- EMCMOS Modeling
  Formula validated by Monte-Carlo simulation
  EMCMOS + generation during multiplication for other devices
- Modeling validation by comparison with real data
  Mean output signal and associated expected variance
- Validation of the impact ionization implementation in a $8-\mu$m pitch pixel

What next ?

- Study of full structures : On-going
- Imaging with EMCMOS

THANK YOU