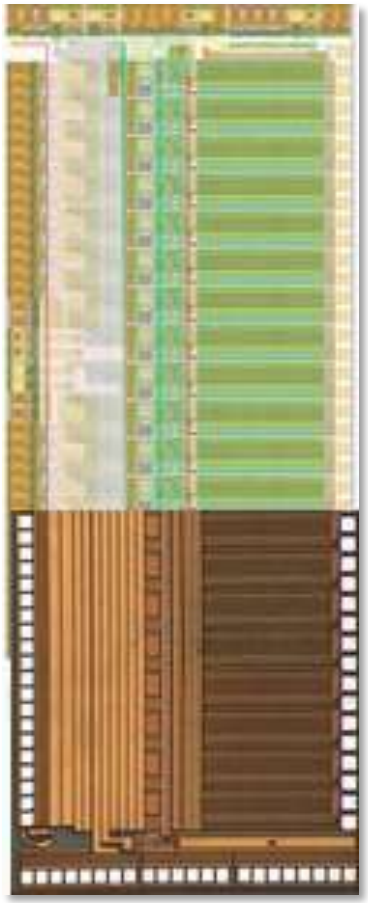
REACHING A FEW PS PRECISION WITH THE 16-CHANNEL DIGITIZER AND TIMESTAMPER SAMPIC ASIC



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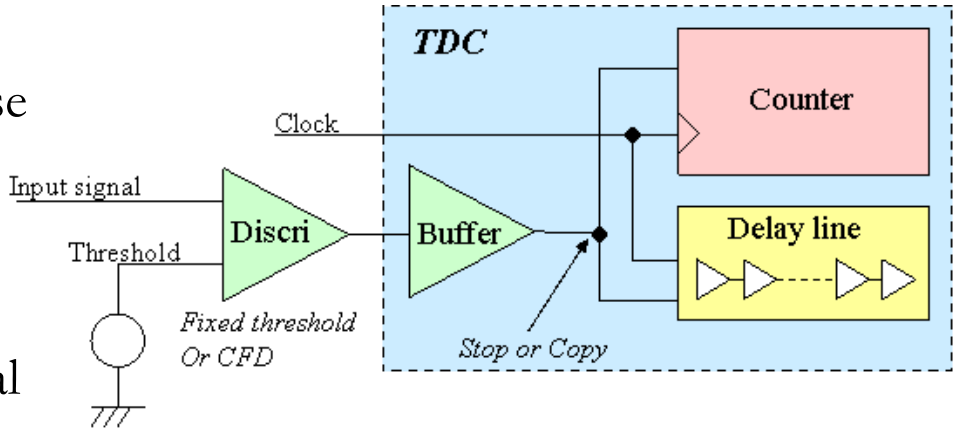
A FEW COMMENTS ABOUT PURE TDCs

Current most advanced TDCs use digital counters (coarse) and Delay Line Loops (DLLs) (fine):

- They can be implemented in **ASICs or FPGAs**
- **Interleaving and other tricks** increase the precision
- Resolution is given by **the DLL step** but precision is usually limited by stability of calibration or environmental effects: limit at ~20ps RMS



BUT a TDC needs a **digital** input signal:

⇒ **analog** input signal has to be translated to digital with a **discriminator**

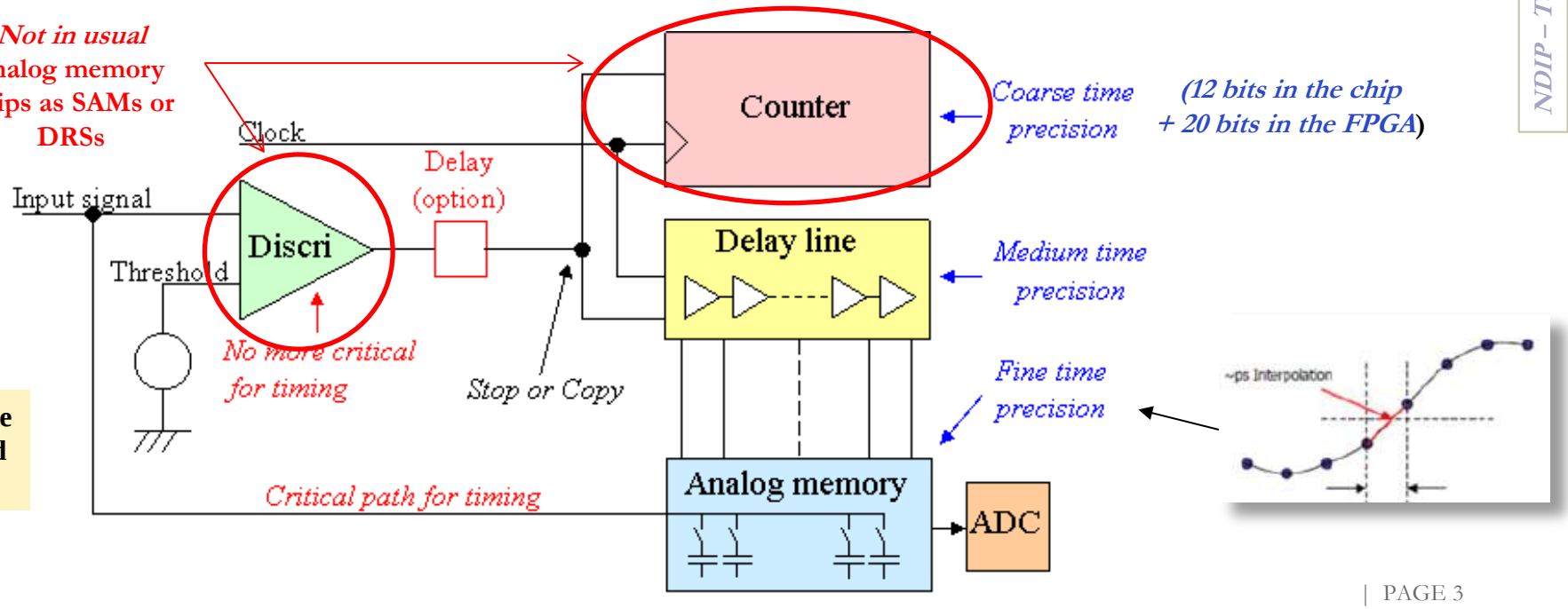
⇒ **additional jitter** and **residues of time walk** effect enter the game

⇒ **overall timing resolution is degraded to the quadratic sum of the discriminator and TDC timing resolutions**

THE « WAVEFORM TDC » STRUCTURE

- **Mix of a TDC and of an analog-memory based Waveform Digitizer**

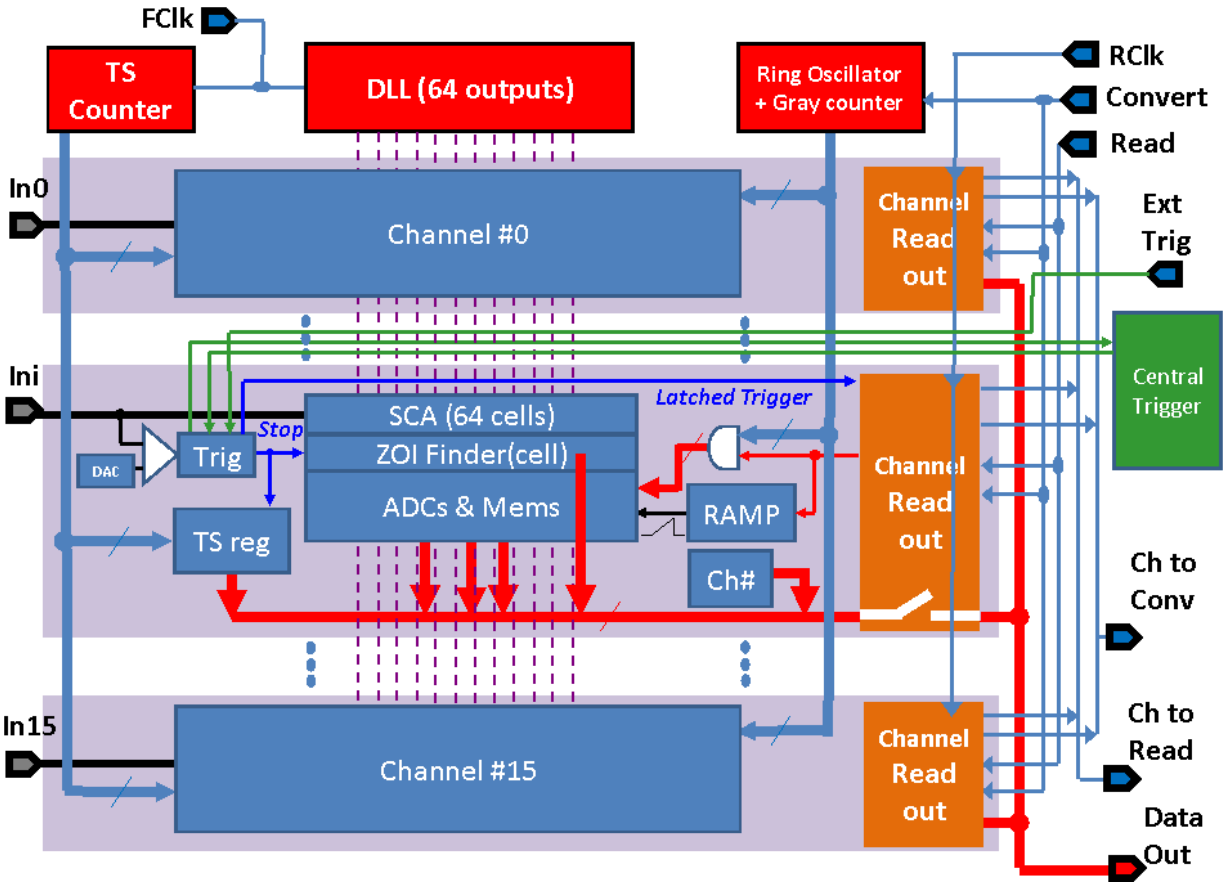
- Time information is given by association of contributions:
  - **Coarse** = Timestamp Gray Counter (few ns step)
  - **Medium** = DLL locked on the clock to define region of interest (100 ps minimum step)
  - **Fine** = samples of the waveform (**interpolation** will give a precision of a few ps rms)
- **Digitized waveform shape, charge and amplitude are available**
- **Discriminator is used only for triggering, not for timing**



Structure patented in 2009

OVERALL ARCHITECTURE

- SAMPIC0 is a prototype to demonstrate the concept, but also to be used in small/medium size setup
- Core of a future dead-time free chip



- **16 single-ended Channels:**
  - ✓Self Triggerable (or Central OR Trigger, or External Trigger)
  - ✓Independent channels
  - ✓ 64 Analog Sampling Cells/Ch
  - ✓One 11-bit ADC/ Cell (Total : 64 x 16 = 1024 on-chip ADCs)

- **One Common 12-bit Gray Counter** (@160MHz) for **Coarse Timestamping**.

- **One Common servo-controlled DLL**: (from 1 to 10 GHz) used for middle precision timing & analog sampling

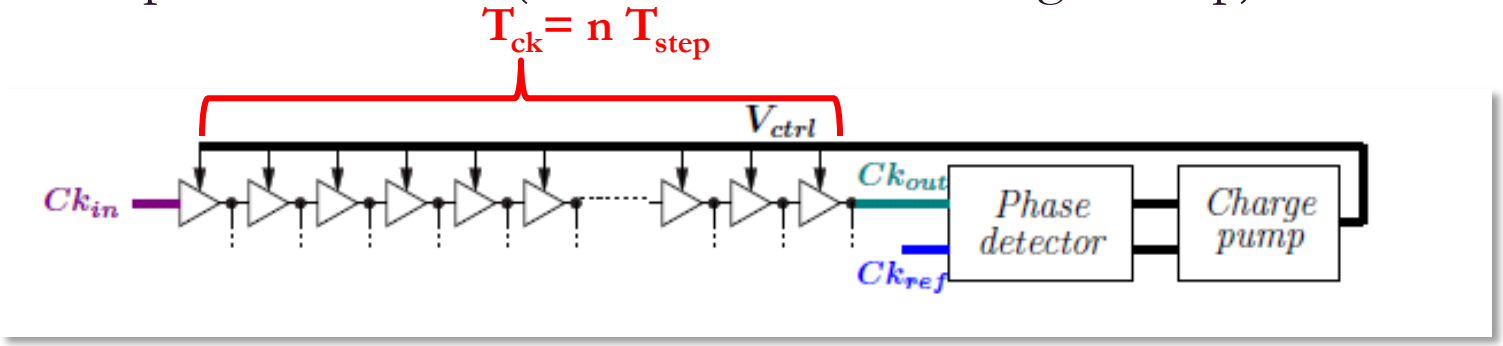
- **One** common **11-bit Gray Counter** running @ 1.3GHz and used for the **parallel Wilkinson AD conversion**.

- 12-bit LVDS **Read-Out Bus** (160 – 400 MHz)

- SPI Link for Slow Control configuration

TIMEBASE

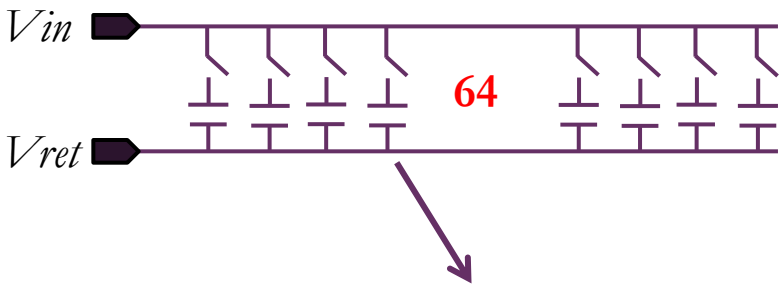
- **One single 64-step Delay Line Loop**
- Locked on the Timestamp counter clock
- On chip servo-control (Phase detector + Charge Pump)

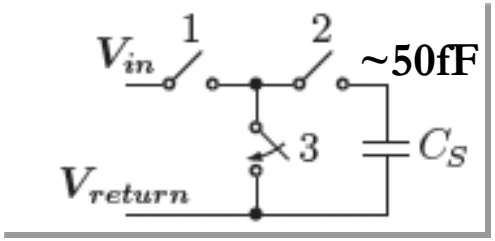


- Provides 64 incrementally **delayed** pulses **with constant width** used to drive the T/H switches of the **64 cells** for **each SCA channel**
- **'virtual multiplication'** by 64 of the TS Clock (100MHz =>6.4GHz)
- T/H signals can be disabled on each channel (stop the sampling)
- Optional low speed mode for sampling < 3 GSPS
- Special focus on ensuring a perfect continuity between last & first cells

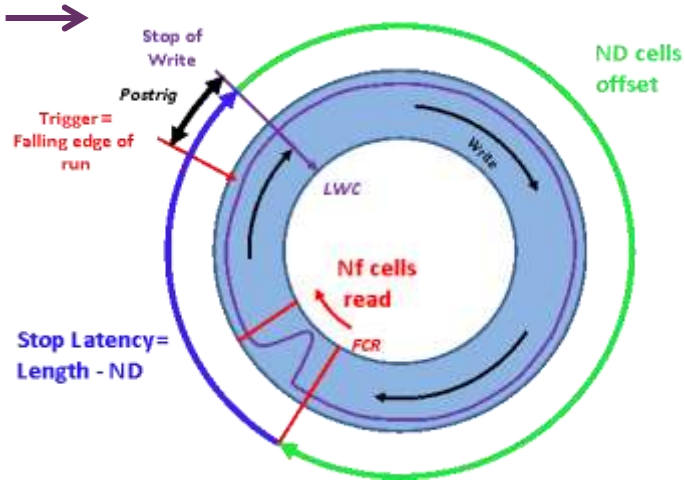
INTERNAL ANALOG MEMORY (SCA)

- **64-cell depth**, trade-off between:
  - Time precision /stability (=> short)
  - Input capacitance (=> short)
  - Bandwidth uniformity (=> short)
  - Time for trigger latency (=> long)





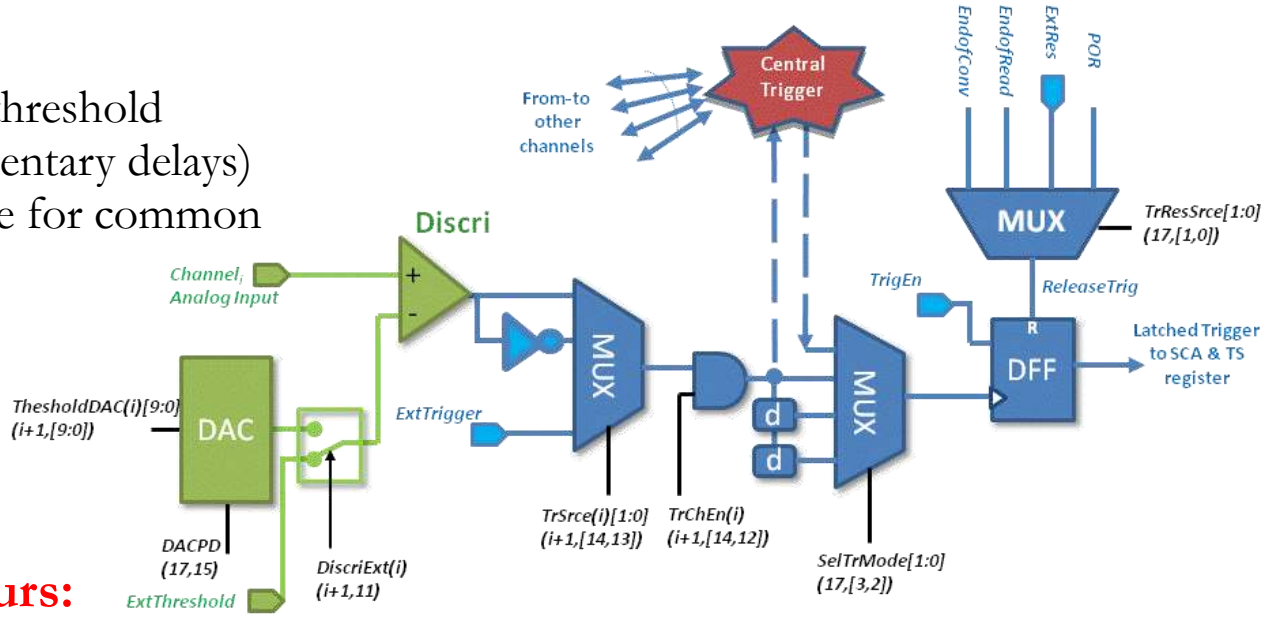
- **No input buffer, single ended**
- 3-switch cell structure to avoid leakages and ghosts. Switch 3 also isolates from input bus during conversion
- **> 1.5 GHz BW**
- **~ 1 V usable range**



- **Continuously writing** until triggering (circular buffer)
- **Post-trigger position marking on DLL cells**
- Optional **Region of Interest Readout** for deadtime minimization

SAMPIC TRIGGERING OPTIONS

- One signal discriminator/channel
- One 10-bit DAC/channel for each discriminator threshold (can be external)
- Several trigger modes programmable for each channel:
  - External
  - "Central" trigger (only OR in this chip)
  - Edge selection
  - Enable/disable
  - Internal/external threshold
  - Postrig (0,1,2 elementary delays)
  - Fast Global Enable for common deadtime

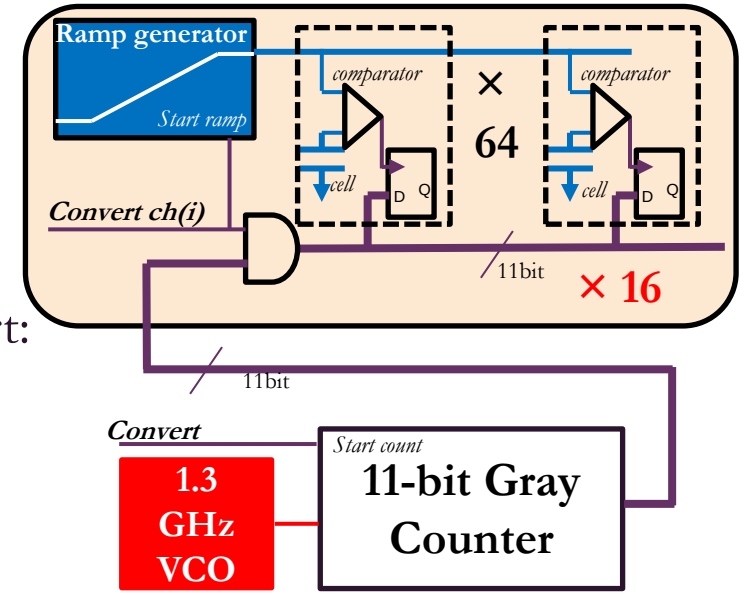


- **When a trigger occurs:**
  - **Sampling in the analog memory is stopped and coarse timestamp is latched**
  - **The chip rises a first flag for the user (FPGA) to start the ADC conversion and once done a second flag to ask for data readout**

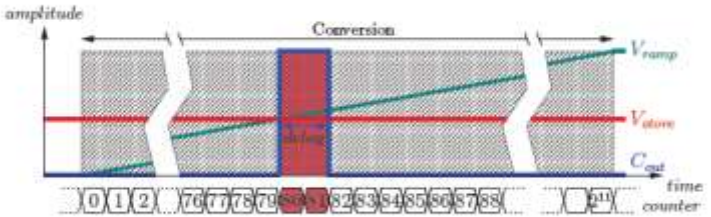
WILKINSON DIGITIZATION (1 PER CELL)

Simultaneous conversion of all the cells of the triggered channels:

- Starts the on-chip 1.3 GHZ VCO
- Starts the on-chip **1.3 GHz Gray counter** and sends its outputs to the channels to convert
- Starts the ramp generators of channels to convert: tunable slope: speed/precision tradeoff
  - **1.6µs/11bit, 400ns for 9 bit…**
  - **Main contribution to the Dead Time**

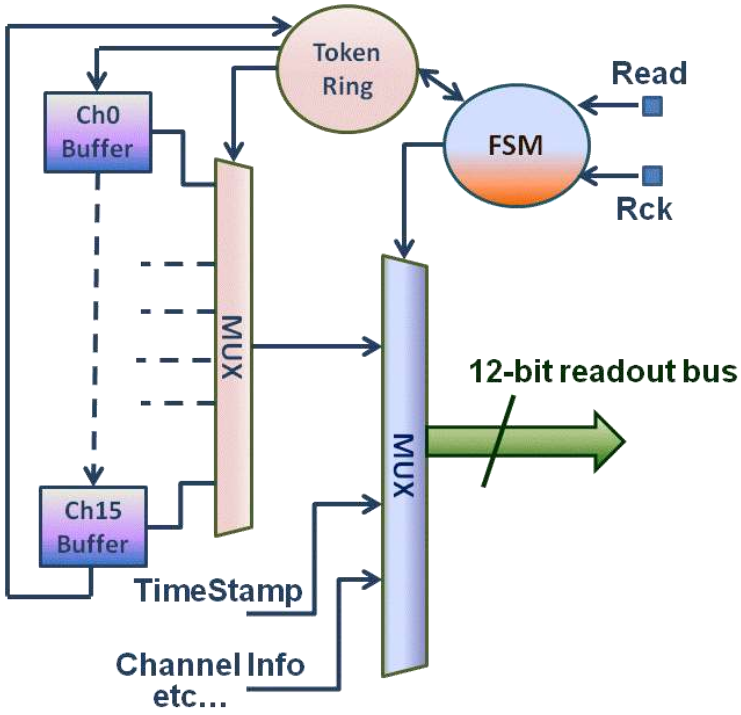


- Enable the **64 comparators** of the enabled channel
- When **Ramp crosses cell value** => the counter stored in a register
- Once converted, a channel is **immediately usable to record** a new event



READOUT PHILOSOPHY

- Readout driven by **Read** and **RCk** signals
- Data is read **channel by channel**
- Rotating **priority mechanism** to avoid reading always the same channel
- **Optional Region Of Interest readout** to reduce the dead time (nb of cells read can be chosen dynamically)
- Readout of converted data through a 12-bit parallel LVDS bus including:
  - Channel Identifier, Timestamps, Trigger Cell Index
  - The cells (all or a selected set) of a given channel sent sequentially
  - Potentially up to 4.8 Gbits/s



- **Channel is not in deadtime during readout, only during conversion (data register is really a buffer stage)**

ACQUISITION MODULE AND SOFTWARE

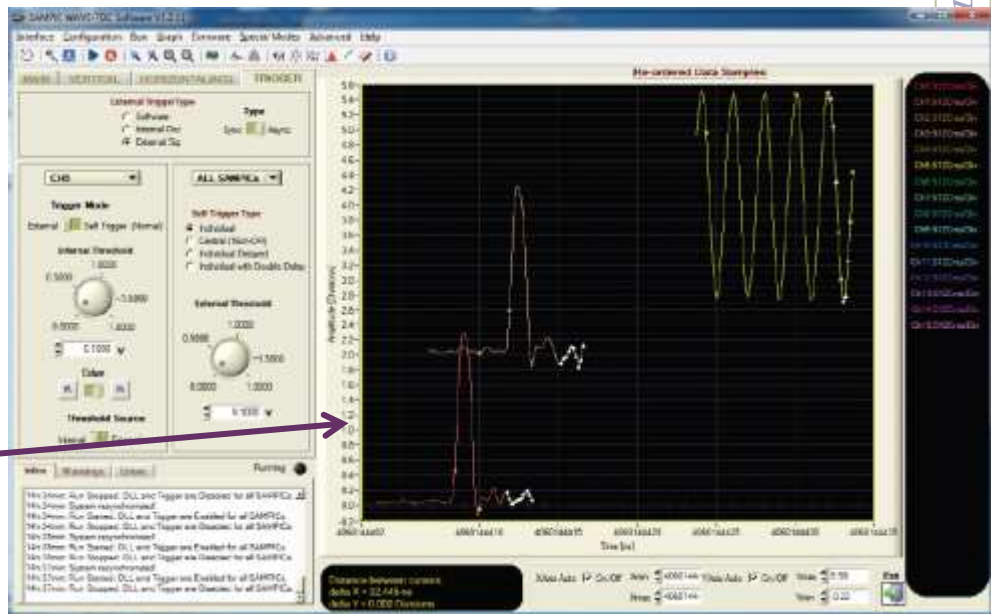
- **SAMPIC module has been designed**
- **Mezzanine board** for 16 channels
- Mother board can hold 2 mezzanines: native **32-channel system**
- MCX input connectors
- **USB** – (Ethernet – Fiber Optic link)
- 5V voltage supply – 1.1 Amp
- 3 modules are currently on duty
- 3 others will soon be available

- **Acquisition software** permits the full characterization of the chip and module
- It is already usable for small size experiments
- **Special visualization** for innovative **WTDC mode**

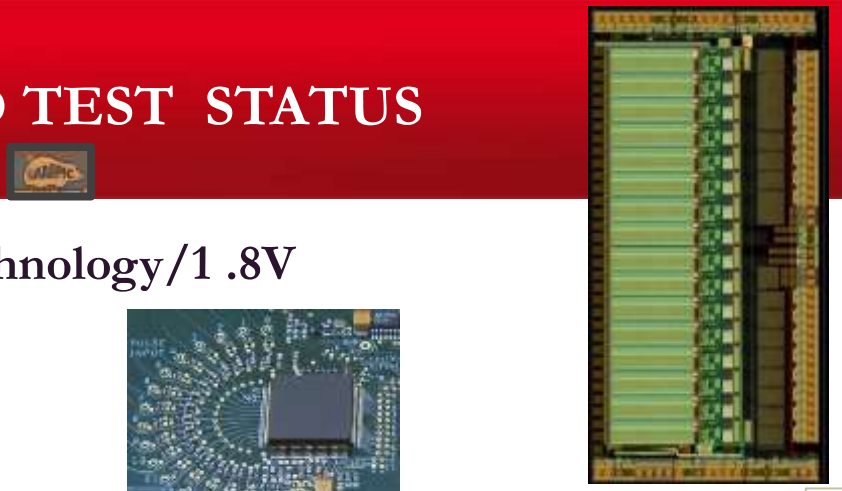
The SAMPIC 16-channel mezzanine

The SAMPIC module

The acquisition software

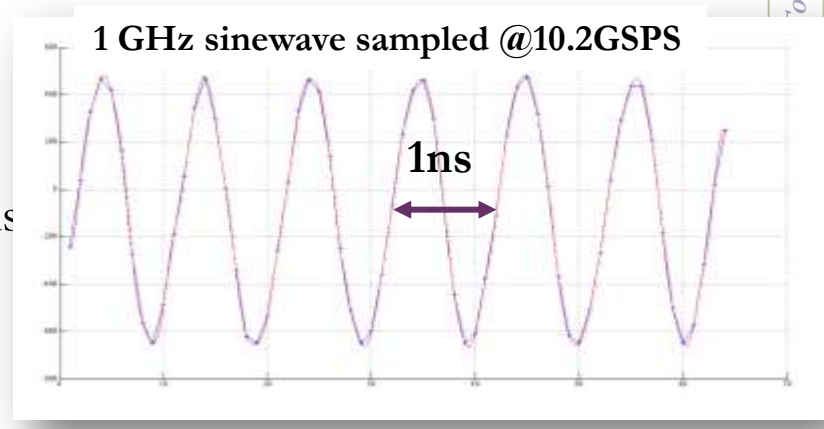


CHIP PROTOTYPING AND TEST STATUS


AMS0.18: 7mm^2

- **Manufactured using AMS CMOS 0.18µm technology/1 .8V**
- **14x14 mm package**
- **Low cost for prototyping : 10kE for 7 mm^2**

- Working smoothly excepted 3 minor bugs which can be easily fixed and that don't prevent to use the chips.
- Sampling is ok :
  - from 3 to 8.2 GSPS on all the channels
  - up to 10.2 GSPS on 8 channels
  - Not tested under 3 GSPS

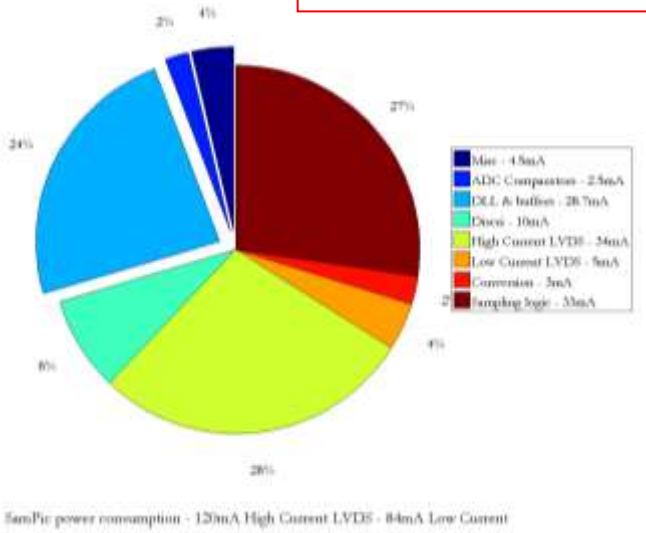


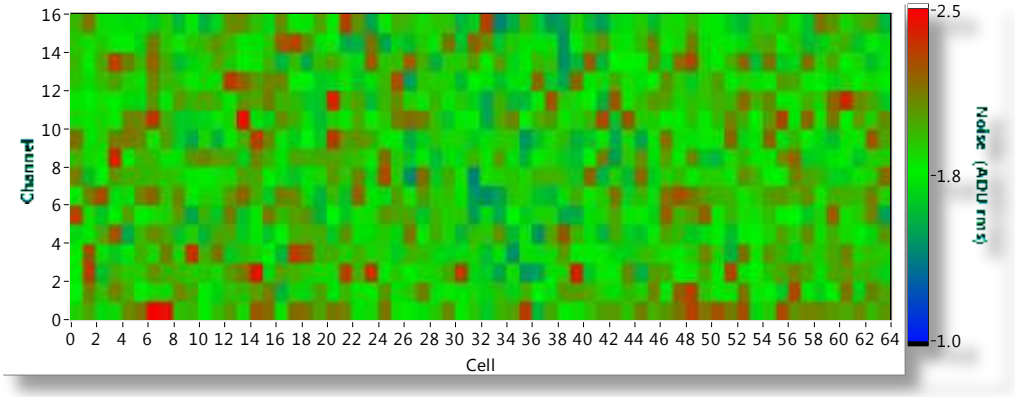
- **Readout ok up to 175 MHz (2 Gbit/s)**. To be tested at higher frequency
- No evidence of cell Leakage. **Data not damaged for storage times of few tens µs**

NOISE AND POWER CONSUMPTION

- Wilkinson ADC works well with 1.3 GHz clock
- 0.5 mV /ADC count
- ~1 V dynamic range => 11 bits digitizer
- Average Noise = **0.95 mV RMS**
- Noisiest cells are at **1.2 mV RMS**
- Unchanged with sampling frequency
- => **~10-bit rms range**
- Also tested in 9-bit mode: LSB = 2 mV, only 15% noise increase

10-15mW/ch

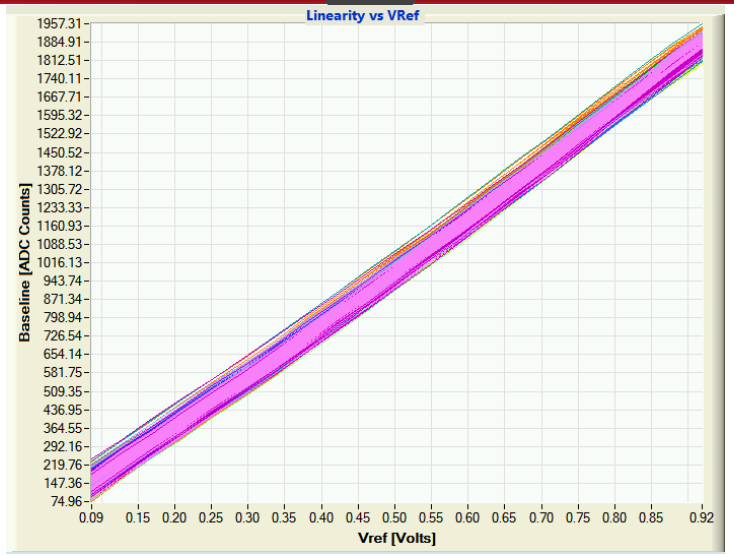


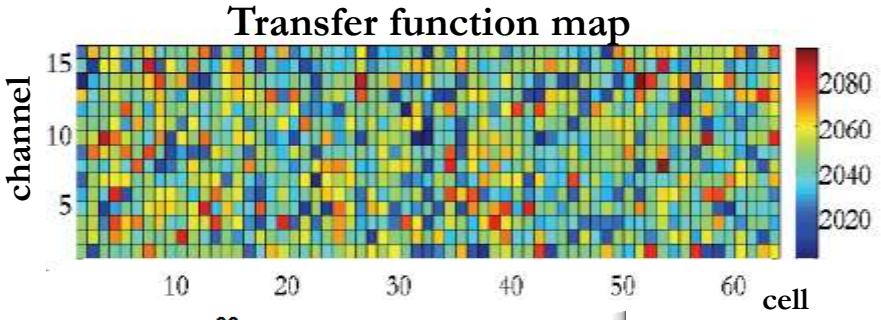


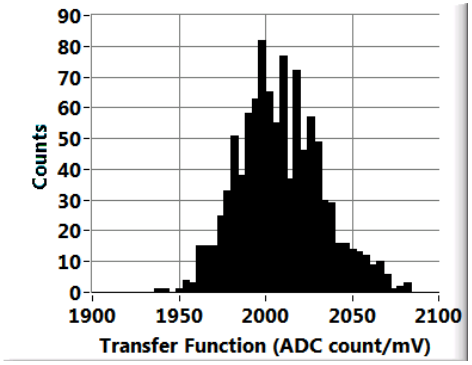
- SAMPIC @ 6.4 GS/s.
- 11-bit mode, soft trigger
- Noise map with FPN subtracted
- Noise = sqrt(variance(Cell(i)) over all the acquisitions
- Average noise = 1.9 ADC count RMS

ADC CALIBRATION AND PERFORMANCE

- Cell-to-cell spread of slopes = 1% rms with random distribution (not related to channel)
- 3% peak to peak integral non-linearity
- Both effects are systematic and due to charge injection by switches
- Can be corrected after calibration. If not, it degrades the resolution to ~7-8 bits rms
- **Already good results without correction**
- **Automatically corrected by software together with pedestals using either a linear fit or a 2nd degree polynomial.**

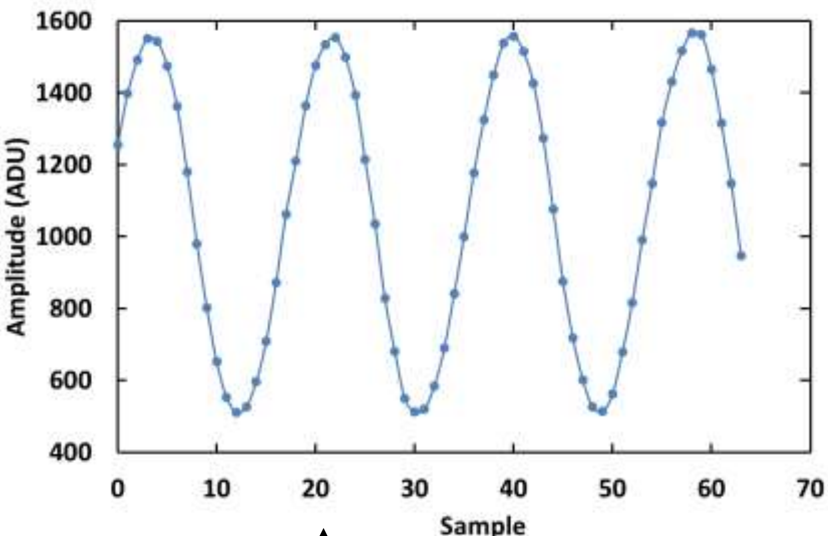


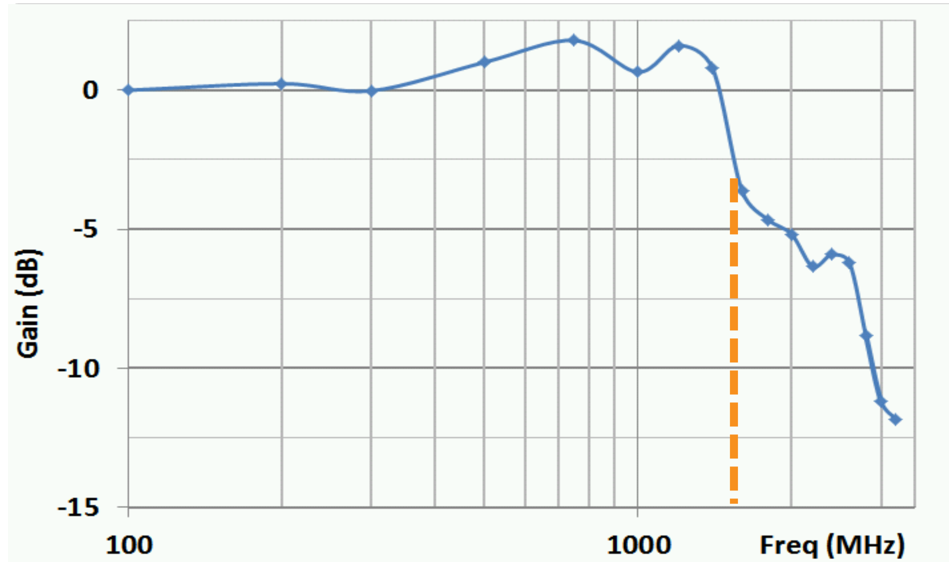




σ=1% rms

BANDWIDTH AND SIGNAL QUALITY





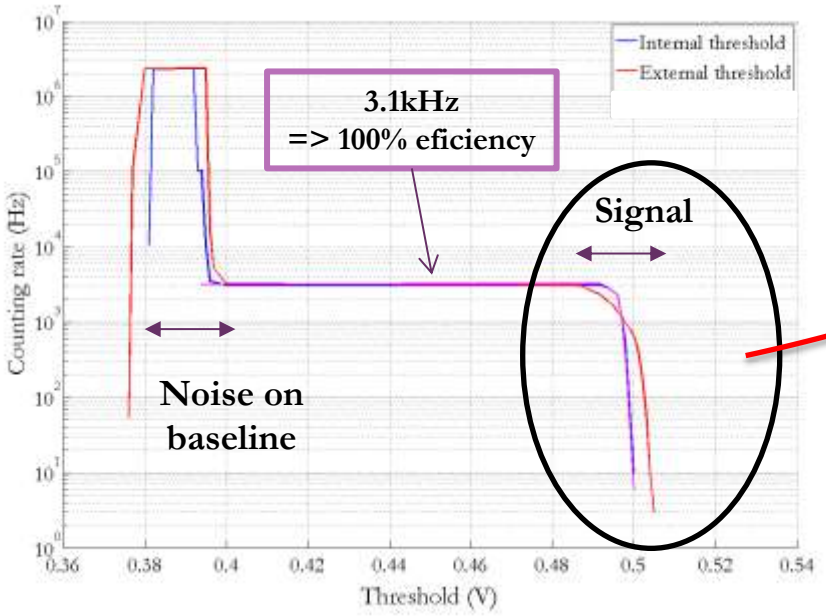
- 350 MHz sinewave (0.5V peak-peak) with 64 samples
- **'Out of the box' (no timing correction)** @ 6.4 GS/s
- 64 usable data points
- Already looks good …
- **-3dB Bandwidth ~ 1.6 GHz**
- Ringing effects probably due to problem of impedance matching at the board input
- **Crosstalk between channels is smaller than ±1%**

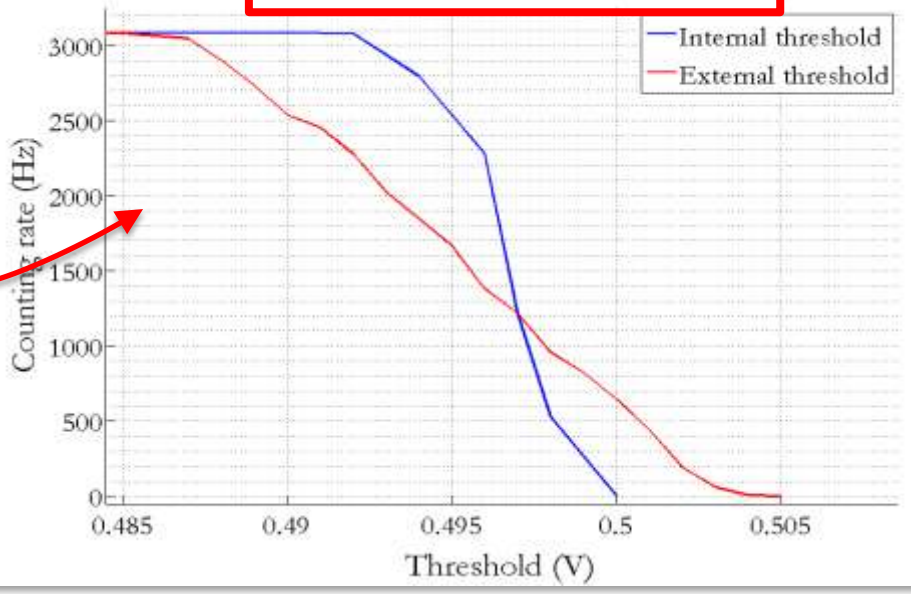
Xtalk is < +/-1% = (2%pp)

SELF-TRIGGER EFFICIENCY AND NOISE

- Input is 150 mV 1 ns wide pulses (3.1 kHz repetition rate)
- Threshold (internal or external) sweep => trigger efficiency curve
- Discriminator Noise extraction by fitting the S curve by en error function
- **Better noise if threshold internally set**

Discriminator noise:
Int threshold :2 mV rms
Ext threshold: 8 mV rms

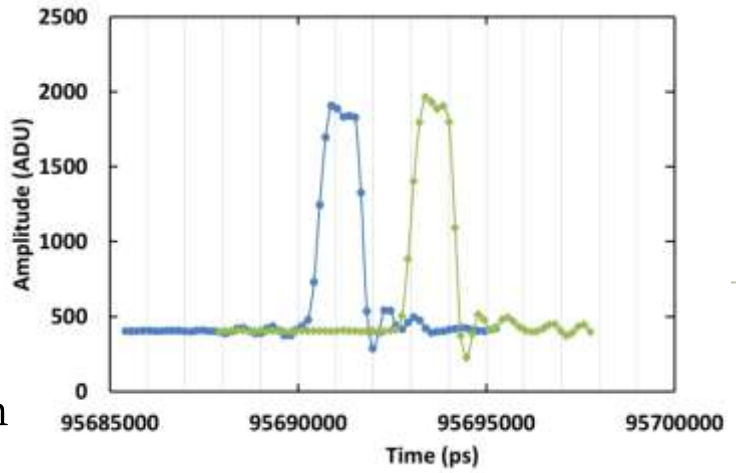




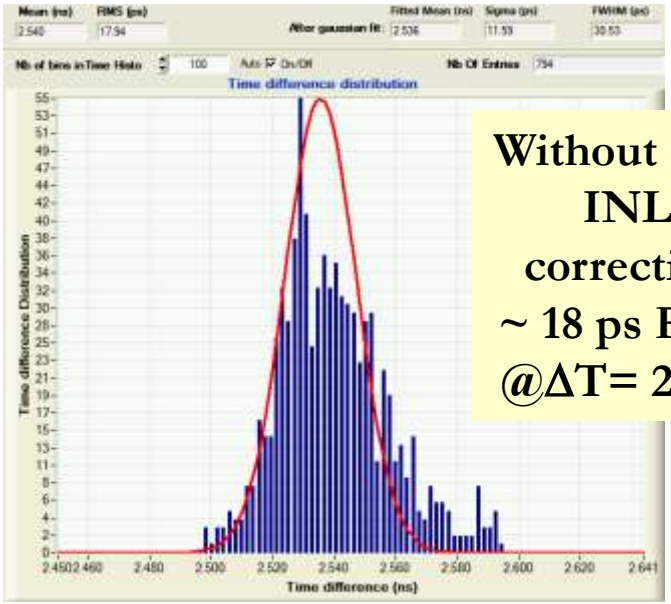
urs July 4th 2014

Timing Precision

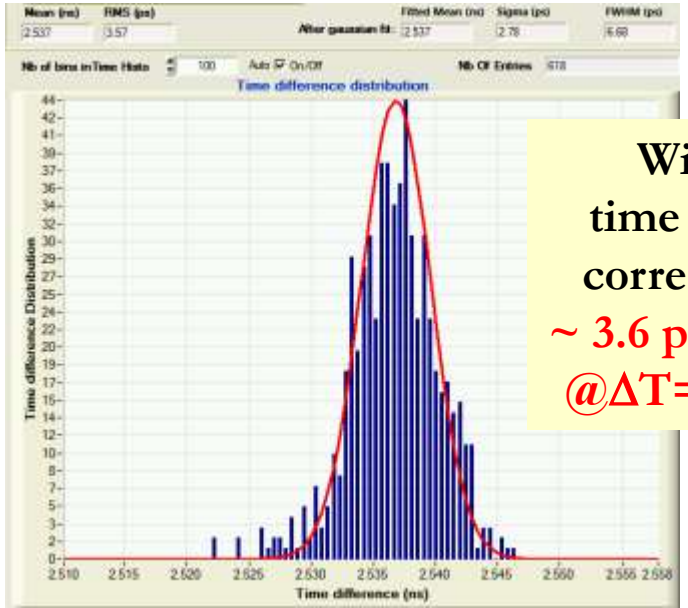
- Example of signal: 2 pulses with 2.5ns distance, **300ps risetime, 1ns FWHM**, 800mV sent on 2 channels
- Measurement performed @ 6.4 GS/s
- 18 ps rms ΔT resolution before any correction => already good.
- **3.6 ps rms ΔT resolution** after time INL correction
- No tail in the distribution.
- **No hit "out of time" due to metastabilities, no problem of boundaries between ranges, …**



Input pulses as recorded by SAMPIC

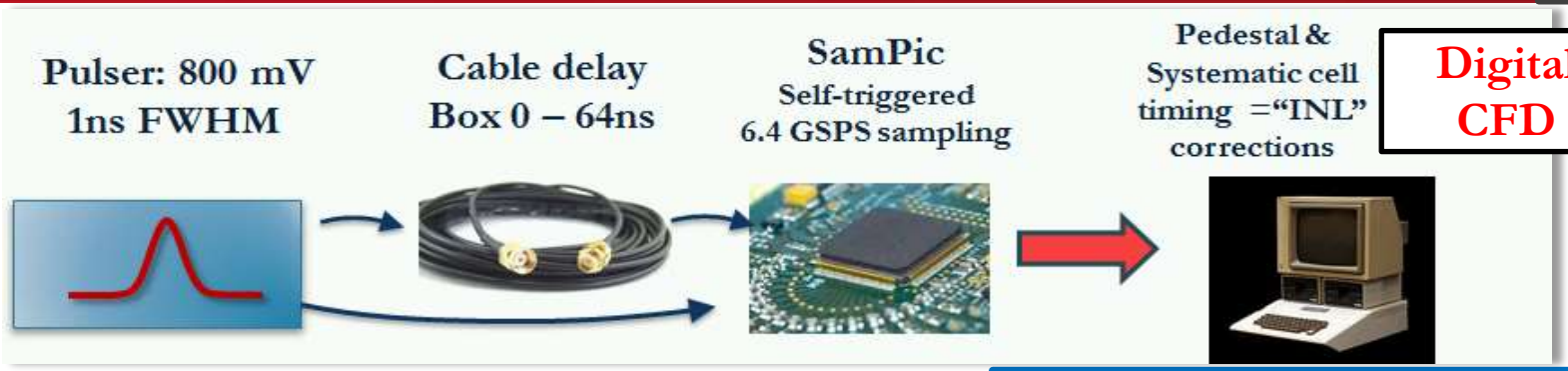


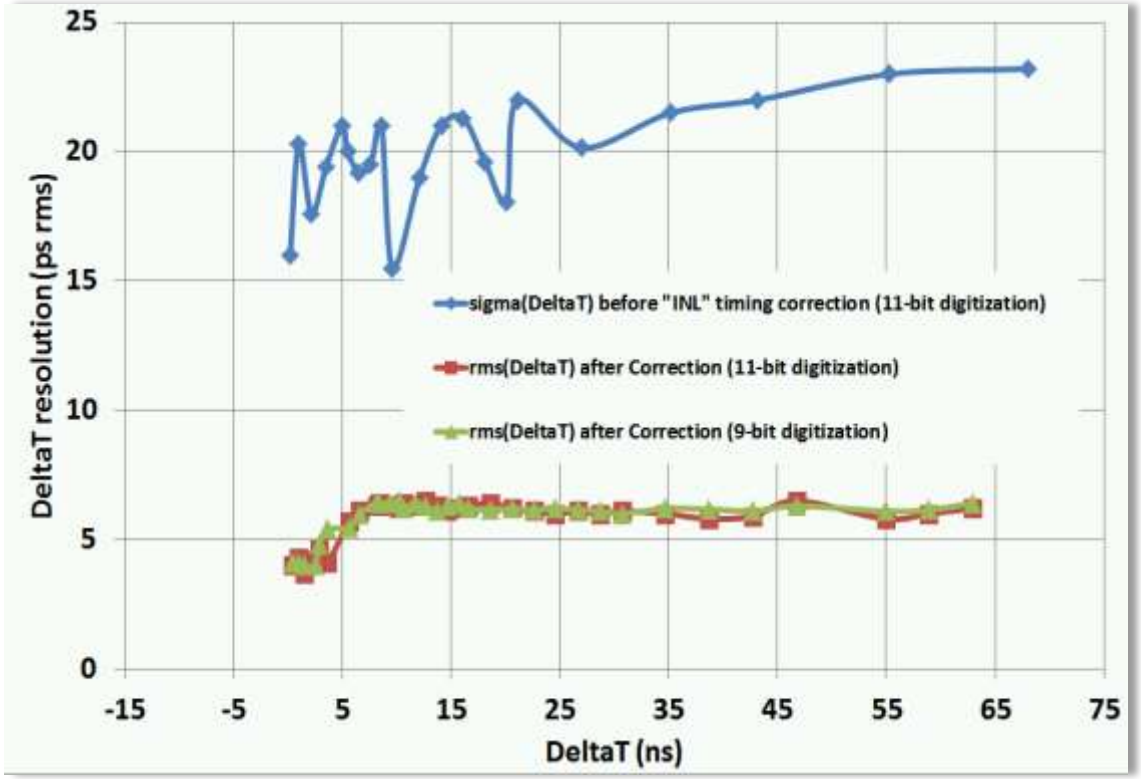
Without time INL correction ~ 18 ps RMS @ΔT= 2.5ns



With time INL correction ~ 3.6 ps RMS @ΔT=2.5ns

ΔT MEASUREMENTS. ONLY PEDESTAL CORRECTION





- <25 ps RMS one time difference without any timing calibration (short DLLs)
- <6 ps RMS timing resolution on time difference after timing "INL" correction
- Resolution vs ΔT is FLAT after 10ns
- Same results in 9-bit/400ns mode
- Correction of ADC gain spread and non-linearity not applied yet

TIMING RESOLUTION VS AMPLITUDE & RISETIME (1 NS FWHM)- 7NS DELAY, DIGITALCFD ALGORITHM

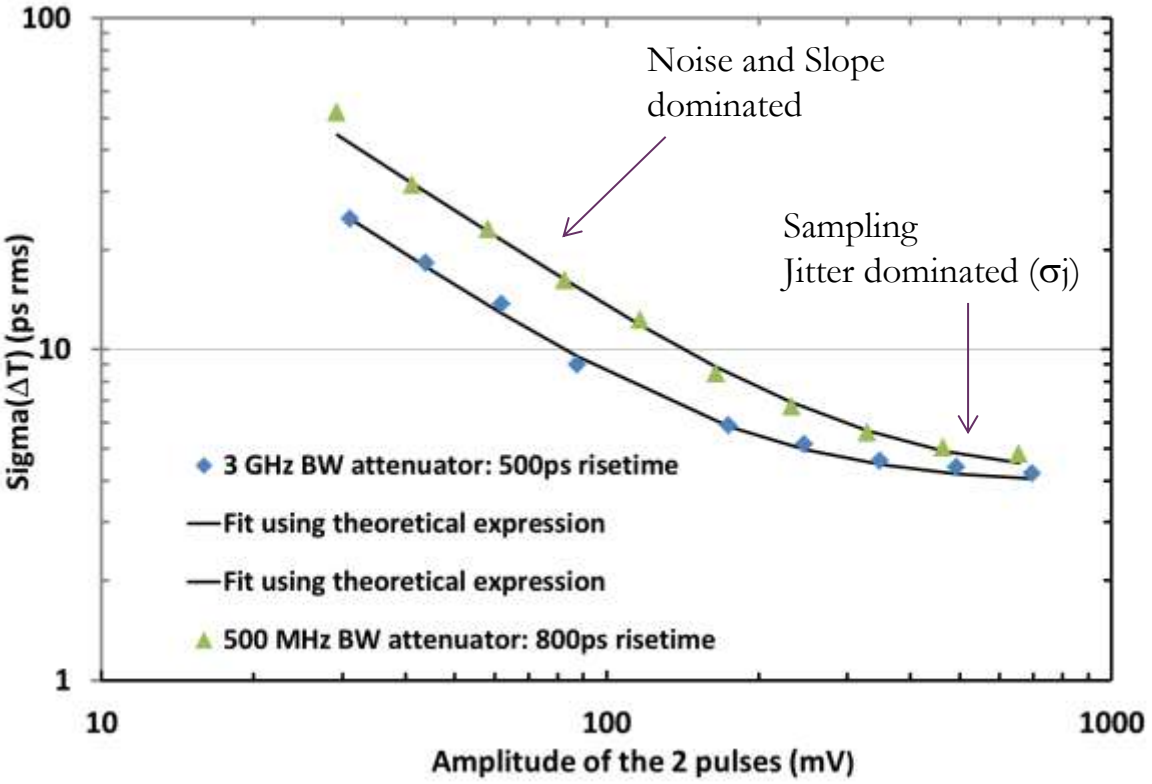
- Theoretical expression is:

$$\sigma(\Delta t) = \sqrt{2} \times \sqrt{{\sigma_j}^2 + \left(\frac{\alpha}{Amp}\right)^2}$$

with $\alpha = \frac{\sigma_n}{Nslope}$ (σ_n is the noise)

where $Nslope = \frac{1}{Amp} \times \frac{dV}{dt}$ is the normalized signal slope

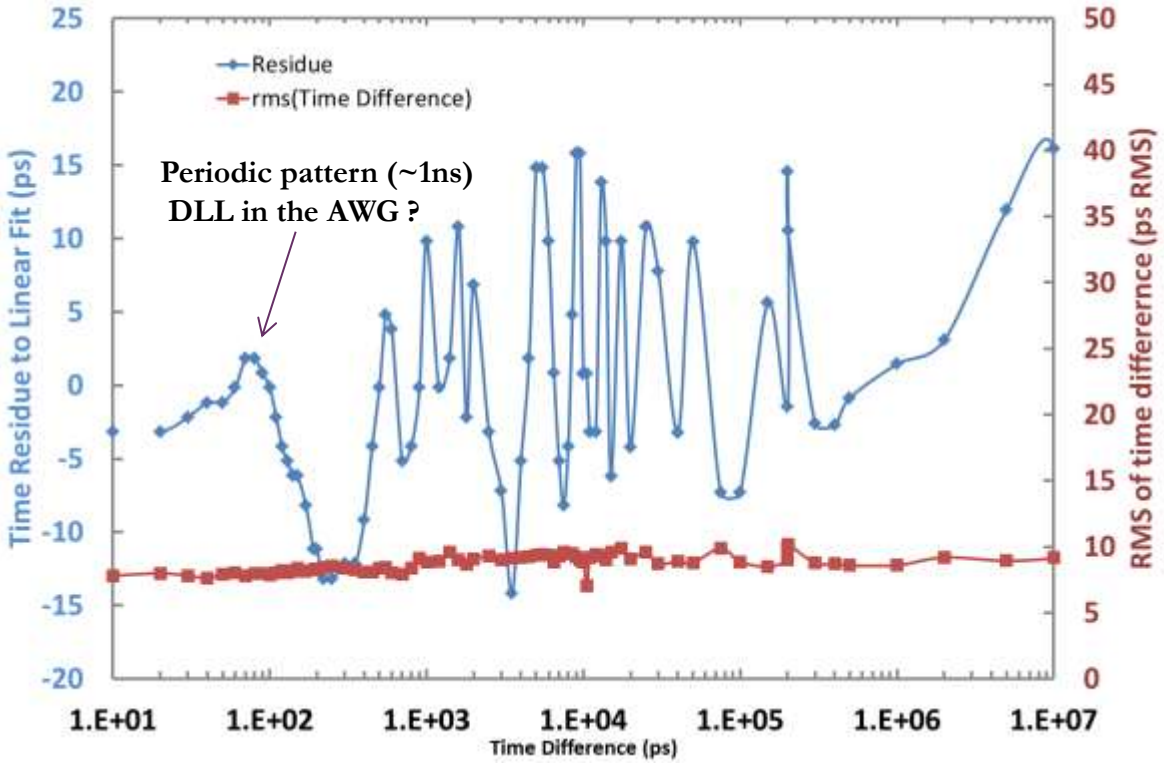
- σ_j and α extracted by fit
- σ_n extracted from α is ~ 1mV RMS
- Measurements in good agreement with the theory



Atten. BW (GHz)	σj fit (ps rms)	α fit (ps.mV)	Nslope (ns^{-1})	Calc σn (mV rms)
500	2.82	919	1.33	1.2
3	2.76	538	1.88	1.0

« ABSOLUTE » TIME MEASUREMENT ?

- Now we use a TEK 3052 arbitrary waveform generator
- Slower than precision one's (2.5ns risetime)
- We use the 2 channels of the pulser and program their delay (step of 10ps)
- Generator specified for few 10 ps delay precision and 100ps jitter (clearly better)



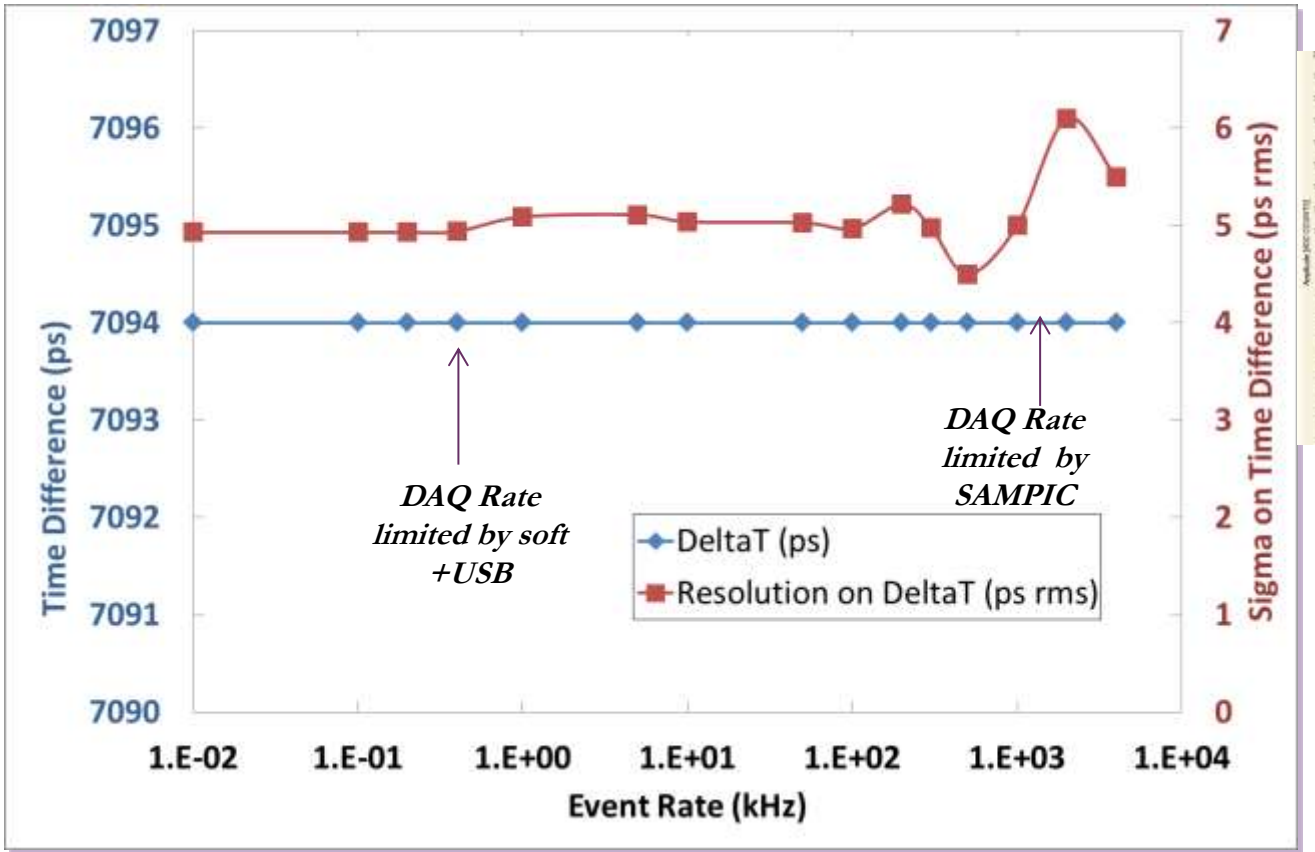
- Resolution on time difference is < 10ps RMS, even for delays up to 10 µs = 1ppm RESOLUTION
- Linear fit of the time difference vs delay programmed in the AWG:
- Slope =1 +1.3E^{-6} => ~ppm relative precision of the oscillators od SAMPIC and of the AWG
- Residue to the fit within +/-15ps up to 10µs delay

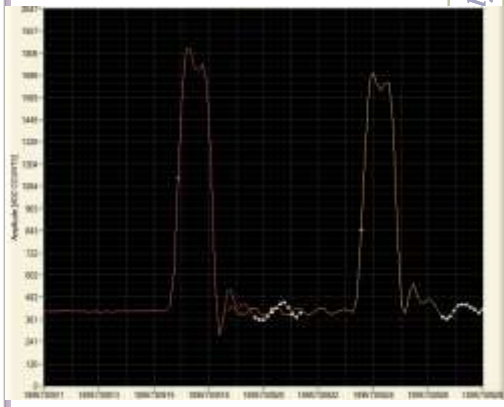
TIMING RESOLUTION VS RATE

1ns FWHM, 0.4ns risetime, 0.7V signals sent to 2 channels of SAMPIC (splitted)

- 7.1ns delay by cable, 6.4 GSPS. 11 bit mode, 64 samples, everything corrected
- Rate is progressively increased.

No change of delay measured or of resolution up 2 MHz rate !!!





SAMPIC0: PERFORMANCE SUMMARY

		Unit
Technology	AMS CMOS 0.18µm	
Number of channels	16	
Power consumption	180 (1.8V supply)	mW
Discriminator noise	2	mV rms
SCA depth	64	Cells
Sampling speed	<3-8.4 (10.2 for 8 channels only)	GSPS
Bandwidth	1.6	GHz
Range (unipolar)	~ 1	V
ADC resolution	8 to 11 (trade-off time/resolution)	bits
SCA noise	< 1	mV rms
Dynamic range	> 10	bits rms
Conversion time	0.2 (8 bits) - 1.6 (11 bits)	µs
Readout time (can be probably be /2)	25 + 6.2/sample	ns
Time precision before correction	<< 20	ps rms
Time precision after time INL correction	<< 5	ps rms

WORK PLANNED OR IN PROGRESS

- Improvements of **Firmware and DAQ** software in progress
- Characterization @ 8.2 and 10 GS/s => no drastic change on performance (with our test signals available)
- Characterization @ low (3GS/s or less) sampling rate: "PM mode".
- Timing characterization with **detectors/test beams**.
  - 3 setups are already on duty, one lent to TOTEM at CERN
  - We plan to produce 3 more ones => **possible collaborations for measurements with detectors and photons.**
- Characterization in fastest-conversion/less-resolution mode

- New submission planned for August 2014 :
  - Correction of the identified few bugs
  - Nb of bits for **coarse timestamp => 16 bits**
  - Improved "central trigger" (**coincidence** & or)
  - Channels could be **merged by groups of 2 or 4** to be used as multiple buffers to reduce dead time

CONCLUSION

A self-triggered Waveform TDC chip and its readout module and acquisition software have been designed and characterized:

- Works well with (even above) expected performance:
  - 1.6 GHz BW
  - Up to 10 GS/s
  - Low noise (trigger and acquisition)
  - **< 5ps rms single pulse timing resolution**
- Already meets our initial requirements
- Already usable for tests with detectors
- Work ongoing on:
  - Readout (firmware + software) optimization
  - Fine characterization of this first prototype
  - Second prototype

THANK YOU FOR YOUR ATTENTION

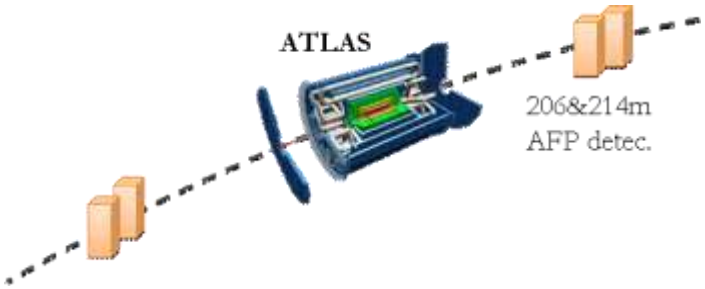
SPARE SLIDES

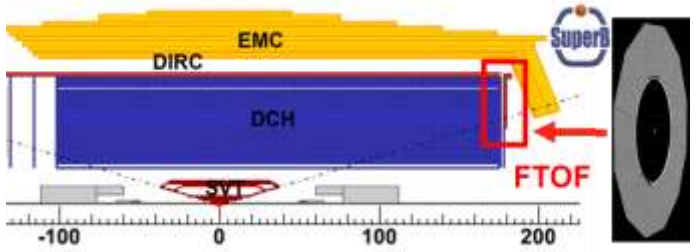
INTRODUCTION

- **ADCs** are usually used for **waveform digitization**.
  - Digitized waveform can be used to extract time information
  - High precision measurement implies high sampling rate (>> GS/s) => huge amount of data => power &cost
  - **Analog memories** nicely solve this problem but their readout deadtime (~2 to 100 μs) may be a limitation
- **TDCs** are usually used for **time measurement**
  - Information is concentrated => reduced dataflow, good for large scale measurement
  - But they do not provide information on waveform (except TOT)
- **Now what about getting a high precision TDC also providing its associated input signal => This is the WTDC**

THE SAMPIC PROJECT

- **Generic R&D** funded by "P2IO Labex" grant
- Initially intended as a common prototype ASIC for **high precision time of flight measurement (5 ps rms)** in **ATLAS AFP** and **SuperB FTOF**





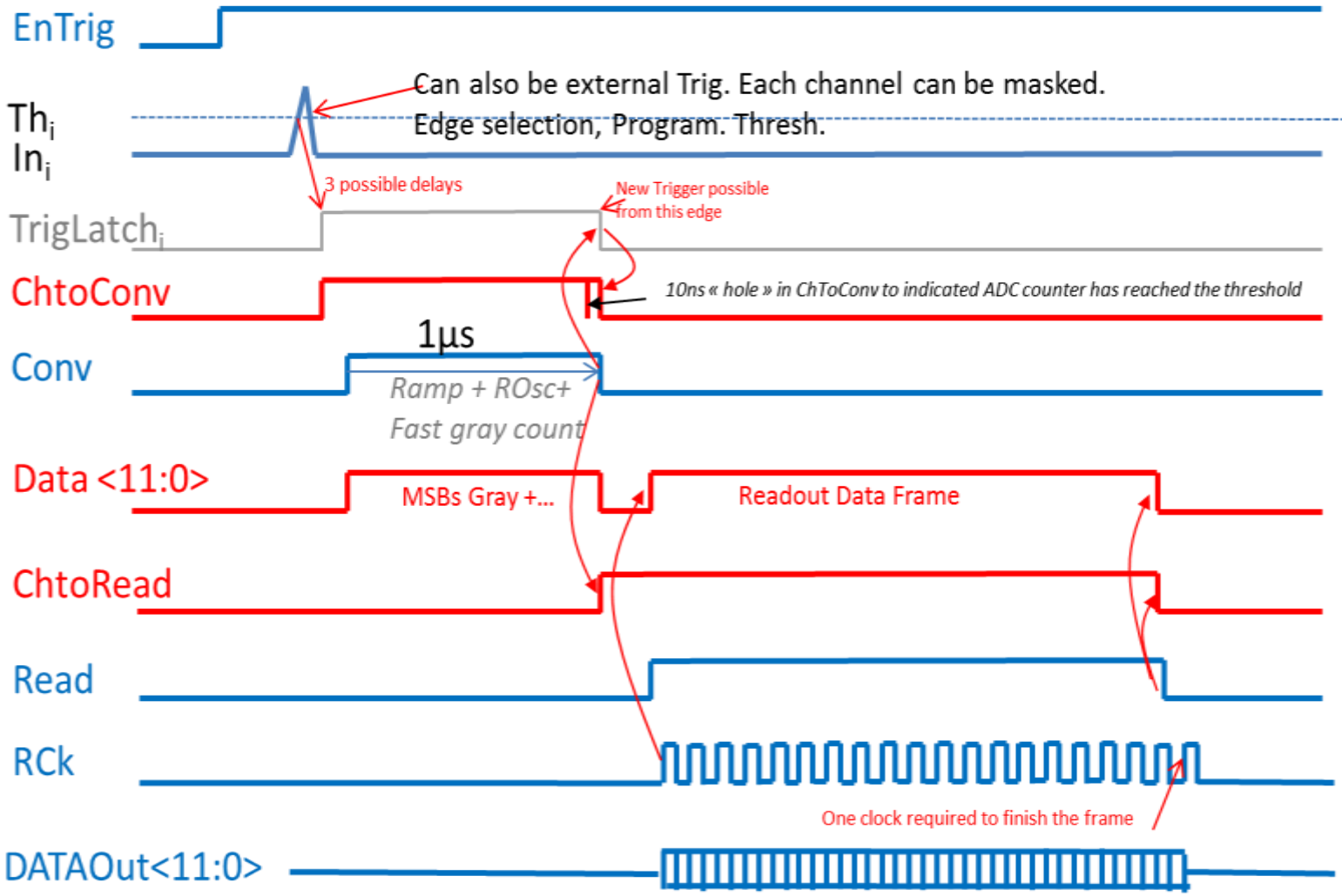
- **Goals for the first prototype (SAMPIC0, received in June 2013):**
  - **Validation of the Waveform TDC structure**
  - Evaluation of AMS 0.18µm technology for mixed design
  - **Design of a multichannel chip usable in a real environment**

  => connected to detector with a real readout and DAQ system
- Core of a future "dead-time free" chip

WHY AMS 0.18µ ?

- Based on IBM0.18µm : IBM quality & documentation
- Good Standard Cells Library
- Good lifetime foreseen (HV module, automotive)
- **1.8V power supply: nice for analog design/ high dynamic range**
- **Reasonable leakages**
- Good noise properties (already checked with IdefX chips for CdTe)
- Reasonable radiation hardness
- Less complex (and less expensive) than IBM 0.13µm
- AMS high quality Design Kit
- Easy access (CMP, Europractice, AMS)

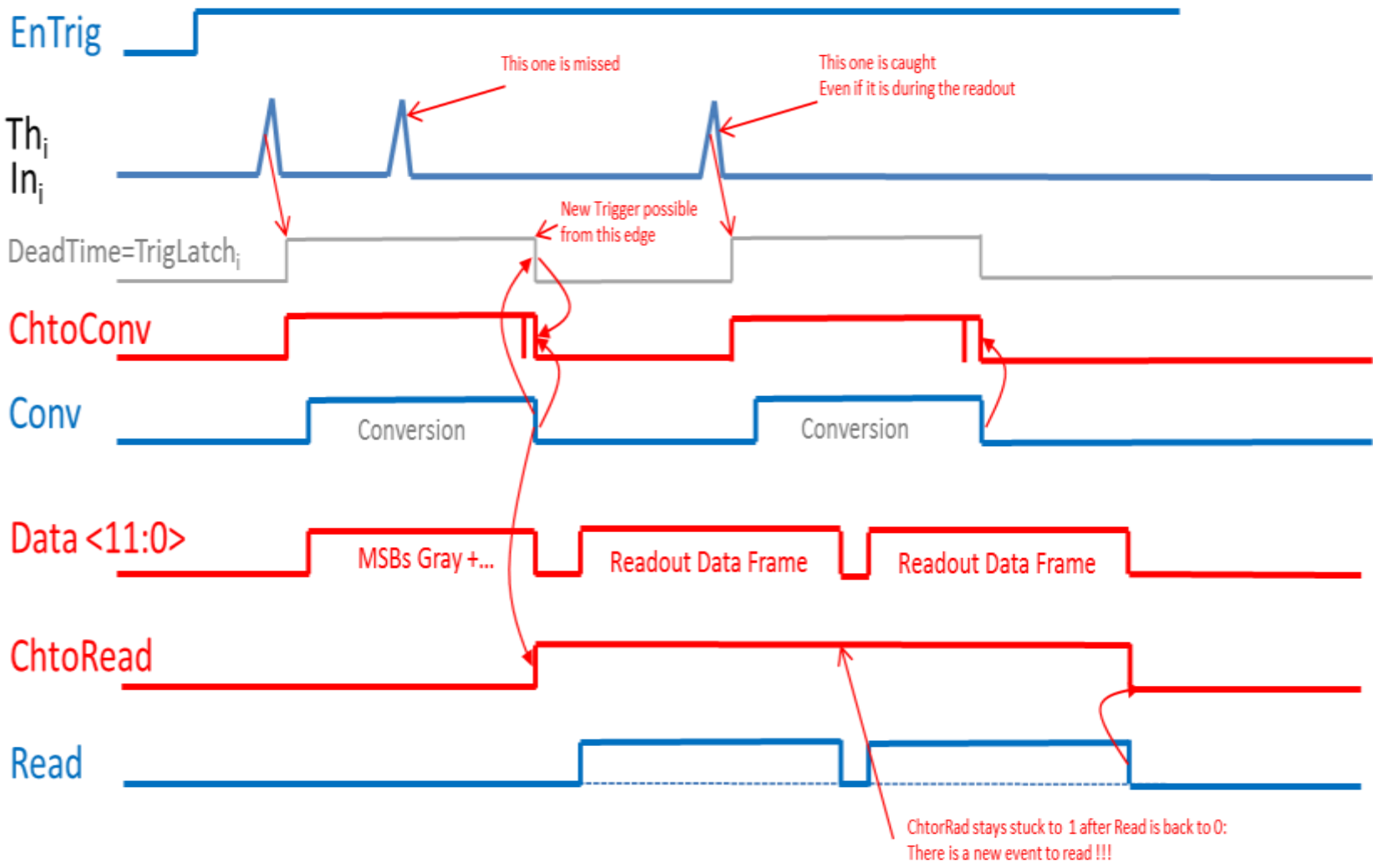
SIMPLEST OPERATION: 1 HIT, 1 CHANNEL



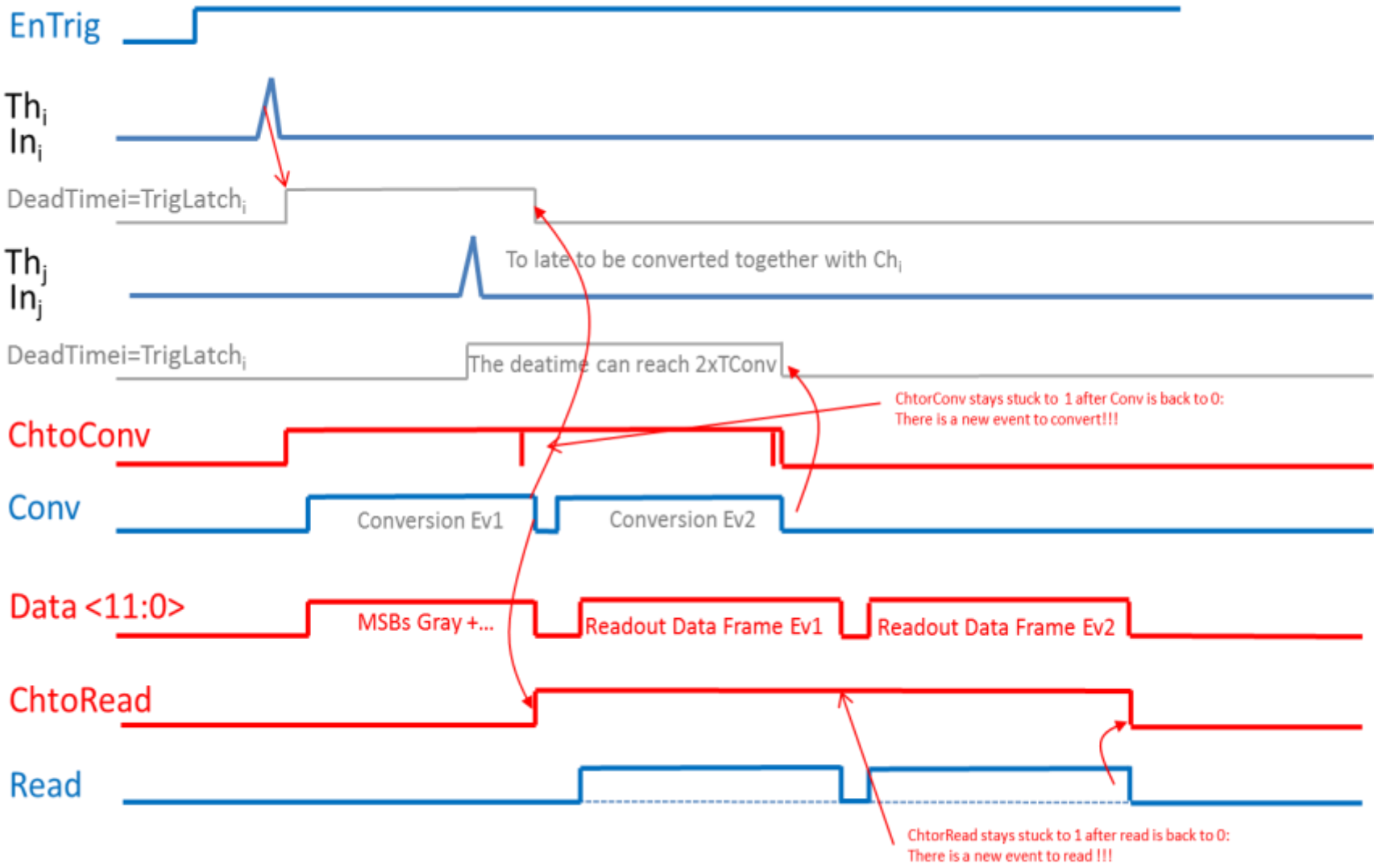
FROM SAMPIC to FPGA

TO FPGA from SAMPIC

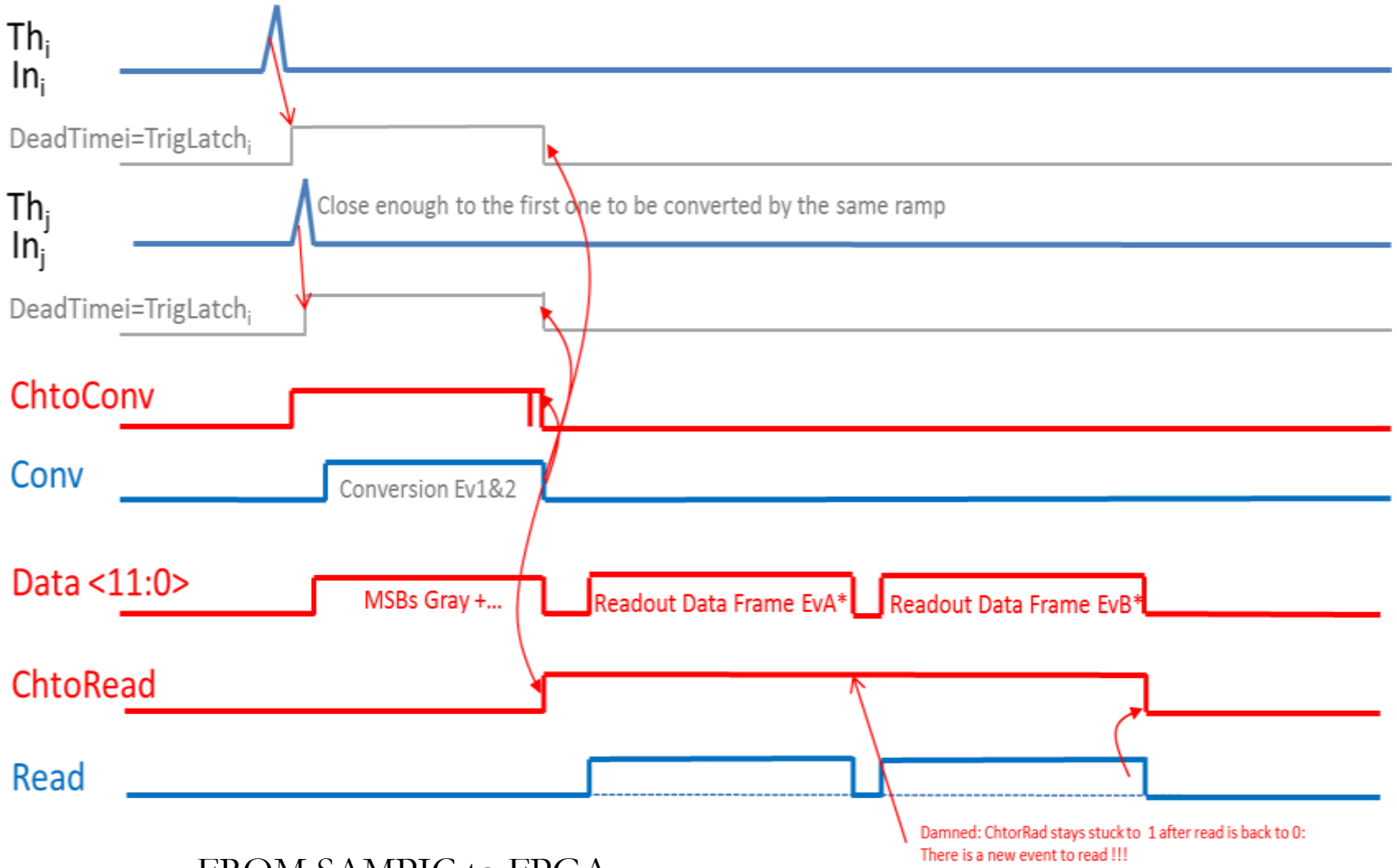
MULTIPLE HITS, 1 CHANNEL



HITS ON 2 CHANNELS, 2 CONVERSIONS



HITS ON 2 CHANNELS, SIMULTANEOUS CONVERSIONS

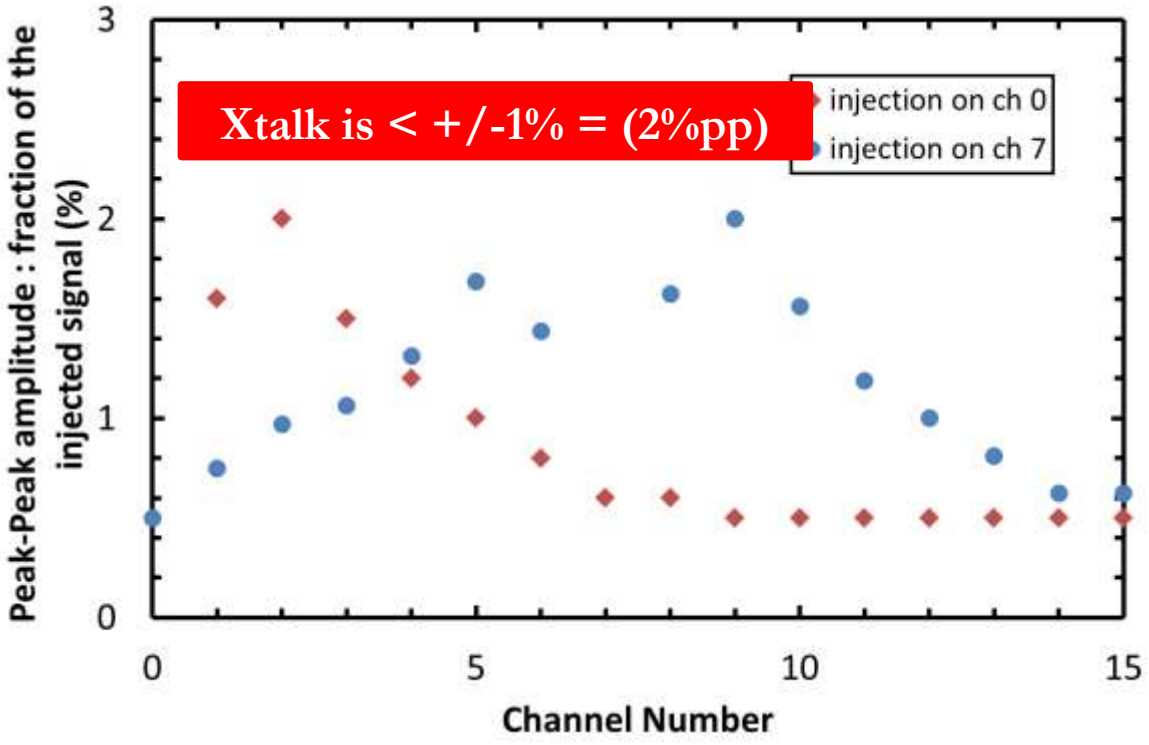


CALIBRATION PHILOSOPHY

- SCAs-based chips are suffering from reproducible non-idealities which can be easily corrected after calibration:
  - The goal is to find the set with the **best performance/complexity ratio**.
  - But also to find the right set for the **highest level of performance**.
- SAMPIC actually offers very good performance with a reduced set of calibrations :
  - **Amplitude: cell pedestal and gain** (linear or parabolic fit)
  - **Time: INL** (one offset per cell)
  - This leads to a limited volume of standard calibration data (6 Bytes/cell/sampling frequency = > 8 kBytes/chip/sampling frequency) => can easily be stored in the on-board EEPROM.
- These simple corrections could even be applied **in the FPGA**.
- Highest level calibrations permit debugging the chip and pushing the performance to its limit (still unknown).

SAMPIC0: XTALK MEASUREMENT

- 800mV, 1ns FWHM, 300ps risetime and falltime injected on **channel 7(blue)**
- Signal measured on the other channels
- Xtalk = derivative and decrease as the distance to the injection channel
- Xtalk signal is bipolar with ~ equal positive and negative lobe
- Similar plot, but shifted if injection in another channel **(red)**

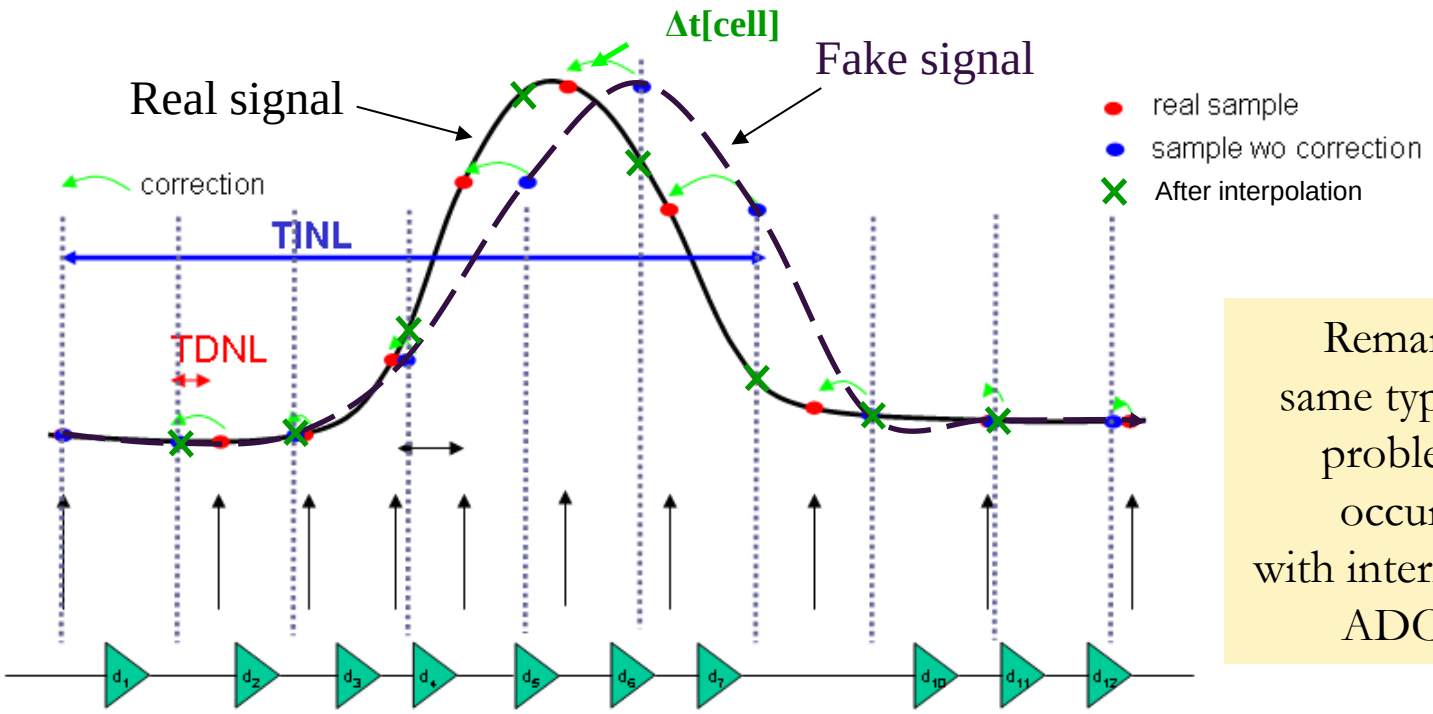


TIMING NON-LINEARITIES

- Dispersion of single delays => **time DNL**
- **Cumulative effect** => **time INL**. Gets worse with delay line length.
- **Systematic & fixed effect** => non equidistant samples => Time Base Distortion

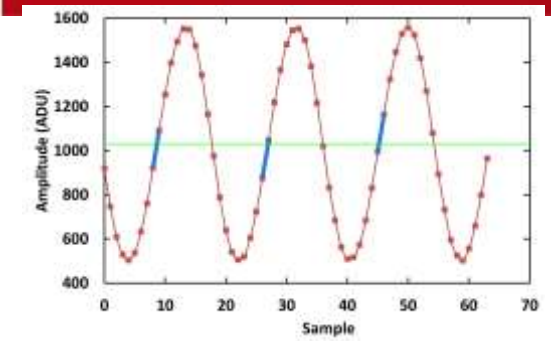
If we can measure it => we can correct it !

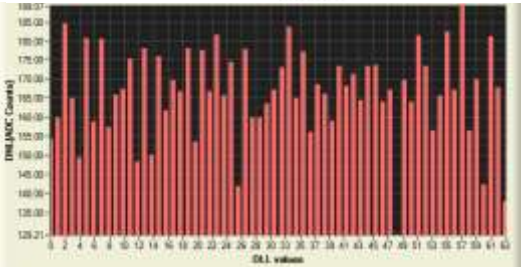
But calibration and even more correction have to remain "reasonable".

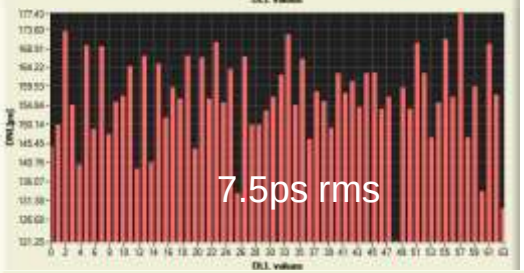


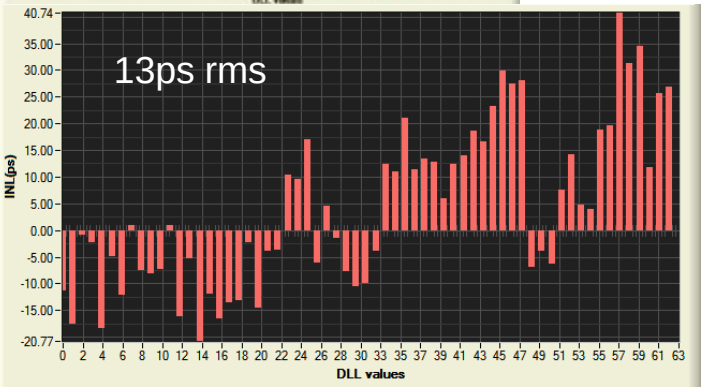
Remark:
same type of problem occurs with interleaved ADCs

TIME INL CALIBRATION AND CORRECTION









Method we introduced in 2009 and used since for our analog memories, assuming that a sinewave is nearly linear in its zero crossing region: much more precise than statistical distribution

- Search of zero-crossing segments of a free running asynchronous sine wave

  => length[position]
- Calculate the average amplitude for zero-crossing segment for each cell.
- Renormalize (divide by average amplitude for all the cells and multiply by the clock period/number of DLL steps)

  => time duration for each step = "time DNL"
- Integrate this plot:

  ⇒ Fixed Pattern Jitter = correction to apply to the time of each sample = "time INL"

Time INL correction:

- Simple addition on T_{sample}
- Also permits the calculation of real equidistant samples by interpolation or digital filtering.